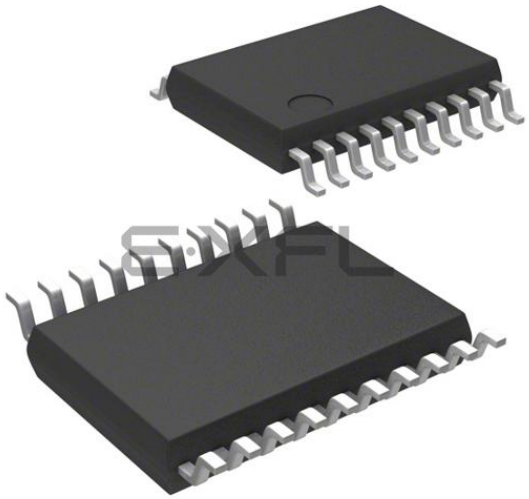

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6223ipcx

Contents

List of tables

2 Description

The STM8AF6213, STM8AF6223, STM8AF6223A and STM8AF6226 automotive 8-bit microcontrollers offer 4 to 8 Kbytes of Flash program memory, plus integrated true data EEPROM. The STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits: performance, robustness and reduced system cost.

Device performance and robustness are ensured by advanced core and peripherals made in a state-of-the-art technology, a 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 kwrite/erase cycles and a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

Table 1. STM8AF6213/23/23A/26 features

Device	STM8AF6226	STM8AF6223	STM8AF6223A	STM8AF6213
Pin count	32	20		
Max. number of GPIOs	28 including 21 high-sink I/Os	16 including 12 high-sink I/Os		
Ext. interrupt pins	28	16		
Timer CAPCOM channels	6	7	6	7
Timer complementary outputs	3	1	2	1
A/D converter channels	7	5	7	5
Low-density Flash program memory (byte)	8 K			4 K
Data EEPROM (byte)	640(1)			
RAM (byte)	1 K			
Peripheral set	Multipurpose timer (TIM1), SPI, I2C, LINUART, window WDG, independent WDG, ADC, PWM timer (TIM5), 8-bit timer (TIM6)			

1. No read-while-write (RWW) capability

4 Product overview

The following section intends to give an overview of the basic features of the products covered by this datasheet.

For more detailed information on each feature please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

4.1 Central processing unit (CPU)

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

4.1.1 Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction.

4.1.2 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

4.1.3 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

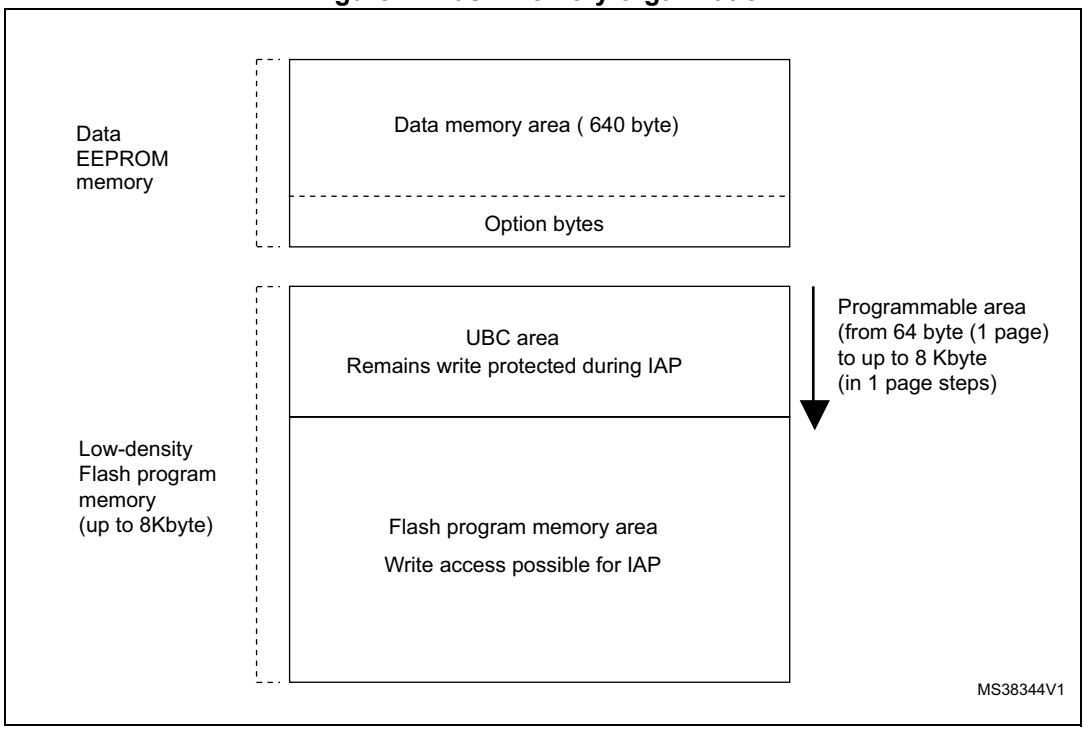
The size of the UBC is programmable through the UBC option byte, in increments of 1 page (64-byte block) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: up to 8 Kbyte minus UBC
- User-specific boot code (UBC): configurable up to 8 Kbyte

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



4.4.2 Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

4.5 Clock controller

The clock controller distributes the system clock (f_{MASTER}) coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

4.5.1 Features

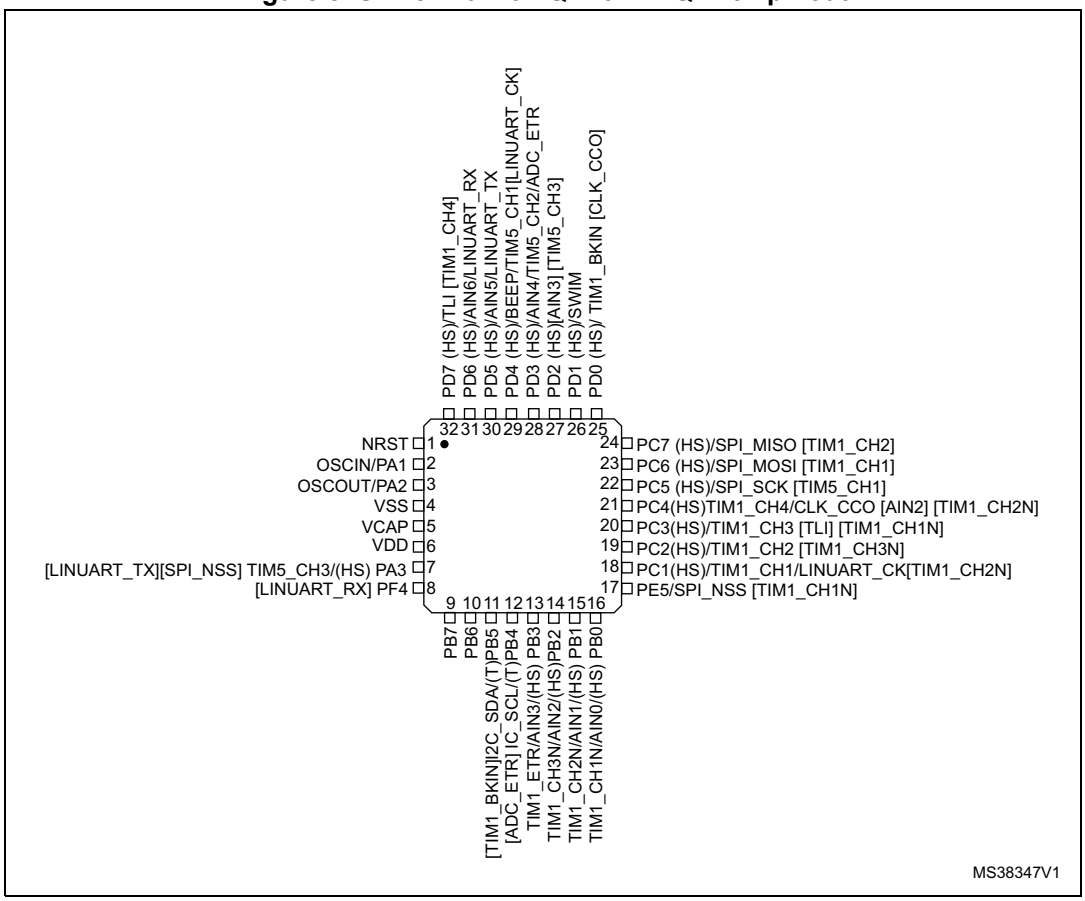
- **Clock prescaler**: to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**: Clock sources can be changed safely on the fly in Run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management**: To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** four different clock sources can be used to drive the master clock:
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- **Startup clock**: after reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS)**: this feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- **Configurable main clock output (CCO)**: This outputs an external clock for use by the application.

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	LINUART	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	TIM5	PCKEN12	Reserved	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	Reserved	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM6	PCKEN10	I^2C	PCKEN24	Reserved	PCKEN20	Reserved

5.2 LQFP32/VFQPN32 pinout and pin description

Figure 5. STM8AF6226 LQFP32/VFQPN32 pinout



1. (HS) high sink capability.
2. (T) true open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 8. STM8AF6226 LQFP32/VFQPN32 pin description

LQFP32 VFQPN32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
2	PA1/ OSCIN(2)	I/O	**X**	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
3	PA2/ OSCOUT	I/O	**X**	X	X	-	O1	X	X	Port A2	Resonator/ crystal out	-

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF
0x00 5208 to 0x00 520F	Reserved area (8 byte)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C own address register low	0x00
0x00 5214		I2C_OARH	I2C own address register high	0x00
0x00 5215		Reserved area (1 byte)		
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C clock control register low	0x00
0x00 521C		I2C_CCRH	I2C clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02
0x00 521E		I2C_PECR	I2C packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 byte)			

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 byte)			

7 Interrupt vector mapping

Table 13. Interrupt mapping

Priority	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Interrupt vector address
—	Reset	Reset	Yes	Yes	0x00 8000
—	TRAP	Software interrupt	-	-	0x00 8004
0	TLI	External top level interrupt	-	-	0x00 8008
1	AWU	Auto-wakeup from Halt	-	Yes	0x00 800C
2	Clock controller	Clock controller	-	-	0x00 8010
3	EXTI0	Port A external interrupts	Yes(1)	Yes(1)	0x00 8014
4	EXTI1	Port B external interrupts	Yes	Yes	0x00 8018
5	EXTI2	Port C external interrupts	Yes	Yes	0x00 801C
6	EXTI3	Port D external interrupts	Yes	Yes	0x00 8020
7	EXTI4	Port E external interrupts	Yes	Yes	0x00 8024
8	EXTI5	Port F	-	-	0x00 8028
9	Reserved	-	-	-	0x00 802C
10	SPI	End of transfer	Yes	Yes	0x00 8030
11	TIM1	TIM1 update/overflow/ underflow/trigger/break	-	-	0x00 8034
12	TIM1	TIM1 capture/compare	-	-	0x00 8038
13	TIM5	TIM5 update/overflow/trigger	-	-	0x00 803C
14	TIM5	TIM5 capture/compare	-	-	0x00 8040
15	Reserved	-	-	-	0x00 8044
16	Reserved	-	-	-	0x00 8048
17	LINUART	Tx complete	-	-	0x00 804C
18	LINUART	Receive register DATA FULL	-	-	0x00 8050
19	I^2C	I^2C interrupts	Yes	Yes	0x00 8054
20	Reserved	-	-	-	0x00 8058
21	Reserved	-	-	-	0x00 805C
22	ADC1	ADC1 end of conversion/analog watchdog interrupt	-	-	0x00 8060

9 Electrical characteristics

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = -40 °C, T_A = 25 °C, and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

9.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

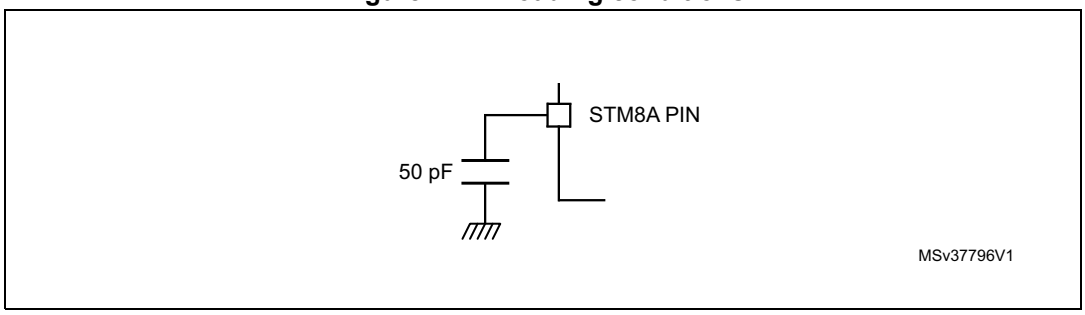
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

Figure 7. Pin loading conditions



9.3 Operating conditions

Table 26. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	-	0	16	MHz
V_{DD}	Standard operating voltage	-	3.0	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
P_D (3)	Power dissipation at T_A = 85 °C for suffix A version, T_A = 125 °C for suffix C version, T_A = 150 °C for suffix D version	TSSOP20	-	45	mW
		LQFP32	-	83	
		VQFPN32	-	TBD	-
T_A	Ambient temperature for suffix A version	Maximum power dissipation	-40	85	°C
	Ambient temperature for suffix C version		-40	125	
	Ambient temperature for suffix D version		-40	150	
T_J	Junction temperature range	Suffix A	-40	90	
		Suffix C	-40	130	
		Suffix D	-40	155	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.
3. See *Section 10.4: Thermal characteristics*.

Total current consumption in halt mode

Table 34. Total current consumption in halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max at 85°C	Max at 125°C	Max at 150°C	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	63	75	105	-	µA
		Flash in power-down mode, HSI clock after wakeup	6.0	20(1)	55(1)	80(1)	

1. Tested in production.

Table 35. Total current consumption in halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max at 85°C(1)	Max at 125°C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	60	75	100	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	17	30	

1. Guaranteed by characterization results.

Low-power mode wakeup times

Table 36. Wakeup times

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$t_{WU(WFI)}$	Wakeup time from wait mode to run mode(2)	0 to 16 MHz			-	See (3)	µs
		f_{CPU}= f_{MASTER}= 16 MHz			0.56	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator on(4)	Flash in operating mode(5)	HSI (after wakeup)	1(6)	2(6)	
					3(6)	-	
		MVR voltage regulator off			48(6)	-	
					50(6)	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode(2)	Flash in operating mode(5)			52	-	
		Flash in power-down mode(5)			54	-	

1. Guaranteed by design.
2. Measured from interrupt event to interrupt vector fetch.
3. $t_{WU(WFI)}$ = 2 x 1/f_{MASTER}+ 67 x 1/f_{CPU}.
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

Figure 13. Typ $I_{DD(RUN)}$ vs. V_{DD} HSEI RC osc., f_{CPU} = 16 MHz

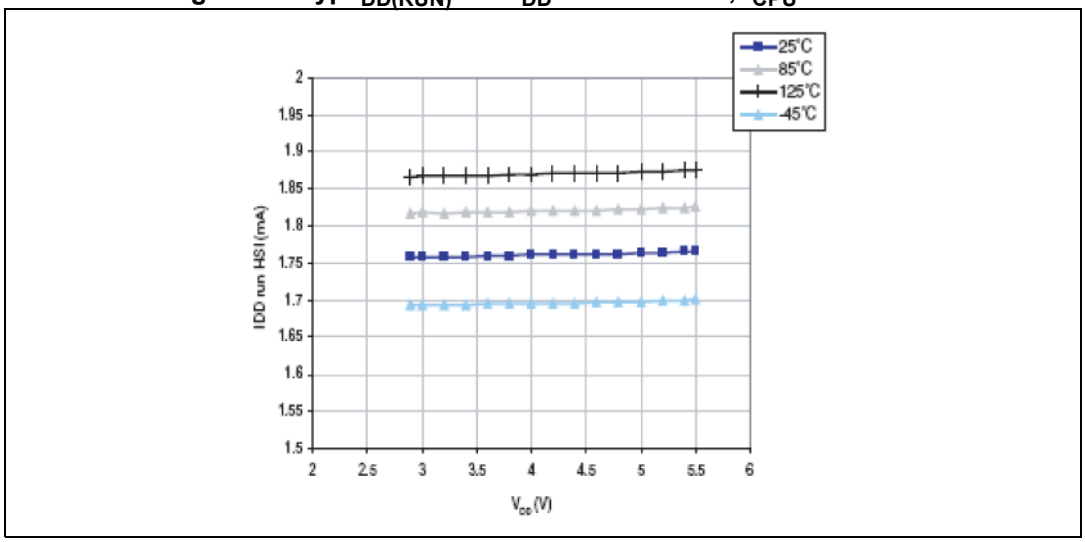
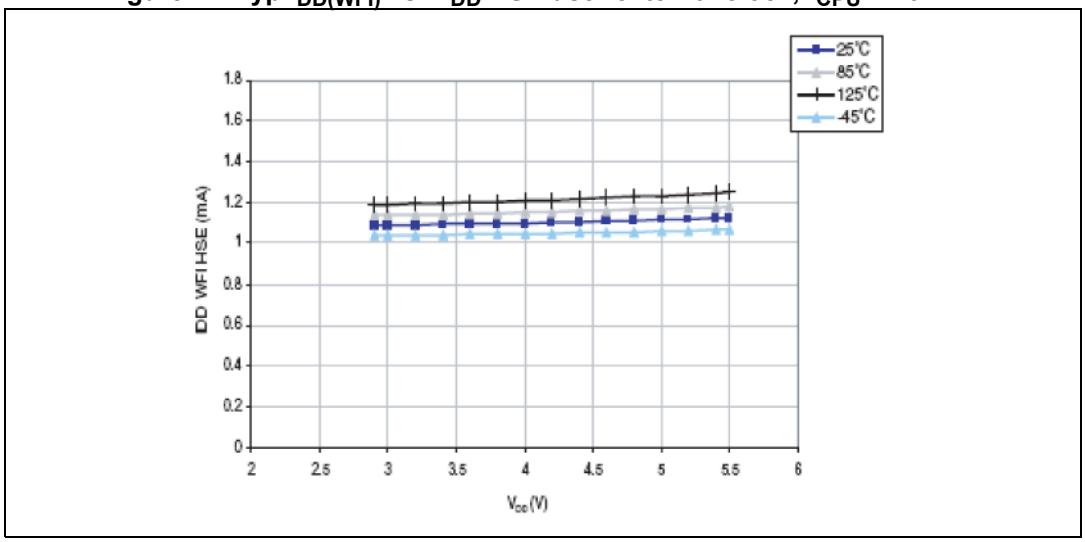


Figure 14. Typ $I_{DD(WFI)}$ vs. V_{DD} HSE user external clock, f_{CPU} = 16 MHz



HSE oscillator critical g_m formula

The crystal characteristics have to be checked with the following formula:

$$g_m \gg g_{mcrit}$$

where g_{mcrit} can be calculated with the crystal parameters as follows:

$$g_{mcrit} = (2 \times \Pi \times {}^{f}HSE)^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
$C_{L1} = C_{L2} = C$: Grounded external capacitance

9.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A.

High speed internal RC oscillator (HSI)

Table 41. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HS}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1(1)	-	1(1)	%
			-0.5(1)	-	0.5(1)	
	HSI oscillator accuracy (factory calibrated)	3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 150 °C	-5	-	5	
		3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C	-3(2)	-	3(2)	
$t_{su(HSI)}$	HSI oscillator wakeup time	-	-	-	2(3)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	170	250(3)	µA

1. Depending on option byte setting (OPT3 and NOPT3).
2. These values are guaranteed for STM8AF62xxIxx order codes only.
3. Guaranteed by characterization results.

Table 45. Flash program memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Flash program memory endurance (erase/write cycles)(1)	T_A = 25 °C	1000	-	cycles
t_{RET}	Data retention time	T_A = 25 °C	40	-	years
		T_A = 55 °C	20	-	

1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.

Table 46. Data memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Data memory endurance(1) (erase/write cycles)	T_A = 25 °C	300 k	-	cycles
		T_A = -40°C to 125 °C	100 k(2)	-	
t_{RET}	Data retention time	T_A = 25 °C	40(3)	-	years
		T_A = 55 °C	20(2)(3)	-	

1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

Table 50. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	0.8	V
	Output low level with 4 pins sunk	I_{IO} = 10 mA, V_{DD} = 3.3 V	-	1.0(1)	
		I_{IO} = 20 mA, V_{DD} = 5 V		1.5(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	4.0	-	
	Output high level with 4 pins sourced	I_{IO} = 10 mA, V_{DD} = 3.3 V	2.1(1)	-	
		I_{IO} = 20 mA, V_{DD} = 5 V	3.3(1)	-	

1. Guaranteed by characterization results.

Figure 22. Typ. V_{OL} @ V_{DD} = 5 V (standard ports)

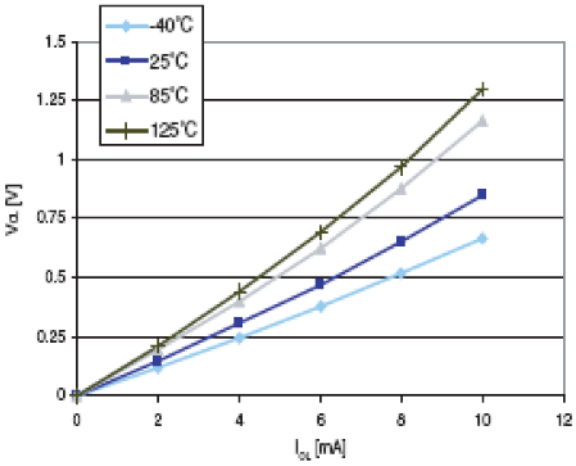


Figure 23. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

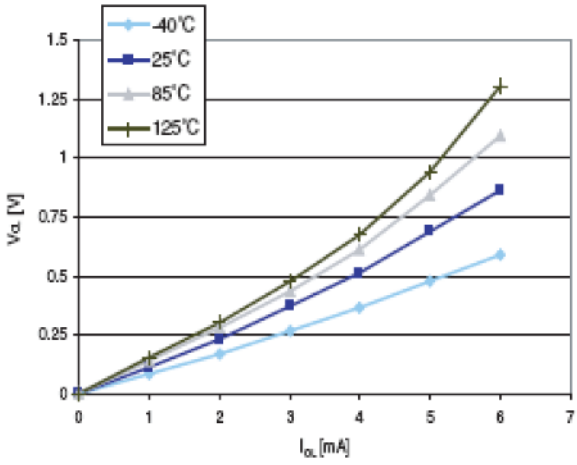
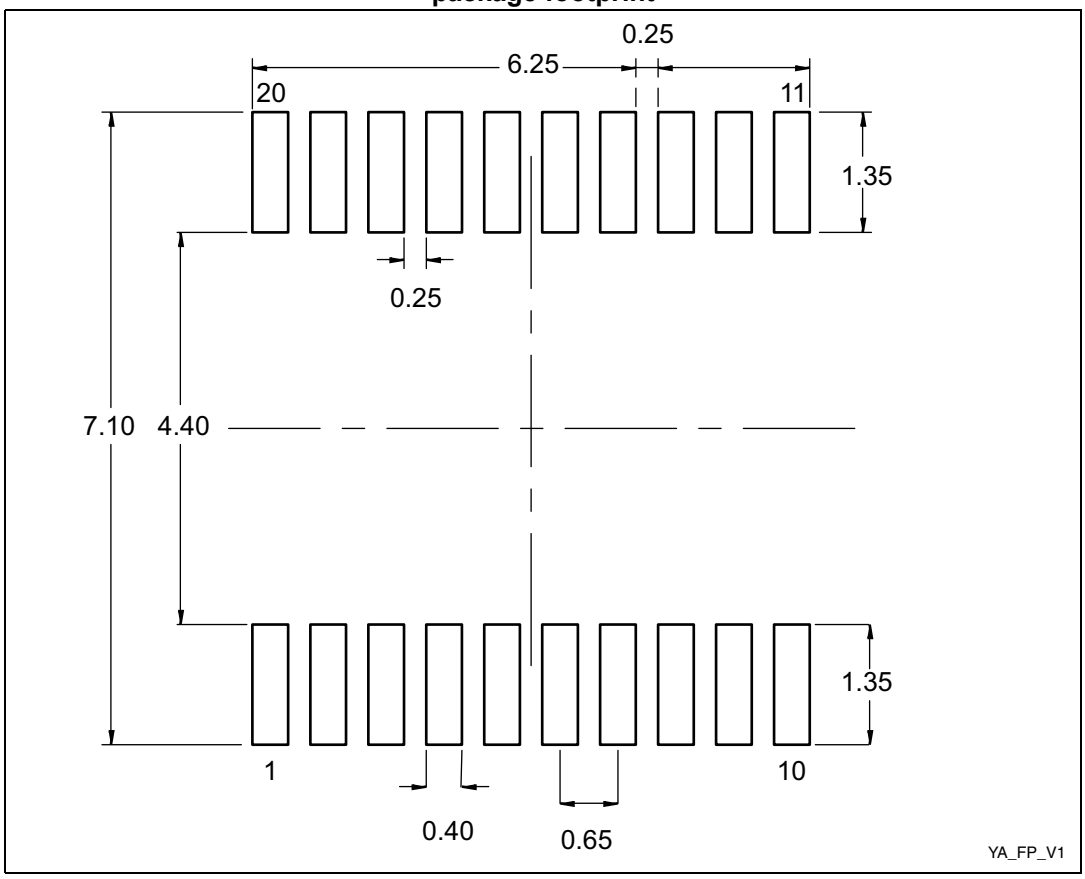


Table 62. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

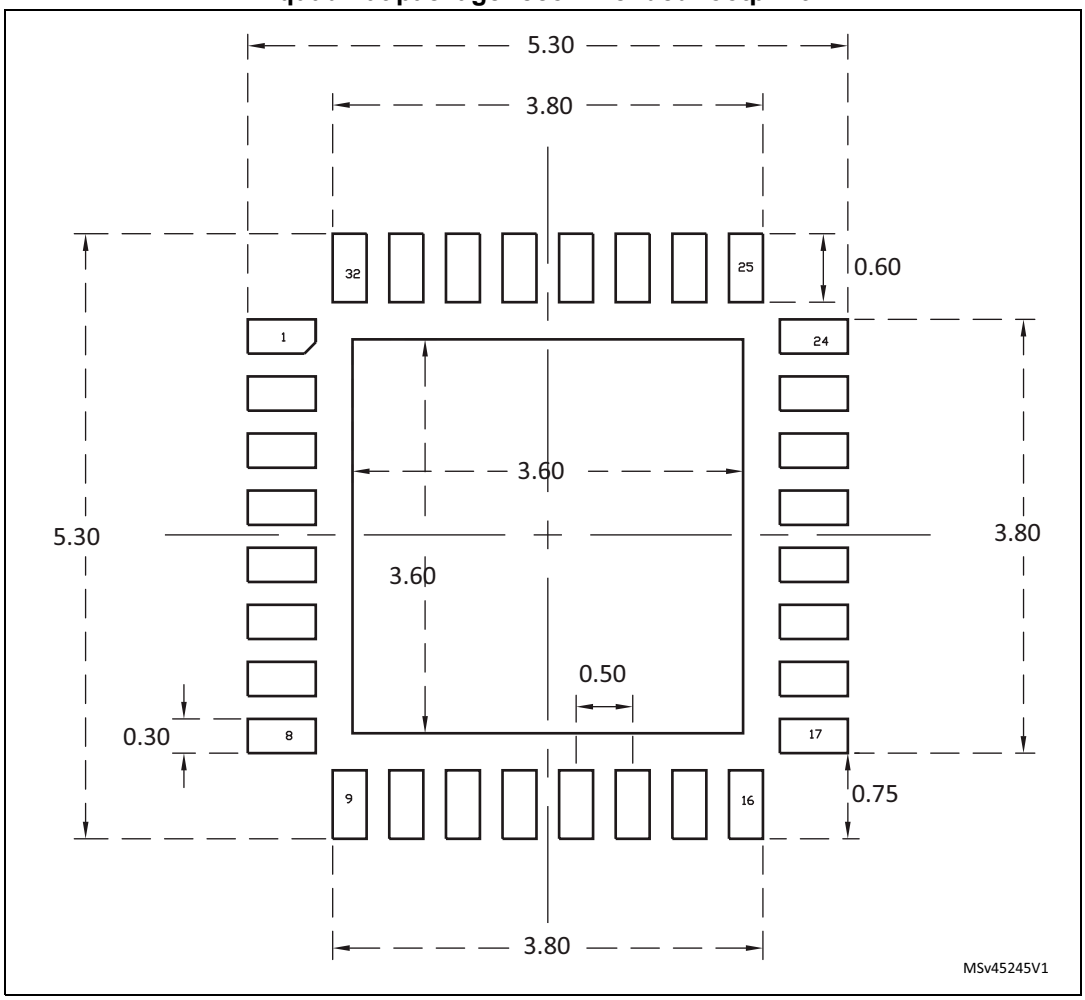
1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 46. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint



1. Dimensions are expressed in millimeters.

Figure 49. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

11 Ordering information

Table 65. STM8AF6213/23/23A/26 ordering information scheme(1)

Example	STM8A	F	62	2	3	I	P	C	A	U

Product Class

8-bit automotive microcontroller

Program memory type

F = Flash + EEPROM

Device family

62 = LIN only

Program memory size

1 = 4 Kbyte
2 = 8 Kbyte

Pin count

3 = 20 pins
6 = 32 pins

HSI accuracy

Blank = ± 5%
I = ± 3%

Package type

T = LQFP
P = TSSOP
U = VFQFPN

Temperature range

A = -40 to 85 °C
C = -40 to 125 °C
D = -40 to 150 °C

Number of ADC analog inputs

Blank = 5 analog inputs
A = 7 analog inputs

Packing

Y = Tray
U = Tube
X = Tape and reel compliant with EIA 481-C

1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.