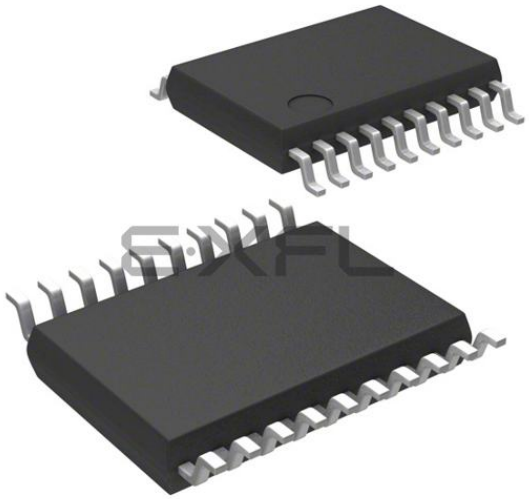

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6223pax

1 Introduction

The datasheet contains the description of STM8AF6213, STM8AF6223, STM8AF6223A and STM8AF6226 features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8 Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

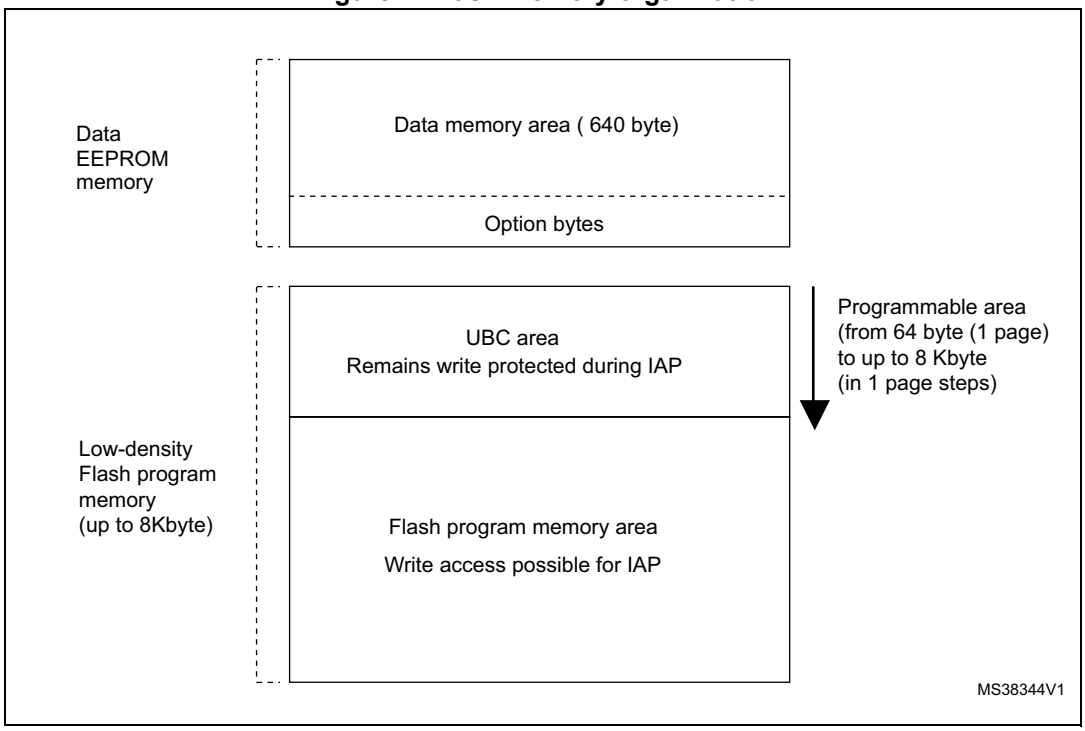
The size of the UBC is programmable through the UBC option byte, in increments of 1 page (64-byte block) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: up to 8 Kbyte minus UBC
- User-specific boot code (UBC): configurable up to 8 Kbyte

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



4.4.2 Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. Users can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- **Wait mode**: in this mode, the CPU is stopped but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- **Active-halt mode with regulator on**: in this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in Active-halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- **Active-halt mode with regulator off**: this mode is the same as Active-halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- **Halt mode**: in this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application timing perfectly. The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: at 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: the downcounter is refreshed before its value is lower than the one stored in the window register.

Table 8. STM8AF6226 LQFP32/VFQPN32 pin description (continued)

LQFP32 VFQPN32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
4	VSS	S	-	-	-	-	-	-	-	Digital ground		-
5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
6	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
7	PA3/ TIM5_CH3 [SPI_NSS] [LINUART_TX]	I/O	**X**	X	X	HS	O3	X	X	Port A3	Timer 52 channel 3	SPI master/ slave select [AFR1]/ LINUART data transmit [AFR1:0]
8	PF4 [LINUART_RX]	I/O	**X**	X	-	-	O1	X	X	Port F4	LINUART data receive [AFR1:0]	-
9	PB7	I/O	**X**	X	X	-	O1	X	X	Port B7	-	-
10	PB6	I/O	**X**	X	X	-	O1	X	X	Port B6	-	-
11	PB5/ I2C_SDA [TIM1_BKIN]	I/O	**X**	-	X	-	O1	T(3)	-	Port B5	I2C data	Timer 1 - break input [AFR4]
12	PB4/ I2C_SCL [ADC_ETR]	I/O	**X**	-	X	-	O1	T(3)	-	Port B4	I2C clock	ADC external trigger [AFR4]
13	PB3/ AIN3/TIM1_ETR	I/O	**X**	X	X	HS	O3	X	X	Port B3	Analog input 3/ Timer 1 external trigger	-
14	PB2/ AIN2/ TIM1_CH3N	I/O	**X**	X	X	HS	O3	X	X	Port B2	Analog input 2/ Timer 1 - inverted channel 3	-
15	PB1/ AIN1/ TIM1_CH2N	I/O	**X**	X	X	HS	O3	X	X	Port B1	Analog input 1/ Timer 1 - inverted channel 2	-
16	PB0/ AIN0/ TIM1_CH1N	I/O	**X**	X	X	HS	O3	X	X	Port B0	Analog input 0/ Timer 1 - inverted channel 1	-

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM5	TIM5_CR1	TIM5 control register 1	0x00
0x00 5301		TIM5_CR2	TIM5 control register 2	0x00
0x00 5302		TIM5_SMCR	TIM5 slave mode control register	0x00
0x00 5303		TIM5_IER	TIM5 interrupt enable register	0x00
0x00 5304		TIM5_SR1	TIM5 status register 1	0x00
0x00 5305		TIM5_SR2	TIM5 status register 2	0x00
0x00 5306		TIM5_EGR	TIM5 event generation register	0x00
0x00 5307		TIM5_CCMR1	TIM5 capture/compare mode register 1	0x00
0x00 5308		TIM5_CCMR2	TIM5 capture/compare mode register 2	0x00
0x00 5309		TIM5_CCMR3	TIM5 capture/compare mode register 3	0x00
0x00 530A		TIM5_CCER1	TIM5 capture/compare enable register 1	0x00
0x00 530B		TIM5_CCER2	TIM5 capture/compare enable register 2	0x00
00 530C0x		TIM5_CNTRH	TIM5 counter high	0x00
0x00 530D		TIM5_CNTRL	TIM5 counter low	0x00
0x00 530E		TIM5_PSCR	TIM5 prescaler register	0x00
0x00 530F		TIM5_ARRH	TIM5 auto-reload register high	0xFF
0x00 5310		TIM5_ARRL	TIM5 auto-reload register low	0xFF
0x00 5311		TIM5_CCR1H	TIM5 capture/compare register 1 high	0x00
0x00 5312		TIM5_CCR1L	TIM5 capture/compare register 1 low	0x00
0x00 5313		TIM5_CCR2H	TIM5 capture/compare reg. 2 high	0x00
0x00 5314		TIM5_CCR2L	TIM5 capture/compare register 2 low	0x00
0x00 5315		TIM5_CCR3H	TIM5 capture/compare register 3 high	0x00
0x00 5316		TIM5_CCR3L	TIM5 capture/compare register 3 low	0x00
0x00 5317 to 0x00 533F	Reserved area (43 byte)			
0x00 5340	TIM6	TIM6_CR1	TIM6 control register 1	0x00
0x00 5341		TIM6_CR2	TIM6 control register 2	0x00
0x00 5342		TIM6_SMCR	TIM6 slave mode control register	0x00
0x00 5343		TIM6_IER	TIM6 interrupt enable register	0x00
0x00 5344		TIM6_SR	TIM6 status register	0x00
0x00 5345		TIM6_EGR	TIM6 event generation register	0x00
0x00 5346		TIM6_CNTR	TIM6 counter	0x00
0x00 5347		TIM6_PSCR	TIM6 prescaler register	0x00
0x00 5348		TIM6_ARR	TIM6 auto-reload register	0xFF

6.2.2 CPU/SWIM/debug module/interrupt controller registers

Table 12. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 byte)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)			

Table 13. Interrupt mapping (continued)

Priority	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Interrupt vector address
23	TIM6	TIM6 update/overflow/trigger	-	-	0x00 8064
24	Flash	EOP/WR_PG_DIS	-	-	0x00 8068

1. Except PA1.

Table 15. Option byte description (continued)

Option byte no.	Description
OPT4	**EXTCLK: External clock selection** 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: Auto-wakeup unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0]: AWU clock prescaler 0x: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]: HSE crystal oscillator stabilization time** 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles

8.2 STM8AF6213/23/23A/26 alternate function remapping bits

Table 16. STM8AF6226 alternate function remapping bits [7:2] for 32-pin packages

Option byte number	Description(1)
OPT2	**AFR7: Alternate function remapping option 7** 0: AFR7 remapping option inactive: default alternate function (2) 1: Port C3 alternate function = = TIM1_CH1N; port C4 alternate function = TIM1_CH2N **AFR6: Alternate function remapping option 6** 0: AFR6 remapping option inactive: default alternate function (2) 1: Port D7 alternate function = TIM1_CH4. **AFR5: Alternate function remapping option 5** 0: AFR5 remapping option inactive: default alternate function (2). 1: Port D0 alternate function = CLK_CCO. **AFR4: Alternate function remapping option 4** 0: AFR4 remapping option inactive: default alternate function (2). 1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN. **AFR3: Alternate function remapping option 3** 0: AFR3 remapping option inactive: default alternate function (2) 1: Port C3 alternate function = TLI **AFR2: Alternate function remapping option 2** 0: AFR2 remapping option inactive: default alternate function (2) 1: Port C4 alternate function = AIN2; port D2 alternate function = AIN3; port D4 alternate function = LINUART_CK

1. Do not use more than one remapping option in the same port.
2. Refer to the pin description.

9.3 Operating conditions

Table 26. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	-	0	16	MHz
V_{DD}	Standard operating voltage	-	3.0	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
P_D (3)	Power dissipation at T_A = 85 °C for suffix A version, T_A = 125 °C for suffix C version, T_A = 150 °C for suffix D version	TSSOP20	-	45	mW
		LQFP32	-	83	
		VQFPN32	-	TBD	-
T_A	Ambient temperature for suffix A version	Maximum power dissipation	-40	85	°C
	Ambient temperature for suffix C version		-40	125	
	Ambient temperature for suffix D version		-40	150	
T_J	Junction temperature range	Suffix A	-40	90	
		Suffix C	-40	130	
		Suffix D	-40	155	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.
3. See *Section 10.4: Thermal characteristics*.

Figure 15. Typ $I_{DD(WFI)}$ vs. f_{CPU} HSE user external clock, V_{DD} = 5 V

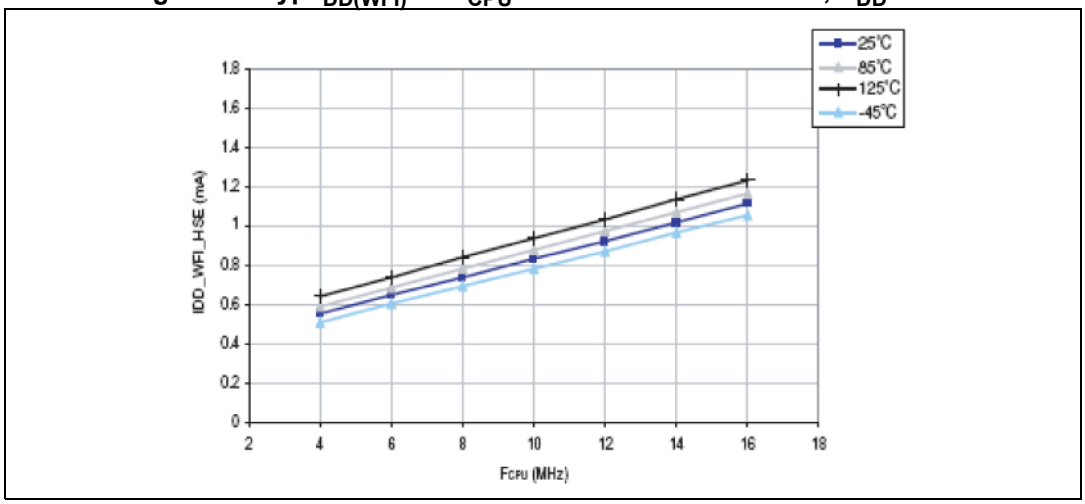
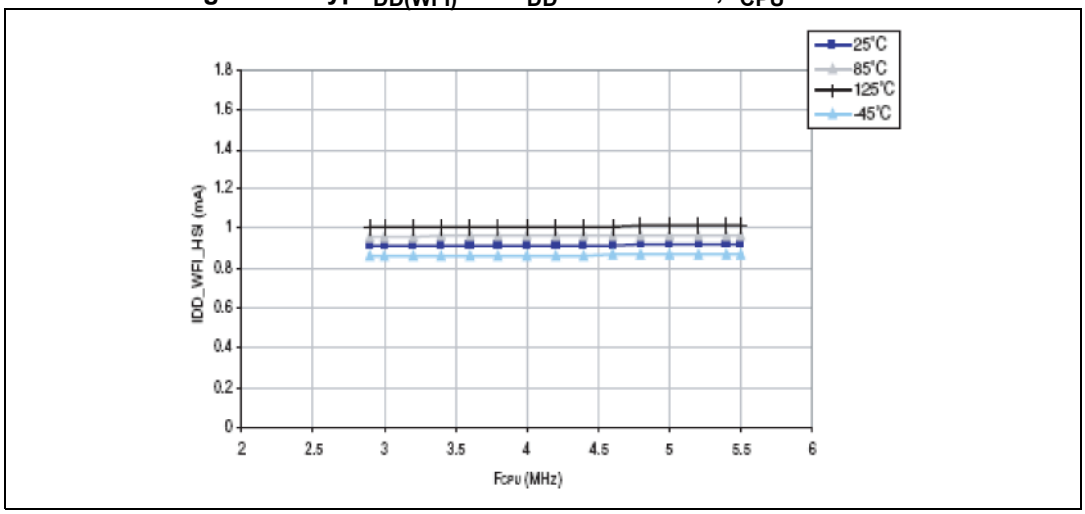


Figure 16. Typ $I_{DD(WFI)}$ vs. V_{DD} HSI RC osc., f_{CPU} = 16 MHz



HSE crystal/ceramic resonator oscillator

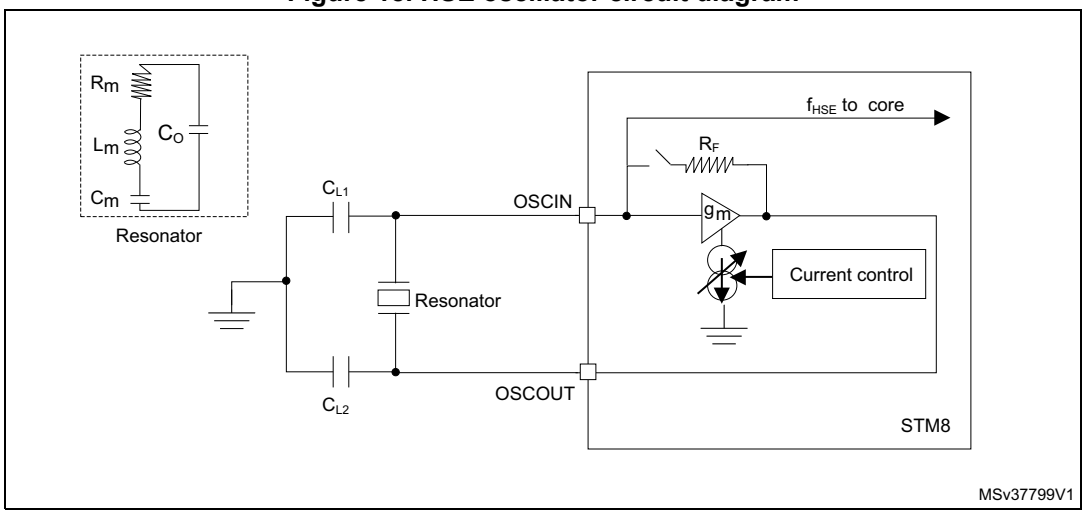
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 40. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high-speed oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	220	-	kΩ
$C^{(1)}$	Recommended load capacitance(2)	-	-	-	20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz	-	-	6 (startup) 1.6 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} = 16 MHz	-	-	6 (startup) 1.2 (stabilized)(3)	
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. C is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value. Refer to the crystal manufacturer for more details.
3. Guaranteed by characterization results.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) until a stabilized 16 MHz oscillation is reached. The value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 18. HSE oscillator circuit diagram



Low speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 42. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	110(1)	128	150(1)	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7	µs
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	5	-	µA

1. Tested in production.

9.3.5 Memory characteristics

RAM and hardware registers

Table 43. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	V_{IT-max}(2)	V

1. Minimum supply voltage without losing the data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design.
2. Refer to the operating conditions for the value of V_{IT-max}

Flash program memory/data EEPROM memory

General conditions: T_A = -40 to 150 °C.

Table 44. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU} is 0 to 16 MHz with 0 ws	3.0	-	5.5	V
	Operating voltage (code execution)		2.6	-	5.5	
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 byte/64 byte)	-	-	6.0	6.6	ms
	Fast programming time for 1 block (64 byte)	-	-	3.0	3.3	
t_{ERASE}	Erase time for 1 block (64 byte)	-	-	3.0	3.3	

Table 45. Flash program memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Flash program memory endurance (erase/write cycles)(1)	T_A = 25 °C	1000	-	cycles
t_{RET}	Data retention time	T_A = 25 °C	40	-	years
		T_A = 55 °C	20	-	

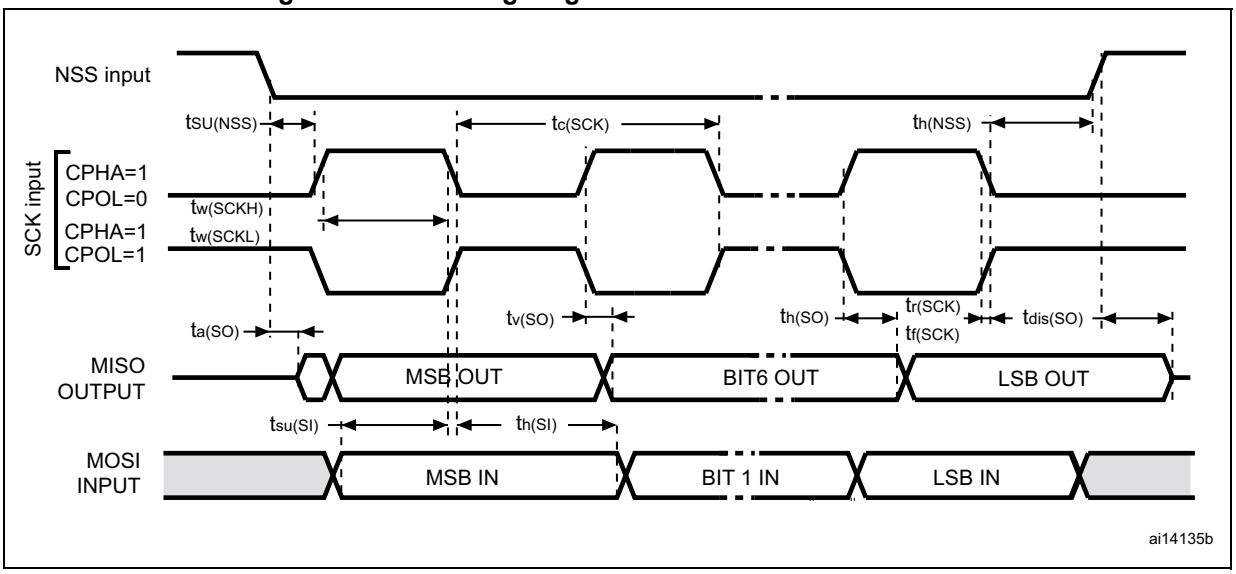
1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.

Table 46. Data memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Data memory endurance(1) (erase/write cycles)	T_A = 25 °C	300 k	-	cycles
		T_A = -40°C to 125 °C	100 k(2)	-	
t_{RET}	Data retention time	T_A = 25 °C	40(3)	-	years
		T_A = 55 °C	20(2)(3)	-	

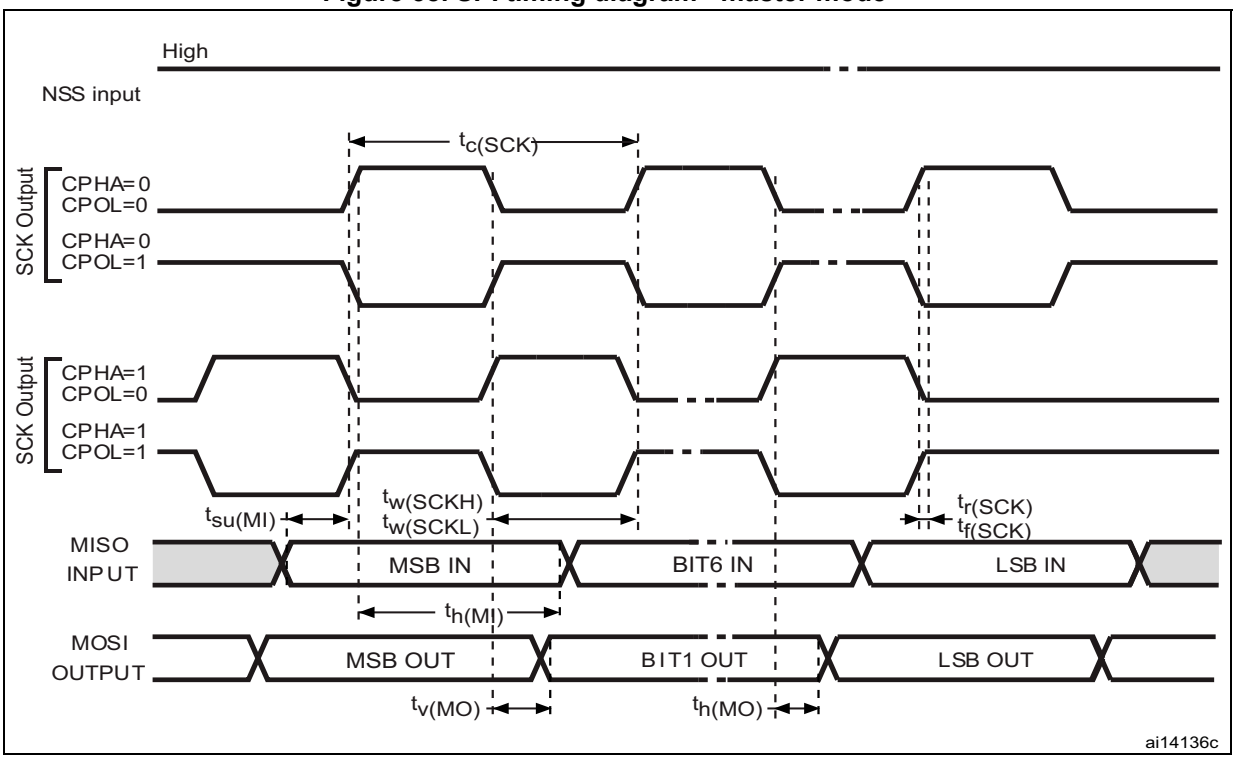
1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

Figure 37. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 38. SPI timing diagram - master mode(1)



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

9.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

Table 54. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DD} = 3 to 5.5 V	1	-	4	MHz
		V_{DD} = 4.5 to 5.5 V	1	-	6	
V_{AIN}	Conversion voltage range(1)	-	V_{SS}	-	V_{DD}	V
V_{BGREF}	Internal bandgap reference voltage	V_{DD} = 3 to 5.5 V	1.19(2)	1.22	1.25(2)	V
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
t_S(1)	Minimum sampling time	f_{ADC} = 4MHz	-	0.75	-	µs
		f_{ADC} = 6 MHz	-	0.5	-	
t_{STAB}	Wakeup time from standby	-	-	7	-	
t_{CONV}	Minimum total conversion time including sampling time, 10-bit resolution	f_{ADC} = 4 Hz	3.5			µs
		f_{ADC} = 6 MHz	2.33			
		-	14			$1/f_{ADC}$

1. During the sample time the input capacitance C_{AIN} (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.
2. Tested in production.

Table 55. ADC accuracy with RAIN < 10 kΩ, V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	2.2	4	
		f_{ADC} = 6 MHz	2.4	4.5	
$\|E_O\|$	Offset error(2)	f_{ADC} = 2 MHz	1.1	2.5	
		f_{ADC} = 4 MHz	1.5	3	
		f_{ADC} = 6 MHz	1.8	3	
$\|E_G\|$	Gain error(2)	f_{ADC} = 2 MHz	1.5	3	
		f_{ADC} = 4 MHz	2.1	3	
		f_{ADC} = 6 MHz	2.2	4	
$\|E_D\|$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	0.7	1.5	
		f_{ADC} = 6 MHz	0.7	1.5	
$\|E_L\|$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	
		f_{ADC} = 6 MHz	0.8	2	

1. Max value is based on characterization, not tested in production.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristics section does not affect the ADC accuracy.

Table 56. ADC accuracy with RAIN < 10 kΩ, V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	1.9	4	
$\|E_O\|$	Offset error	f_{ADC} = 2 MHz	1	2.5	
		f_{ADC} = 4 MHz	1.5	2.5	
$\|E_G\|$	Gain error	f_{ADC} = 2 MHz	1.3	3	
		f_{ADC} = 4 MHz	2	3	
$\|E_D\|$	Differential linearity error	f_{ADC} = 2 MHz	0.7	1	
		f_{ADC} = 4 MHz	0.7	1.5	
$\|E_L\|$	Integral linearity error	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	

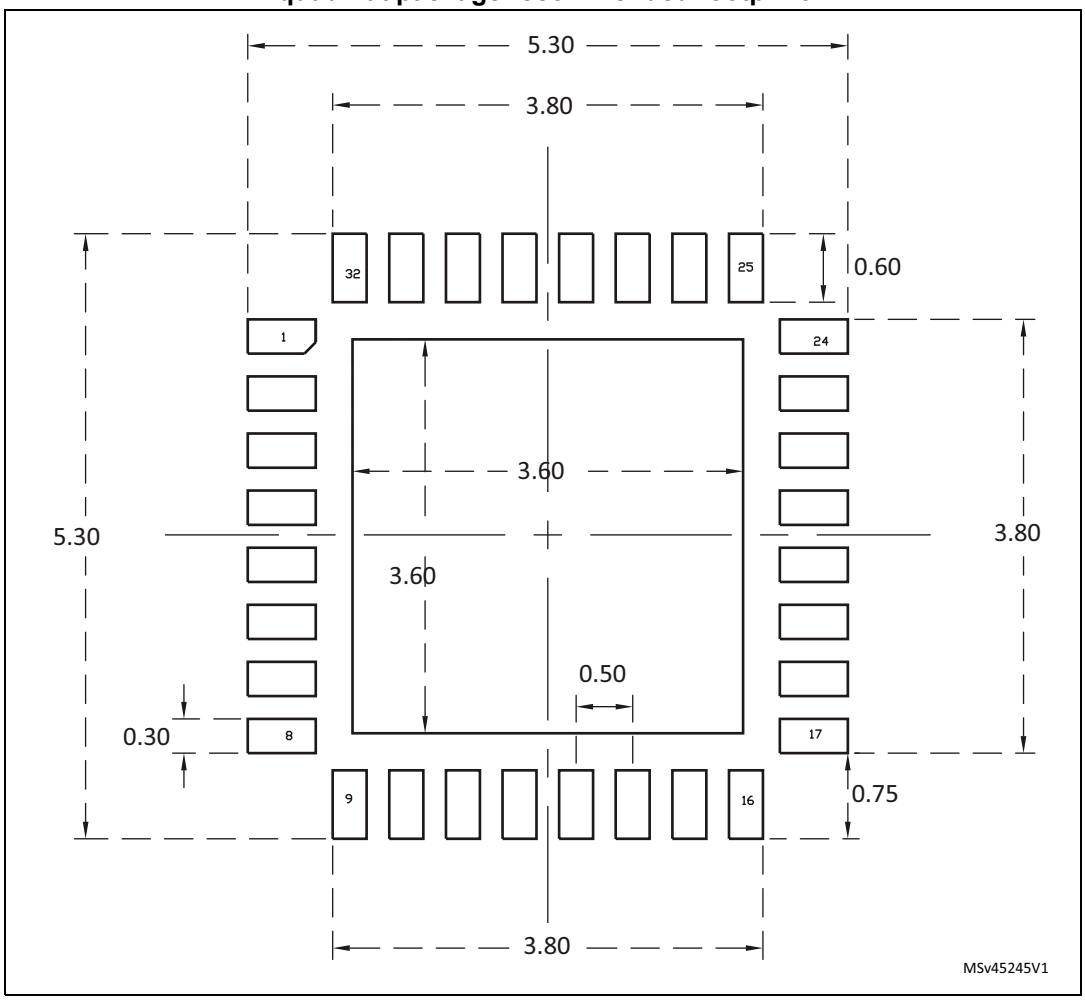
1. Max value is based on characterization, not tested in production.

Table 63. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.200	-	-	0.0079	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D2	3.500	3.600	3.700	0.1378	0.1417	0.1457
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E2	3.500	3.600	3.700	0.1378	0.1417	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 66. Document revision history (continued)

Date	Revision	Changes
10-Jul-2014	4	Extended the applicability to STM8AF6213 devices. Updated the program memory feature, the power management, and the clock management features on the cover page. Added the table in *Section: Memory map*. Updated the *Figure: f_{CPUmax} versus V_{DD}* in *Section: Operating conditions.* Updated *Section: Ordering information*.
26-Jun-2015	5	Added: – the footnote about the inrush current below *Table 27: Operating conditions at power-up/power-down*, – *Figure 44: LQFP32 marking example (package top view)*, – *Figure 47: TSSOP20 marking example (package top view)*. Updated – LIN standard version, – the register label for LINUART block in *Table 11: General hardware register map*, – the power dissipation in *Table 26: General operating conditions*, – *Table 41: HSI oscillator characteristics* for HSI oscillator accuracy, – the standard for EMI in *Electromagnetic interference (EMI)*, – *Figure 48: STM8AF6213/23/23A/26 ordering information scheme*(1) (2) to add HSI accuracy. Moved *Section 10.4: Thermal characteristics* to *Section 10: Package information*.
28-Mar-2017	6	Updated *Table 6: STM8AF6213/STM8AF6223 TSSOP20 pin description* Added VFQFPN32 (5x5 mm) package information updating: – *Section : Features* on the cover page: added VFQFPN32 (5x5 mm) figure – Added *Section 10.3: VFQFPN32 package information*: – Updated *Table 26: General operating conditions* – Updated *Table 64: Thermal characteristics* – Updated *Section 5.2: LQFP32/VFQPN32 pinout and pin description* – Updated *Section 11: Ordering information* Additional updates (not related to VFQFPN32): – Table footnotes on *Section 9: Electrical characteristics* – Updated *Section : Device marking on page 93*, *Section : Device marking on page 96* and *Section : Device marking on page 100* – *Section 9.2: Absolute maximum ratings*