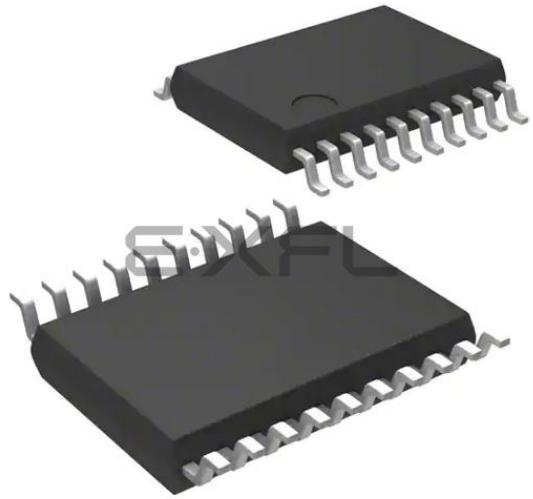

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6223pcu

4.13 Analog-to-digital converter (ADC1)

The STM8AF6213, STM8AF6223, STM8AF6223A and STM8AF6226 products contain a 10-bit successive approximation A/D converter (ADC1) with up to 7 external and 1 internal multiplexed input channels and the following main features:

- Input voltage range: 0 to V_{DD}
- Input voltage range: 0 to V_{DDA}
- Conversion time: 14 clock cycles
- Single and continuous and buffered continuous conversion modes
- Buffer size (n x 10 bits) where n = number of input channels
- Scan mode for single and continuous conversion of a sequence of channels
- Analog watchdog capability with programmable upper and lower thresholds
- Internal reference voltage on channel AIN7
- Analog watchdog interrupt
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

Note: Additional AIN12 analog input is not selectable in ADC scan mode or with analog watchdog. Values converted from AIN12 are stored only into the ADC_DRH/ADC_DRL registers.

Internal bandgap reference voltage

Channel AIN7 is internally connected to the internal bandgap reference voltage. The internal bandgap reference is constant and can be used, for example, to monitor V_{DD}. It is independent of variations in V_{DD} and ambient temperature T_A.

4.14 Communication interfaces

The following communication interfaces are implemented:

- LINUART: Full feature UART, synchronous mode, SPI master mode, Smartcard mode, IrDA mode, single wire mode, LIN2.2 capability
- SPI: full and half-duplex, 8 Mbit/s
- I²C: up to 400 Kbit/s

Some peripheral names differ between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016 (see *Table 4*).

Table 4. Communication peripheral naming correspondence

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
LINUART	UART4

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

4.14.2 Serial peripheral interface (SPI)

- Maximum speed: 8 Mbit/s (f_{MASTER}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave /master selection input pin

4.14.3 Inter integrated circuit (I^2C) interface

- I^2C master features:
  - Clock generation
  - Start and stop generation
- I^2C slave features:
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)

5 Pinout and pin description

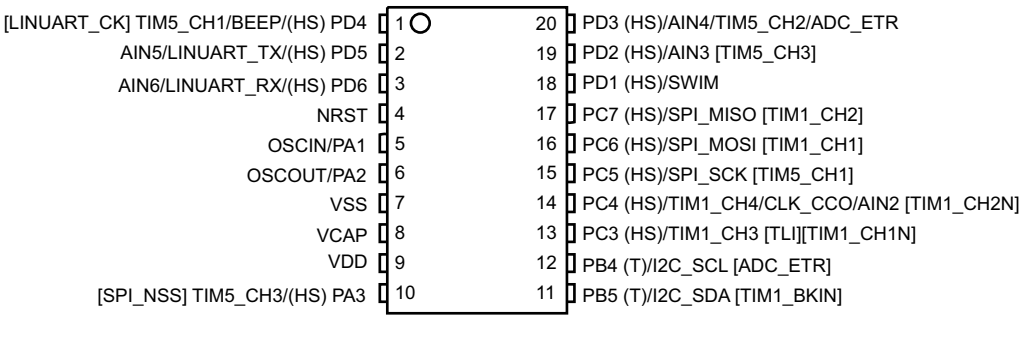
The following table presents the meaning of the abbreviations in use in the pin description tables in this section.

Table 5. Legend/abbreviations for pinout tables

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS (standard for all I/Os)
	Output	HS = High sink
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after internal reset release). Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release.	

5.1 TSSOP20 pinouts and pin descriptions

Figure 3. STM8AF6213/STM8AF6223 TSSOP20 pinout



1. (HS) high sink capability.
2. (T) true open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 6. STM8AF6213/STM8AF6223 TSSOP20 pin description (continued)

TSSOP	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
10	PA3/ TIM5_CH3 [SPI_NSS]	I/O	**X**	X	X	HS	O3	X	X	Port A3	Timer 5 channel 3	SPI master/ slave select [AFR1]
11	PB5/ I2C_SDA [TIM1_BKIN]	I/O	**X**	-	X	-	O1	T(3)	-	Port B5	I2C data	Timer 1 - break input [AFR4]
12	PB4/ I2C_SCL [ADC_ETR]	I/O	**X**	-	X	-	O1	T(3)	-	Port B4	I2C clock	ADC external trigger [AFR4]
13	PC3/ TIM1_CH3/[TLI]/[TIM1_CH1N]	I/O	**X**	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	Top level interrupt [AFR3] Timer 1 inverted channel 1 [AFR7]
14	PC4/ TIM1_CH4/ CLK_CCO/AIN2/[TIM1_CH2N]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4 /configurabl e clock output	Analog input 2 [AFR2]Time r 1 inverted channel 2 [AFR7]
15	PC5/SPI_SCK [TIM5_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 5 channel 1 [AFR0]
16	PC6/ SPI_MOSI [TIM1_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C6	PI master out/slave in	Timer 1 channel 1 [AFR0]
17	PC7/ SPI_MISO [TIM1_CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 channel 2[AFR0]
18	PD1/ SWIM(4)	I/O	**X**	X	X	HS	O4	X	X	Port D1	SWIM data interface	-

Table 8. STM8AF6226 LQFP32/VFQPN32 pin description (continued)

LQFP32 VFQPN32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
27	PD2/[AIN3] [TIM5_CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	-	Analog input 3 [AFR2] Timer 52 - channel 3 [AFR1]
28	PD3/ AIN4/ TIM5_CH2/ ADC_ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Analog input 4 Timer 52 - channel 2/ADC external trigger	-
29	PD4/ TIM5_CH1/ BEEP [LINUART_CK]	I/O	**X**	X	X	HS	O3	X	X	Port D4	Timer 5 - channel 1/BEEP output	LINUART clock [AFR2]
30	PD5/ AIN5/ LINUART_TX	I/O	**X**	X	X	HS	O3	X	X	Port D5	Analog input 5/ LINUART data transmit	-
31	PD6/ AIN6/ LINUART_RX	I/O	**X**	X	X	HS	O3	X	X	Port D6	Analog input 6/ LINUART data receive	-
32	PD7/ TLI [TIM1_CH4]	I/O	**X**	X	X	HS	O3	X	X	Port D7	Top level interrupt	Timer 1 - channel 4 [AFR6]

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 9.2: Absolute maximum ratings*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

5.3 Alternate function remapping

As shown in the rightmost column of *Table 6*, *Table 7* and *Table 8* some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 8: Option bytes on page 46*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016).

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	LINUART	UART4_SR	LINUART status register	0xC0
0x00 5231		UART4_DR	LINUART data register	0xXX
0x00 5232		UART4_BRR1	LINUART baud rate register 1	0x00
0x00 5233		UART4_BRR2	LINUART baud rate register 2	0x00
0x00 5234		UART4_CR1	LINUART control register 1	0x00
0x00 5235		UART4_CR2	LINUART control register 2	0x00
0x00 5236		UART4_CR3	LINUART control register 3	0x00
0x00 5237		UART4_CR4	LINUART control register 4	0x00
0x00 5238		Reserved		
0x00 5239		UART4_CR6	LINUART control register 6	0x00
0x00 523A		UART4_GTR	LINUART guard time register	0x00
0x00 523B		UART4_PSCR	LINUART prescaler	0x00
0x00 523C to 0x00 523F	Reserved area (20 byte)			

6.2.2 CPU/SWIM/debug module/interrupt controller registers

Table 12. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 byte)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)			

8 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 14: Option bytes* below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP and UBC options that can only be modified in ICP mode (via SWIM).

Refer to the STM8 Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 14. Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0x00
0x00 4801	User boot code (UBC)	OPT1	UBC[7:0]								0x00
0x00 4802		NOPT1	NUBC[7:0]								0xFF
0x00 4803	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	0x00
0x00 4804		NOPT2	NAFR7	NAFR6	NAFR 5	NAFR 4	NAFR 3	NAFR 2	NAFR 1	NAFR 0	0xFF
0x00 4805	Miscell. option	OPT3	Reserved			HSI TRIM	LSI _EN	IWDG _HW	WWDG _HW	WWDG _HALT	0x00
0x00 4806		NOPT3	Reserved			NHSI TRIM	NLSI _EN	NIWDG _HW	NWWDG _HW	NWWG _HALT	0xFF
0x00 4807	Clock option	OPT4	Reserved				EXT CLK	CKAWU SEL	PRS C1	PRS C0	0x00
0x00 4808		NOPT4	Reserved				NEXT CLK	NCKAWU SEL	NPRS C1	NPRS C0	0xFF
0x00 4809	HSE clock startup	OPT5	HSECNT[7:0]								0x00
0x00 480A		NOPT5	NHSECNT[7:0]								0xFF

Table 28. Total current consumption with code execution in run mode at V_{DD} = 5 V (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	4.5	-	mA
			HSE user ext. clock (16 MHz)	4.3	4.75	
			HSI RC osc. (16 MHz)	3.7	4.5(1)	
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	0.84	2(1)	
		$f_{CPU} = f_{MASTER}$/128 = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
		$f_{CPU} = f_{MASTER}$/128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

1. Tested in production.
2. Default clock configuration measured with all peripherals off.

Table 29. Total current consumption with code execution in run mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ =16 MHz	HSE crystal osc. (16 MHz)	1.8	-	mA
			HSE user ext. clock (16 MHz)	2	2.3	
			HSI RC osc. (16 MHz)	1.5	2	
		$f_{CPU} = f_{MASTER}$/128 = 125 kHz	HSE user ext. clock (16 MHz)	0.81	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}$/ 128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ =128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	4	-	
			HSE user ext. clock (16 MHz)	3.9	4.7	
			HSI RC osc. (16 MHz)	3.7	4.5	
		$f_{CPU} = f_{MASTER}$ =2 MHz	HSI RC osc. (16 MHz/8)(2)	0.84	1.05	
		$f_{CPU} = f_{MASTER}$/ 128 = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
		$f_{CPU} = f_{MASTER}$/128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ =128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Total current consumption in wait mode

Unless otherwise specified, data based are on characterization results, and not tested in production.

Table 30. Total current consumption in wait mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.6	-	mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.5(1)	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.45	0.57	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.4	0.54	

1. Tested in production.
2. Default clock configuration measured with all peripherals off.

Table 31. Total current consumption in wait mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.1	-	mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.1	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.45	0.57	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.4	0.54	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Total current consumption and timing in forced reset state

Table 37. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$I_{DD(R)}$	Supply current in reset state(2)	V_{DD}= 5 V	400	-	µA
		V_{DD}= 3.3 V	300	-	
$t_{RESETBL}$	Reset pin release to vector fetch	-	-	150	µs

1. Guaranteed by design.
2. Characterized with all I/Os tied to V_{SS}.

Current consumption for on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU} = f_{MASTER} = 16 MHz, V_{DD} = 5 V

Table 38. Peripheral current consumption

Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)	210	µA
$I_{DD(TIM5)}$	TIM5 supply current(1)	130	
$I_{DD(TIM6)}$	TIM6 supply current(1)	50	
$I_{DD(UART1)}$	LINUART supply current(2)	120	
$I_{DD(SPI)}$	SPI supply current(2)	45	
$I_{DD(I2C)}$	I2C supply current(2)	65	
$I_{DD(ADC1)}$	ADC1 supply current(3)	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions. Not tested in production.

Figure 13. Typ $I_{DD(RUN)}$ vs. V_{DD} HSEI RC osc., f_{CPU} = 16 MHz

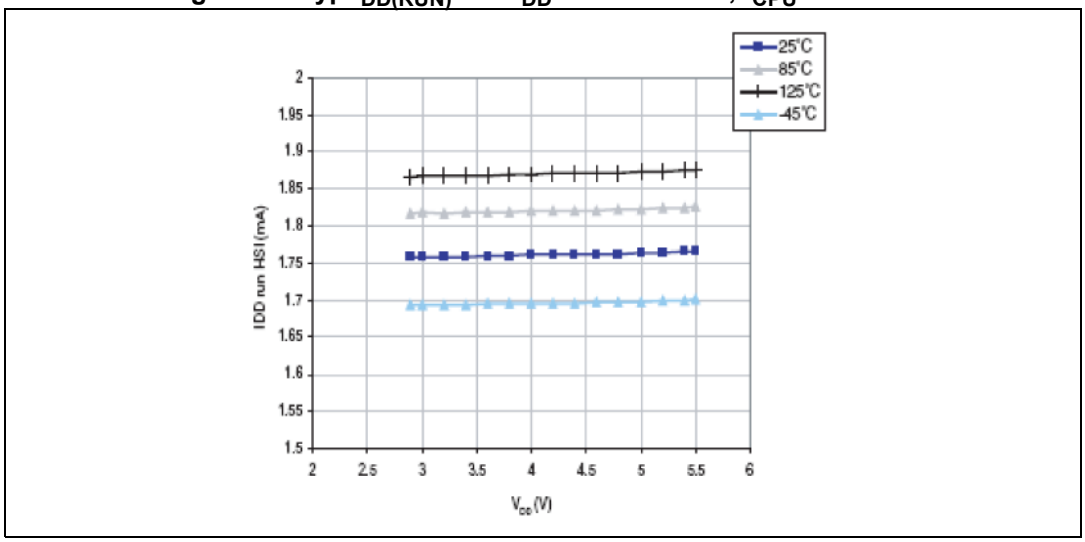


Figure 14. Typ $I_{DD(WFI)}$ vs. V_{DD} HSE user external clock, f_{CPU} = 16 MHz

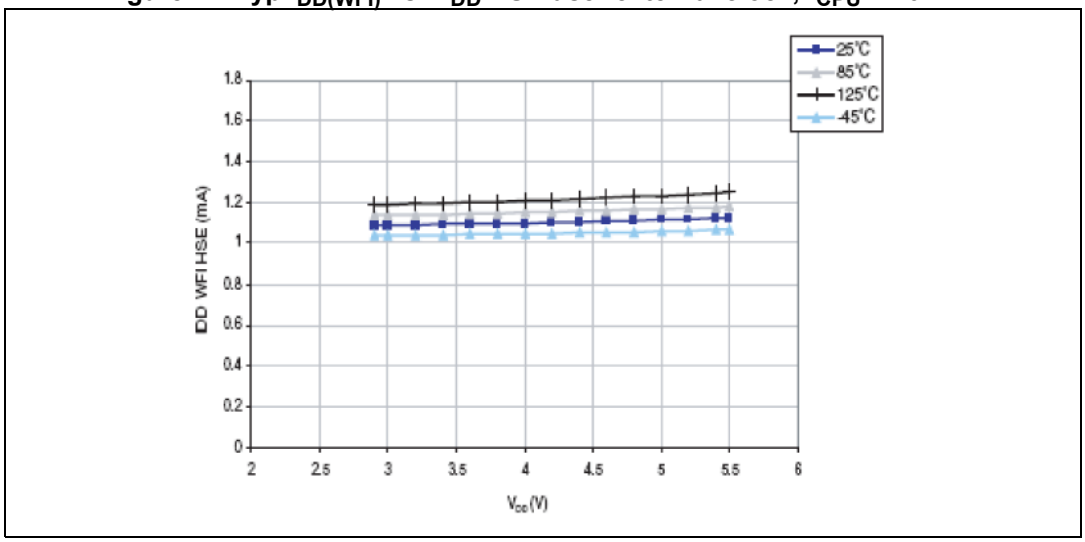


Figure 19. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

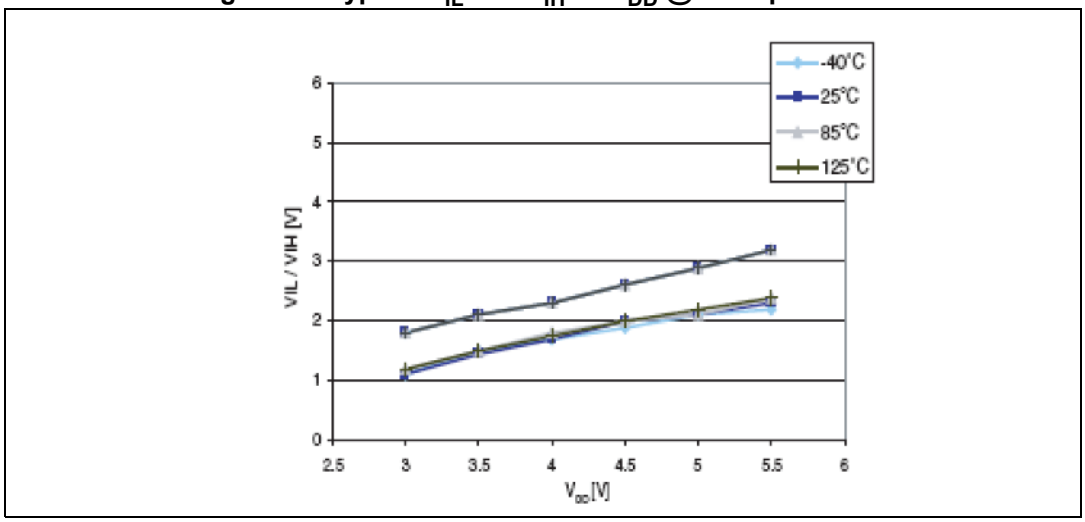
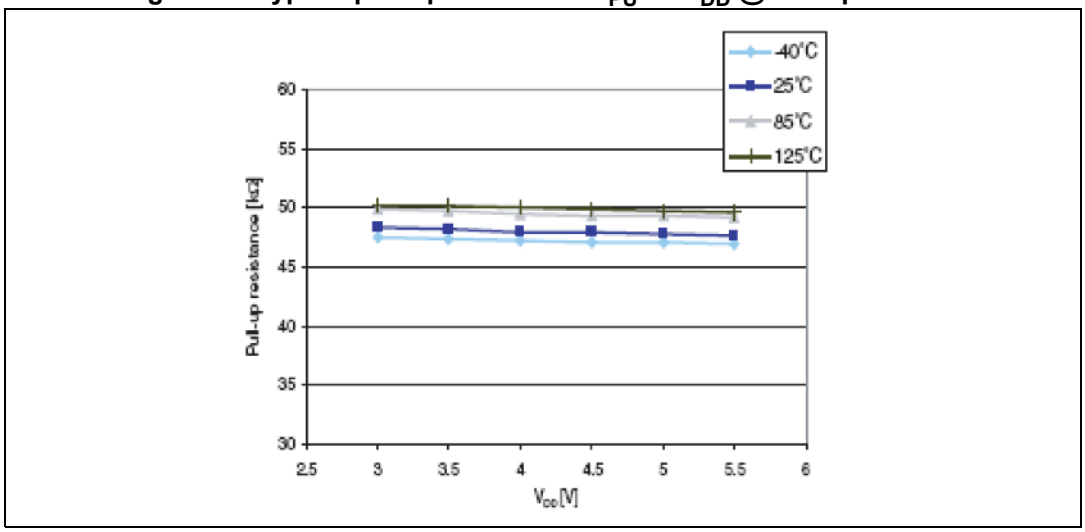


Figure 20. Typical pull-up resistance R_{PU} vs V_{DD} @ 4 temperatures



9.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 51. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	-0.3	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	I_{OL}= 2 mA	0.7 x V_{DD}	-	V_{DD} + 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	-	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)	-	30	55	80	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse duration(3)	-	500	-	-	
$t_{OP(NRST)}$	NRST output pulse(3)	-	20	-	-	µs

1. Guaranteed by characterization results.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
3. Guaranteed by design.

Figure 32. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

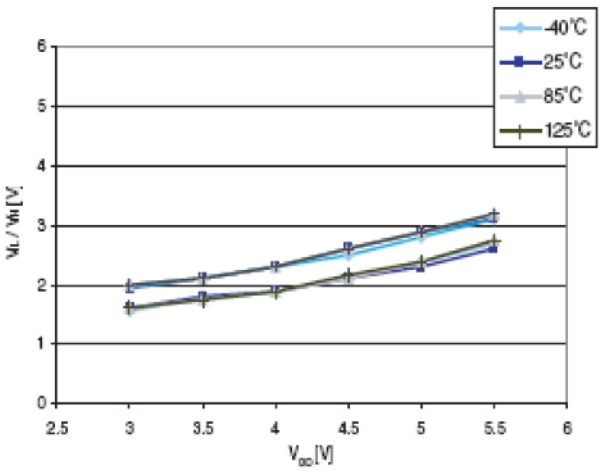
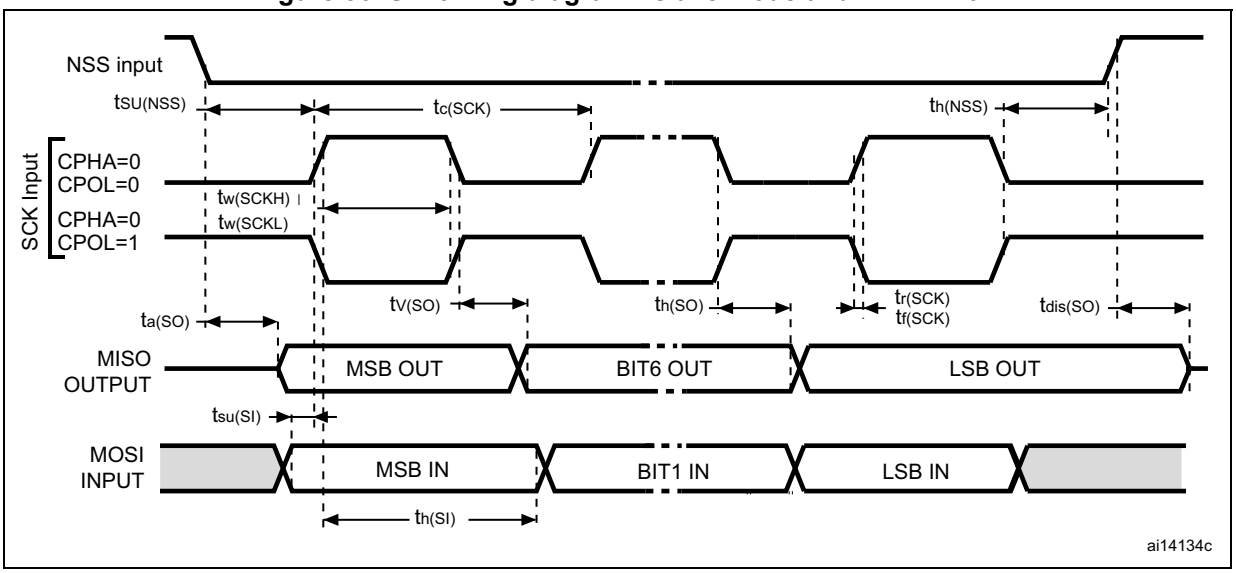


Table 52. SPI characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Max	Unit
$t_{h(SO)}$[2]	Data output hold time	Slave mode (after enable edge)	27	-	ns
$t_{h(MO)}$[2]		Master mode (after enable edge)	11	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 36. SPI timing diagram - slave mode and CPHA = 0



1. Measurement points are made at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

Table 58. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f_{HSE}/f_{CPU}(1)		
				16 MHz/ 8 MHz	16 MHz/ 16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP32 package conforming to IEC 61967-2	0.1 MHz to 30 MHz	5	5	dBµV
			30 MHz to 130 MHz	4	5	
			130 MHz to 1 GHz	5	5	
	EMI level		—	2.5	2.5	level

1. Guaranteed by characterization results.

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

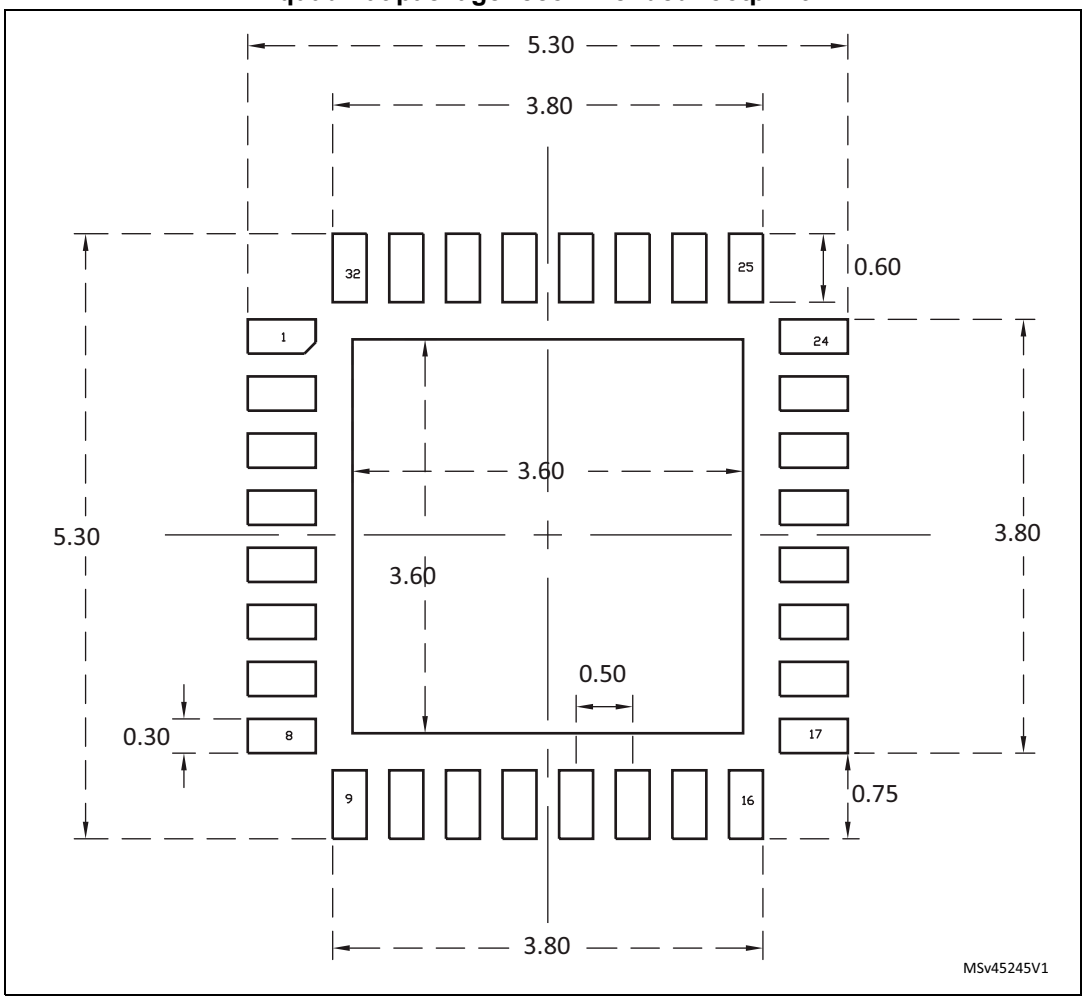
Electrostatic discharges (one positive then one negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 59. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine model)	T_A= 25°C, conforming to JESD22-A115	B	200	

1. Guaranteed by characterization results.

Figure 49. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax}= 75 °C (measured according to JESD51-2), I_{DDmax} = 8 mA, V_{DD} = 5 V

Maximum 20 I/Os used at the same time in output at low level with:
I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 8 mA x 5 V= 400 mW

P_{IOmax} = 20 x 8 mA x 0.4 V = 64 mW

This gives: P_{INTmax} = 400 mW and P_{IOmax} 64 mW:

P_{Dmax} = 400 mW + 64 mW

Thus: P_{Dmax} = 464 mW.

Using the values obtained in *Table 64: Thermal characteristics on page 101* T_{Jmax} is calculated as follows:

For LQFP32 60 °C/W

T_{Jmax} = 75 °C + (60 °C/W x464 mW) = 75 °C + 27.8 °C = 102.8 °C

This is within the range of the suffix C version parts (-40 < T_J < 125 °C).

Parts must be ordered at least with the temperature range suffix C.

13 Revision history

Table 66. Document revision history

Date	Revision	Changes
11-Oct-2013	1	Initial release.
16-Dec-2013	2	Changed the document status to Production data. Updated *Figure: STM8AF6223PxAx TSSOP20 pinout* to add SPI_NSS to PD4, TLI to PD2, and change remap function on PB5 from TIM5_BKIn to TIM1_BKIN. Updated *Table: STM8AF6223PxAx TSSOP20 pin description* to add SPI_NSS to PD4 and TLI to PD2. Updated *Table: STM8AF6223 TSSOP20 pin description* and *Table: LQFP32 pin descriptio*n. Updated AFR2 definition in *Table: STM8AF6223PxAx alternate function remapping bits [7:2] for 20-pin packages*. Removed the remapping option on PA3 for AFR[1:0]=10 in *Table: STM8AF6223PxAx alternate function remapping bits [1:0] for 20-pin packages*. Added note and removed remapping option on PA3 for AFR[1:0]=11 in *Table: STM8AF6223 alternate function remapping bits [1:0] for 20-pin packages*. Updated AFR2 definition in STM8AF6223 alternate function remapping bits [7:2] for 20-pin packages. Added the note below *Table: STM8AF6226T alternate function remapping bits [1:0] for 32-pin packages*. Updated *Table: I2C characteristics* to modify $t_{h(SDA)}$ and add t_{SP}. Updated *Section: C assembly toolchains*.
03-Apr-2014	3	Replaced STM8AF6226T by STM8AF6226 part number. Added STM8AF6223A part number to cover STM8AF6223PxAx order codes. Removed LINUART alternate function for PA3 in *Table: STM8AF6223PxAx TSSOP20 pin description*. Removed note 3 for $I_{DD(AH)}$ in *Table: Total current consumption in active halt mode at VDD = 5 V*. Updated the remapping option on PA3 for AFR[1:0]=11 in *Table: STM8AF6223 alternate function remapping bits [1:0] for 20-pin packages*. Updated notes related to t_{RET} minimum value in *Table: Data memory*. Updated *Table: ESD absolute maximum ratings*. Added notes related to protrusions and gate burrs for D and E1 dimensions in *Table: 20-pin, 4.40 mm body, 0.65 mm pitch mechanical data*.