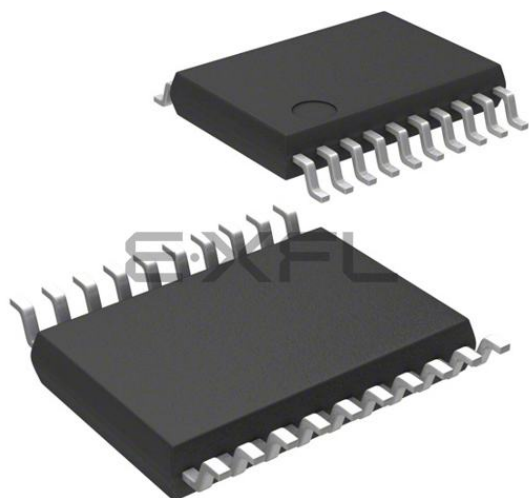




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Details

Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6223pcx

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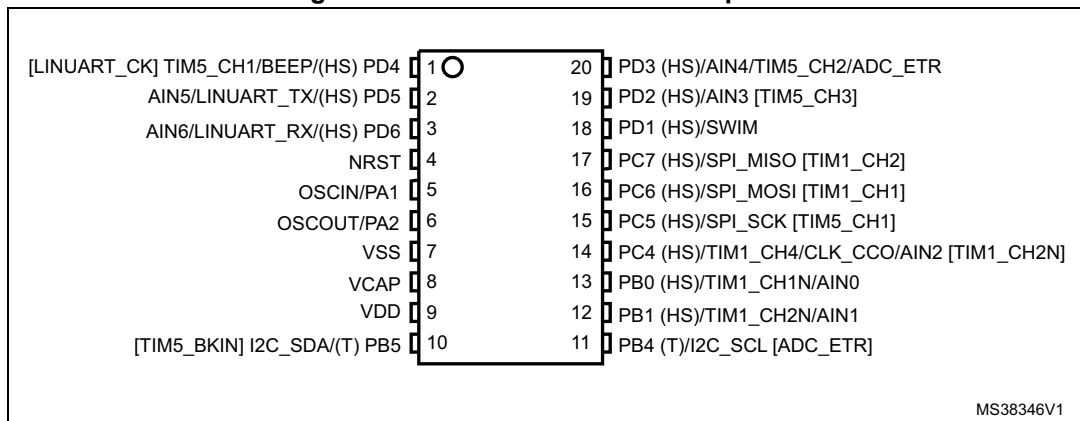
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1 Introduction

The datasheet contains the description of STM8AF6213, STM8AF6223, STM8AF6223A and STM8AF6226 features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8 Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

Figure 4. STM8AF6223A TSSOP20 pinout



1. (HS) high sink capability.
2. (T) true open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 6. STM8AF6213/STM8AF6223 TSSOP20 pin description

TSSOP	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink ⁽¹⁾	Speed	OD	PP			
1	PD4/ TIM5_CH1/ BEEP [LINUART_CK]	I/O	X	X	X	HS	O3	X	X	Port D4	Timer 5 - channel 1/BEEP output	LINUART clock [AFR2]
2	PD5/ AIN5/ LINUART_TX	I/O	X	X	X	HS	O3	X	X	Port D5	Analog input 5/ LINUART data transmit	-
3	PD6/ AIN6/ LINUART_RX	I/O	X	X	X	HS	O3	X	X	Port D6	Analog input 6/ LINUART data receive	-
4	NRST	I/O	-	X	-	-	-	-	-	Reset		
5	PA1/ OSCIN ⁽²⁾	I/O	X	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
6	PA2/ OSCOUT	I/O	X	X	X	O1	X	X		Port A2	Resonator/ crystal out	-
7	VSS	S	-	-	-	-	-	-	-	Digital ground		
8	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		
9	VDD	S	-	-	-	-	-	-	-	Digital power supply		

Table 7. STM8AF6223A TSSOP20 pin description (continued)

TSSOP	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink ⁽¹⁾	Speed	OD	PP			
3	PD6/ AIN6/ LINUART_RX	I/O	X	X	X	HS	O3	X	X	Port D6	Analog input 6/ LINUART data receive	-
4	NRST	I/O	-	X	-	-	-	-	-	Reset		-
5	PA1/ OSCIN ⁽²⁾	I/O	X	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
6	PA2/ OSCOUT	I/O	X	X	X	-	O1	X	X	Port A2	Resonator/ crystal out	-
7	VSS	S	-	-	-	-	-	-	-	Digital ground		-
8	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
9	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
10	PB5/ I2C_SDA [TIM1_BKIN]	I/O	X	-	X	-	O1	T ⁽³⁾	-	Port B5	I2C data	Timer 1 - break input [AFR4]
11	PB4/ I2C_SCL [ADC_ETR]	I/O	X	-	X	-	O1	T ⁽³⁾	-	Port B4	I2C clock	ADC external trigger [AFR4]
12	PB1/ TIM1_CH2N/ AIN1	I/O	X	X	X	HS	O3	X	X	Port B1	Timer 1 - inverted channel 2/Analog input 1	-
13	PB0/ TIM1_CH1N/AIN0	I/O	X	X	X	HS	O3	X	X	Port B0	Timer 1 - inverted channel 1/Analog input 0	-
14	PC4/ TIM1_CH4/ CLK_CCO/AIN2/[TIM1_CH2]	I/O	X	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4 /configurable clock output	Analog input 2 [AFR2]Timer 1 channel 2 [AFR7]
15	PC5/SPI_SCK [TIM5_CH1]	I/O	X	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 5 channel 1 [AFR0]

Table 9. Memory model for the devices covered in this datasheet

Flash program memory size	Flash program memory end address	RAM size	RAM end address	Stack roll-over address
8 K	0x00 9FFF	1 K	0x00 03FF	0x00 0200
4 K	0x00 8FFF			

6.2 Register map

6.2.1 I/O port hardware register map

Table 10. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX ⁽¹⁾
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX ⁽¹⁾
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xXX ⁽¹⁾
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX ⁽¹⁾
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

6.2.2 CPU/SWIM/debug module/interrupt controller registers

Table 12. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU ⁽¹⁾	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 byte)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)			

Table 12. CPU/SWIM/debug module/interrupt controller registers (continued)

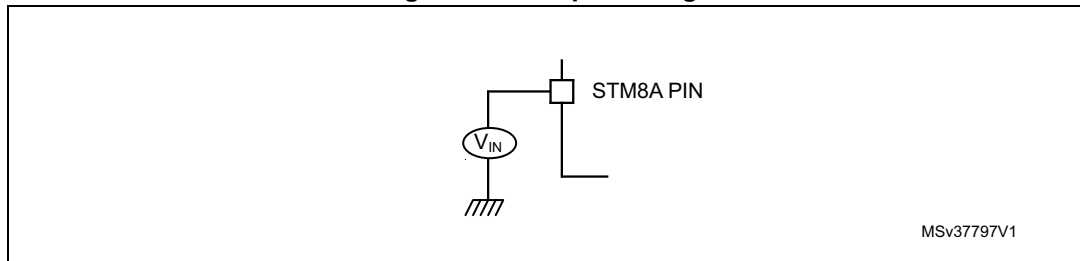
Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 byte)			

1. Accessible by debug module only

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 8](#).

Figure 8. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 22: Voltage characteristics](#), [Table 23: Current characteristics](#) and [Table 24: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 22. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V _{DDx} - V _{SS}	Supply voltage (including V _{DDA} and V _{DDIO}) ⁽¹⁾	-0.3	6.5	V
V _{IN}	Input voltage on true open drain pins ⁽²⁾	V _{SS} - 0.3	6.5	V
	Input voltage on any other pin ⁽²⁾	V _{SS} - 0.3	V _{DD} + 0.3	
V _{DDx} - V _{DD}	Variations between different power pins	-	50	mV
V _{SSx} - V _{SS}	Variations between all the different ground pins	-	50	
V _{ESD}	Electrostatic discharge voltage	see <i>Absolute maximum ratings (electrical sensitivity) on page 89</i>		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Total current consumption in halt mode

Table 34. Total current consumption in halt mode at $V_{DD} = 5\text{ V}$

Symbol	Parameter	Conditions	Typ	Max at 85°C	Max at 125°C	Max at 150°C	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	63	75	105	-	μA
		Flash in power-down mode, HSI clock after wakeup	6.0	20 ⁽¹⁾	55 ⁽¹⁾	80 ⁽¹⁾	

1. Tested in production.

Table 35. Total current consumption in halt mode at $V_{DD} = 3.3\text{ V}$

Symbol	Parameter	Conditions	Typ	Max at 85°C ⁽¹⁾	Max at 125°C ⁽¹⁾	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	60	75	100	μA
		Flash in power-down mode, HSI clock after wakeup	4.5	17	30	

1. Guaranteed by characterization results.

Low-power mode wakeup times

Table 36. Wakeup times

Symbol	Parameter	Conditions			Typ	Max ⁽¹⁾	Unit
t _{WU(WFI)}	Wakeup time from wait mode to run mode ⁽²⁾	0 to 16 MHz			-	See ⁽³⁾	μs
		f _{CPU} = f _{MASTER} = 16 MHz			0.56	-	
t _{WU(AH)}	Wakeup time active halt mode to run mode ⁽²⁾	MVR voltage regulator on ⁽⁴⁾	Flash in operating mode ⁽⁵⁾	HSI (after wakeup)	1 ⁽⁶⁾	2 ⁽⁶⁾	
					3 ⁽⁶⁾	-	
		MVR voltage regulator off			48 ⁽⁶⁾	-	
					50 ⁽⁶⁾	-	
t _{WU(H)}	Wakeup time from halt mode to run mode ⁽²⁾	Flash in operating mode ⁽⁵⁾			52	-	
		Flash in power-down mode ⁽⁵⁾			54	-	

1. Guaranteed by design.

2. Measured from interrupt event to interrupt vector fetch.

3. $t_{WU(WFI)} = 2 \times 1/f_{MASTER} + 67 \times 1/f_{CPU}$.

4. Configured by the REGAH bit in the CLK_ICR register.

5. Configured by the AHALT bit in the FLASH_CR1 register.

6. Plus 1 LSI clock depending on synchronization.

Total current consumption and timing in forced reset state**Table 37. Total current consumption and timing in forced reset state**

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾	Unit
$I_{DD(R)}$	Supply current in reset state ⁽²⁾	$V_{DD} = 5\text{ V}$	400	-	μA
		$V_{DD} = 3.3\text{ V}$	300	-	
t_{RESETBL}	Reset pin release to vector fetch	-	-	150	μs

1. Guaranteed by design.

2. Characterized with all I/Os tied to V_{SS} .

Current consumption for on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A .

HSI internal $RC/f_{\text{CPU}} = f_{\text{MASTER}} = 16\text{ MHz}$, $V_{DD} = 5\text{ V}$

Table 38. Peripheral current consumption

Symbol	Parameter	Typ	Unit
$I_{DD(\text{TIM1})}$	TIM1 supply current ⁽¹⁾	210	μA
$I_{DD(\text{TIM5})}$	TIM5 supply current ⁽¹⁾	130	
$I_{DD(\text{TIM6})}$	TIM6 supply current ⁽¹⁾	50	
$I_{DD(\text{UART1})}$	LINUART supply current ⁽²⁾	120	
$I_{DD(\text{SPI})}$	SPI supply current ⁽²⁾	45	
$I_{DD(\text{I2C})}$	I2C supply current ⁽²⁾	65	
$I_{DD(\text{ADC1})}$	ADC1 supply current ⁽³⁾	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.

2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.

3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions. Not tested in production.

9.3.3 External clock sources and timing characteristics

HSE user external clock

Subject to general operating conditions for V_{DD} and T_A .

Table 39. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	-	16	MHz
$V_{HSEH}^{(1)}$	OSCIN input pin high level voltage	-	$0.7 \times V_{DD}$	-	$V_{DD} + 0.3 V$	V
$V_{HSEL}^{(1)}$	OSCIN input pin low level voltage	-	V_{SS}	-	$0.3 \times V_{DD}$	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	-	+1	μA

1. Guaranteed by characterization results.

Figure 17. HSE external clock source

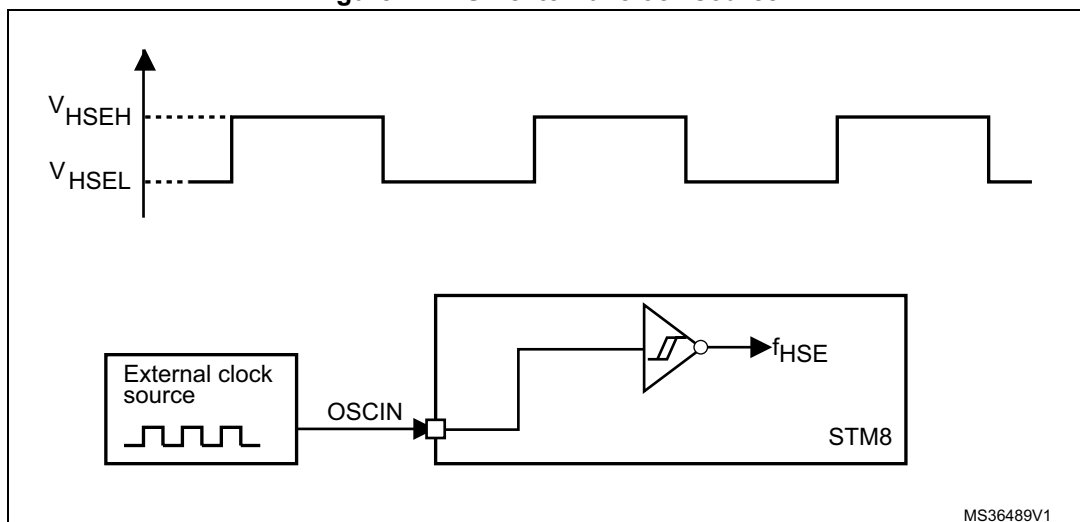


Table 45. Flash program memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Flash program memory endurance (erase/write cycles) ⁽¹⁾	$T_A = 25\text{ °C}$	1000	-	cycles
t_{RET}	Data retention time	$T_A = 25\text{ °C}$	40	-	years
		$T_A = 55\text{ °C}$	20	-	

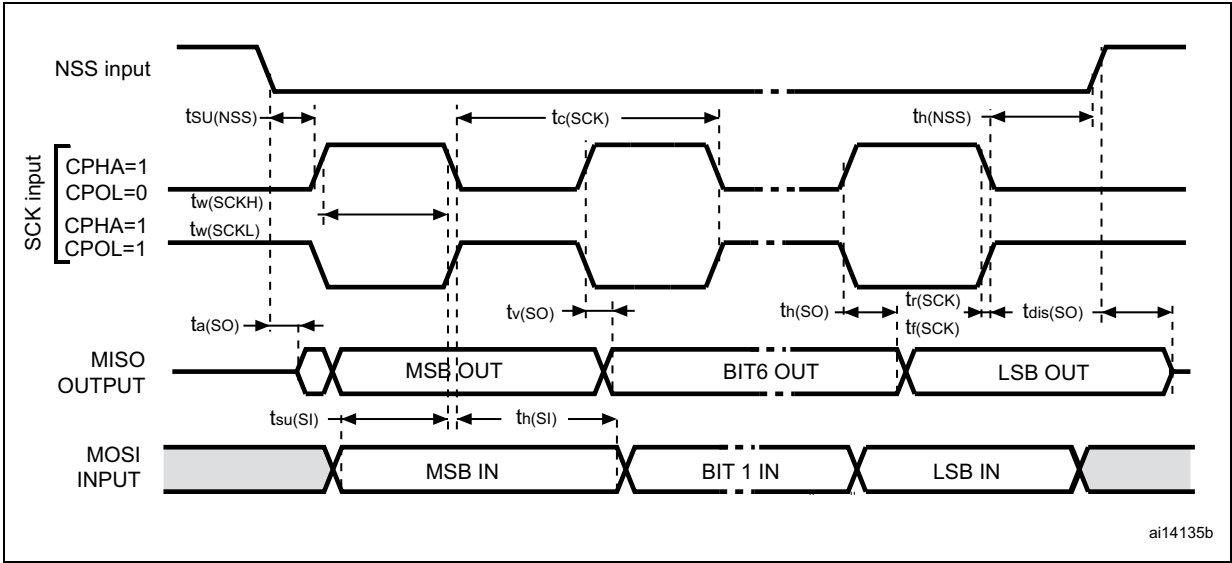
1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.

Table 46. Data memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Data memory endurance ⁽¹⁾ (erase/write cycles)	$T_A = 25\text{ °C}$	300 k	-	cycles
		$T_A = -40\text{ °C to }125\text{ °C}$	100 k ⁽²⁾	-	
t_{RET}	Data retention time	$T_A = 25\text{ °C}$	40 ⁽³⁾	-	years
		$T_A = 55\text{ °C}$	20 ⁽²⁾⁽³⁾	-	

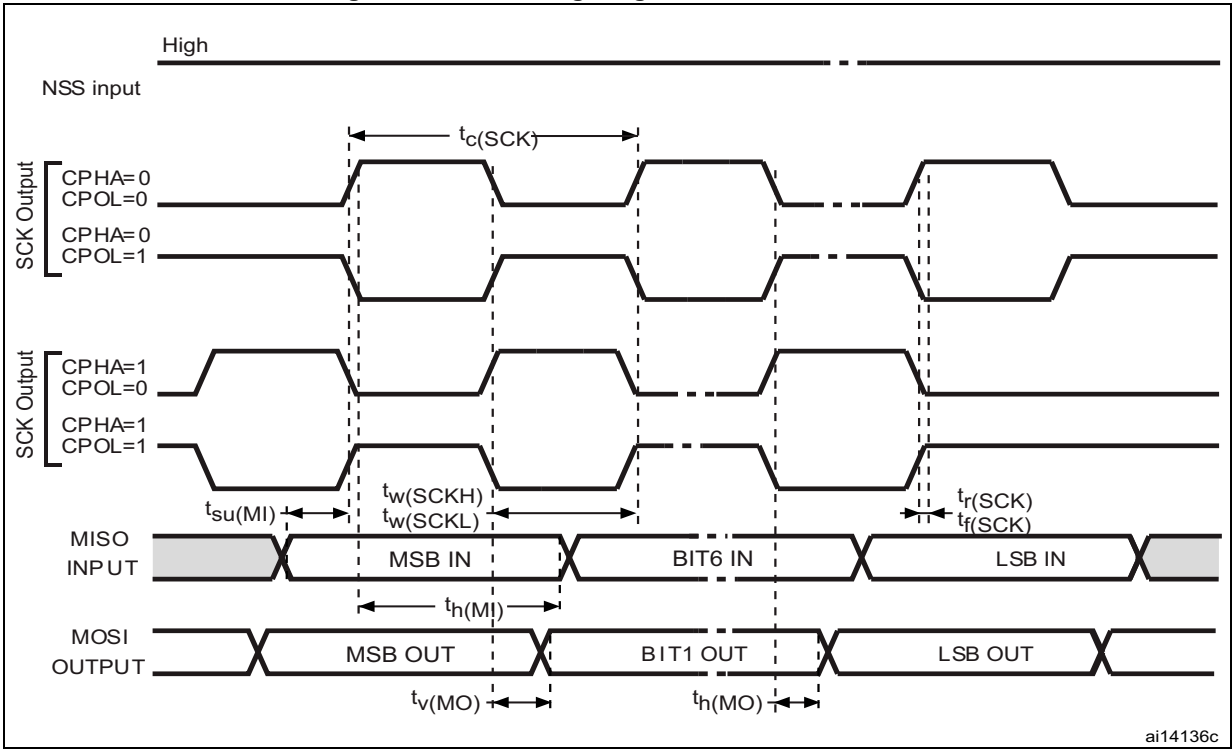
1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

Figure 37. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD} .

Figure 38. SPI timing diagram - master mode⁽¹⁾



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD} .

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

Table 58. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f _{HSE} /f _{CPU} ⁽¹⁾		
				16 MHz/ 8 MHz	16 MHz/ 16 MHz	
S _{EMI}	Peak level	V _{DD} = 5 V, T _A = 25 °C, LQFP32 package conforming to IEC 61967-2	0.1 MHz to 30 MHz	5	5	dBμV
			30 MHz to 130 MHz	4	5	
			130 MHz to 1 GHz	5	5	
	EMI level	—	2.5	2.5	level	

1. Guaranteed by characterization results.

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

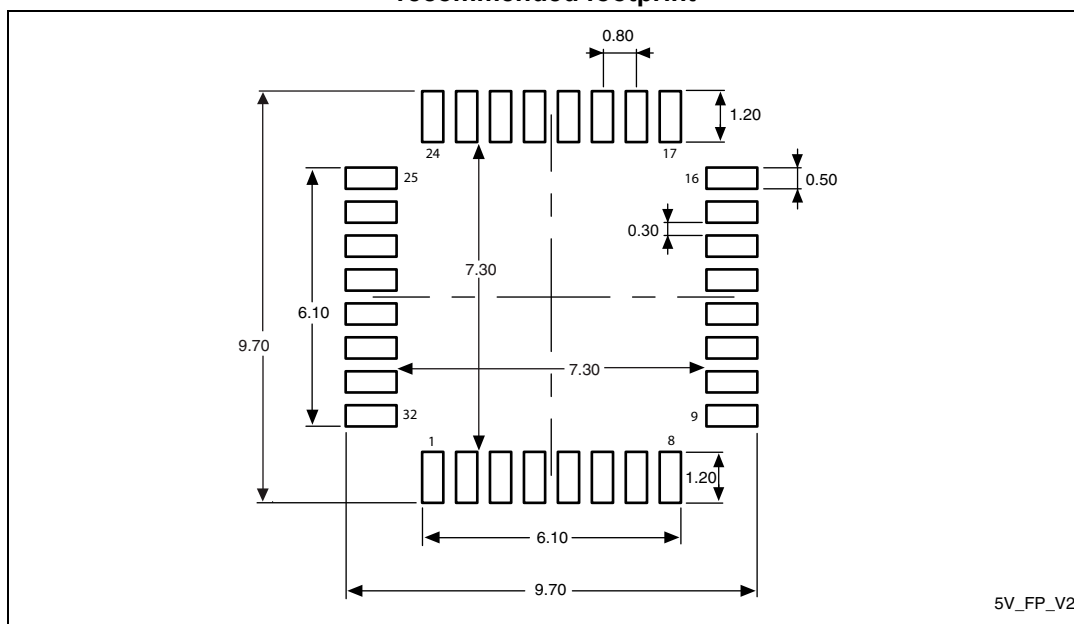
Electrostatic discharges (one positive then one negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 59. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	$T_A = 25\text{ }^{\circ}\text{C}$, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	$T_A = 25\text{ }^{\circ}\text{C}$, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine model)	$T_A = 25\text{ }^{\circ}\text{C}$, conforming to JESD22-A115	B	200	

1. Guaranteed by characterization results.

Figure 43. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint

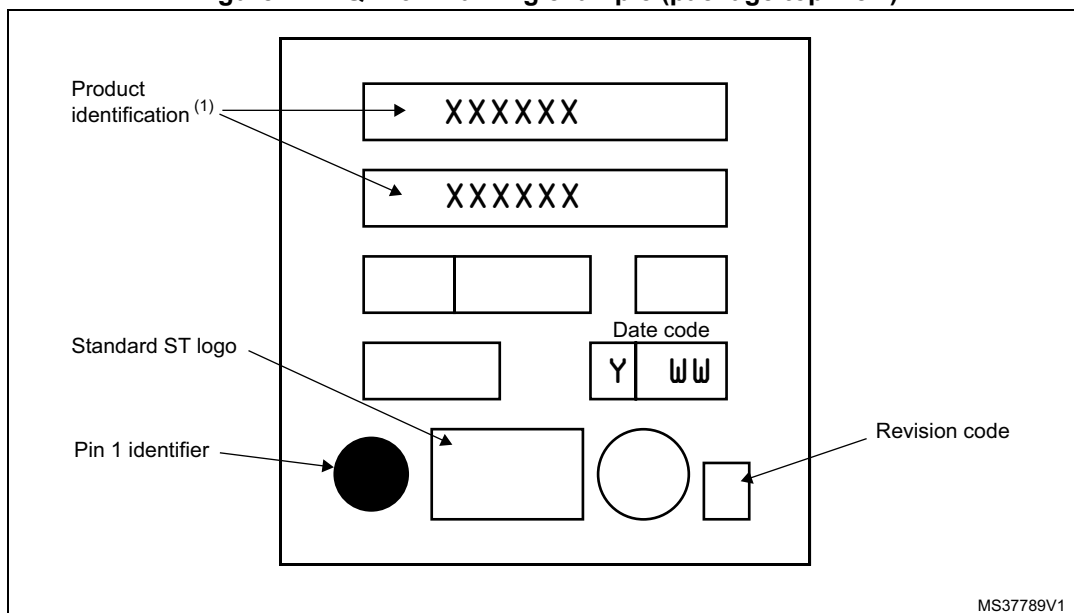


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

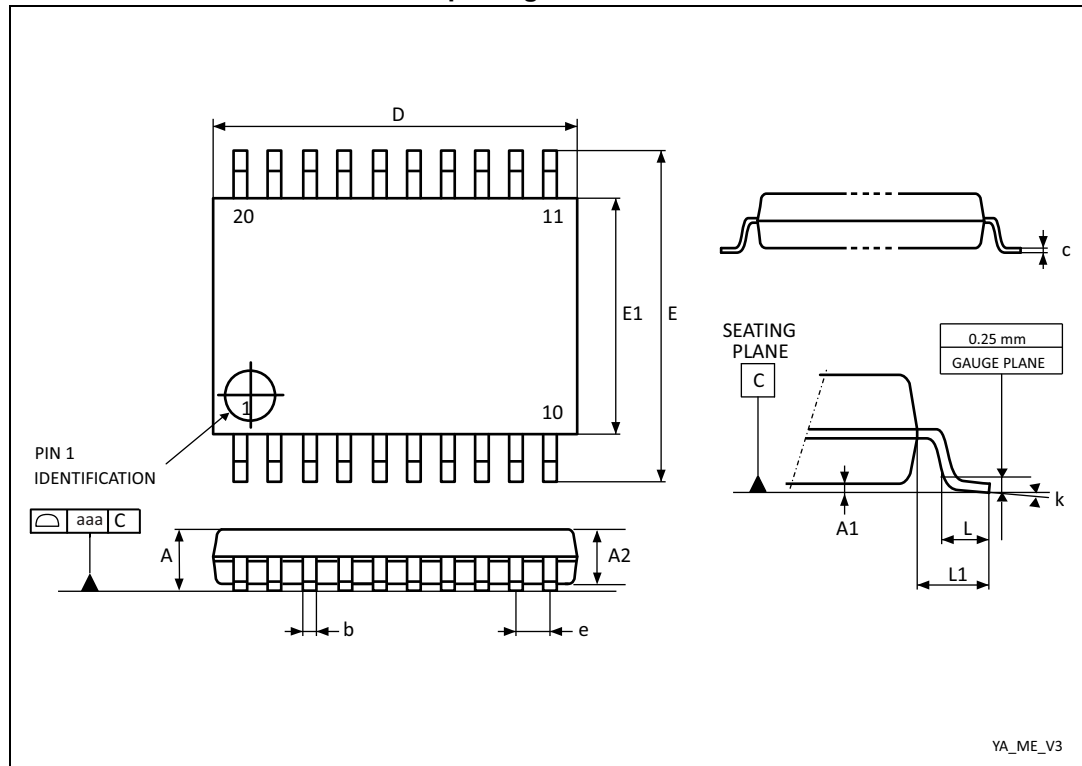
Figure 44. LQFP32 marking example (package top view)



1. Parts marked as "ES" or "E" are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

10.2 TSSOP20 package information

Figure 45. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package outline



1. Drawing is not to scale.

Table 62. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D ⁽²⁾	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1 ⁽³⁾	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

Table 63. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.200	-	-	0.0079	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D2	3.500	3.600	3.700	0.1378	0.1417	0.1457
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E2	3.500	3.600	3.700	0.1378	0.1417	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

10.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 26: General operating conditions](#).

T_{Jmax} , in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

- $P_{I/Omax}$ represents the maximum power dissipation on output pins

Where:

$$P_{I/Omax} = \Sigma (V_{OL} \cdot I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \cdot I_{OH}),$$

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 64. Thermal characteristics⁽¹⁾

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient TSSOP20 - 4 x 4 mm	110	°C/W
	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	60	
	Thermal resistance junction-ambient VFQFPN32 - 5 x 5 mm	TBD	

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

10.4.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

10.4.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see [Section 11: Ordering information](#)).

The following example shows how to calculate the temperature range needed for a given application.

12.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the user application board via the SWIM protocol. Additional tools include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.