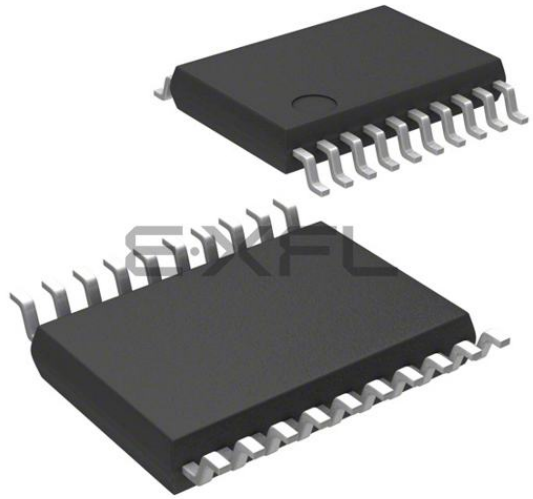

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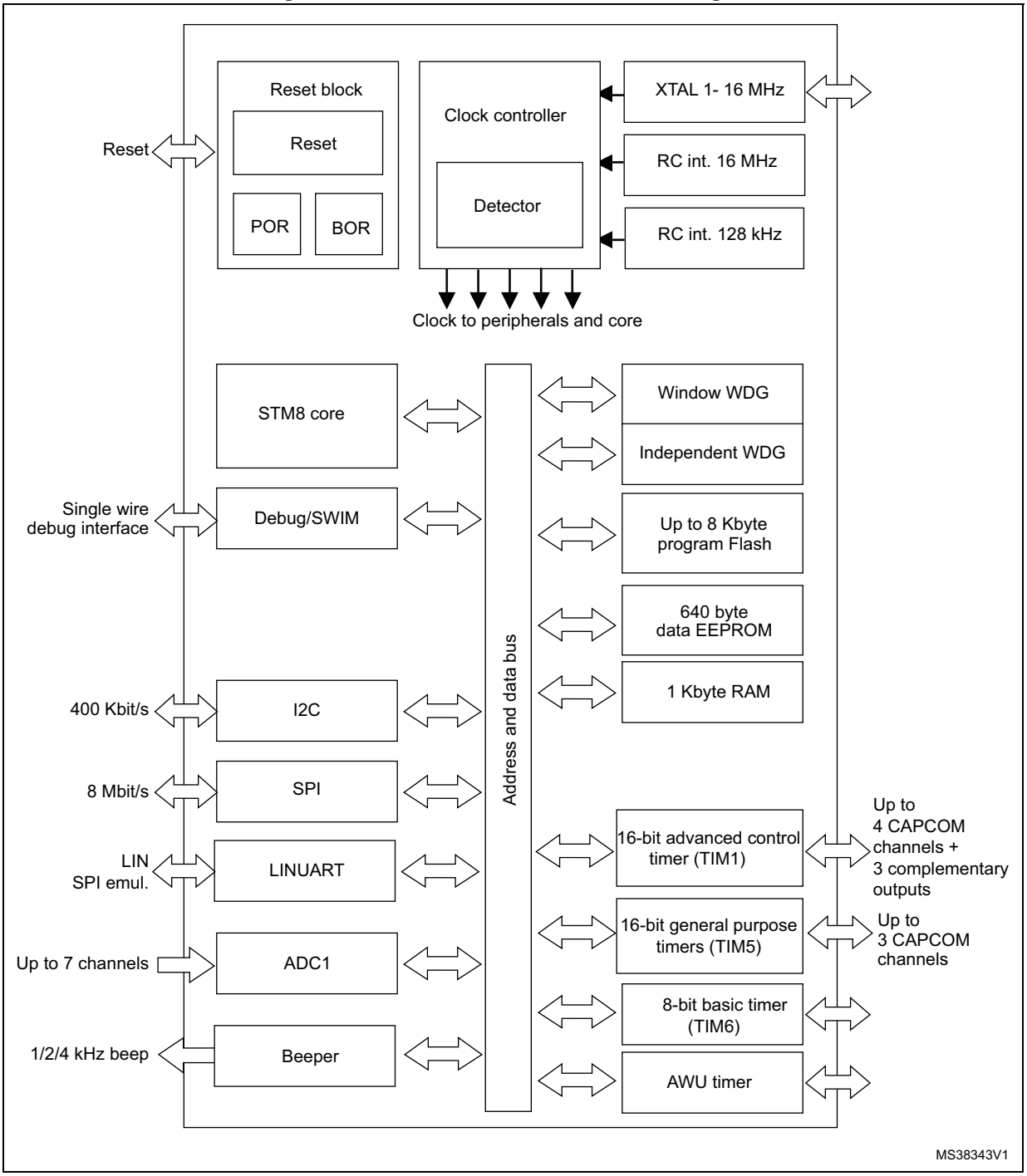
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6223pdax

3 Block diagram

Figure 1. STM8AF6213/23/23A/26 block diagram



1. **Legend:** ADC (Analog-to-digital converter), beCAN (Controller area network), BOR (Brownout reset), I²C (Inter-integrated circuit multimaster interface),IWDG (Independent window watchdog), LINUART (Local interconnect network universal asynchronous receiver transmitter), POR (Power on reset), SPI (Serial peripheral interface), SWIM (Single wire interface module), USART (Universal synchronous asynchronous receiver transmitter), Window WDG (Window watchdog).

4.13 Analog-to-digital converter (ADC1)

The STM8AF6213, STM8AF6223, STM8AF6223A and STM8AF6226 products contain a 10-bit successive approximation A/D converter (ADC1) with up to 7 external and 1 internal multiplexed input channels and the following main features:

- Input voltage range: 0 to V_{DD}
- Input voltage range: 0 to V_{DDA}
- Conversion time: 14 clock cycles
- Single and continuous and buffered continuous conversion modes
- Buffer size (n x 10 bits) where n = number of input channels
- Scan mode for single and continuous conversion of a sequence of channels
- Analog watchdog capability with programmable upper and lower thresholds
- Internal reference voltage on channel AIN7
- Analog watchdog interrupt
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

Note: Additional AIN12 analog input is not selectable in ADC scan mode or with analog watchdog. Values converted from AIN12 are stored only into the ADC_DRH/ADC_DRL registers.

Internal bandgap reference voltage

Channel AIN7 is internally connected to the internal bandgap reference voltage. The internal bandgap reference is constant and can be used, for example, to monitor V_{DD}. It is independent of variations in V_{DD} and ambient temperature T_A.

4.14 Communication interfaces

The following communication interfaces are implemented:

- LINUART: Full feature UART, synchronous mode, SPI master mode, Smartcard mode, IrDA mode, single wire mode, LIN2.2 capability
- SPI: full and half-duplex, 8 Mbit/s
- I²C: up to 400 Kbit/s

Some peripheral names differ between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016 (see *Table 4*).

Table 4. Communication peripheral naming correspondence

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
LINUART	UART4

4.14.1 LINUART

Main features

- 1 Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN mode
- Single wire half duplex mode

LIN mode

Master mode:

- LIN break and delimiter generation
- LIN break and delimiter detection with separate flag and interrupt source for read back checking.

Slave mode:

- Autonomous header handling – one single interrupt per valid header
- Mute mode to filter responses
- Identifier parity error checking
- LIN automatic resynchronization, allowing operation with internal RC oscillator (HSI) clock source
- Break detection at any time, even during a byte reception
- Header errors detection:
  - Delimiter too short
  - Synch field error
  - Deviation error (if automatic resynchronization is enabled)
  - Framing error in synch field or identifier field
  - Header time-out

Table 7. STM8AF6223A TSSOP20 pin description (continued)

TSSOP	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
3	PD6/ AIN6/ LINUART_RX	I/O	**X**	X	X	HS	O3	X	X	Port D6	Analog input 6/ LINUART data receive	-
4	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
5	PA1/ OSCIN(2)	I/O	**X**	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
6	PA2/ OSCOUT	I/O	**X**	X	X	-	O1	X	X	Port A2	Resonator/ crystal out	-
7	VSS	S	-	-	-	-	-	-	-	Digital ground		-
8	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
9	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
10	PB5/ I2C_SDA [TIM1_BKIN]	I/O	**X**	-	X	-	O1	T(3)	-	Port B5	I2C data	Timer 1 - break input [AFR4]
11	PB4/ I2C_SCL [ADC_ETR]	I/O	**X**	-	X	-	O1	T(3)	-	Port B4	I2C clock	ADC external trigger [AFR4]
12	PB1/ TIM1_CH2N/ AIN1	I/O	**X**	X	X	HS	O3	X	X	Port B1	Timer 1 - inverted channel 2/Analog input 1	-
13	PB0/ TIM1_CH1N/AIN0	I/O	**X**	X	X	HS	O3	X	X	Port B0	Timer 1 - inverted channel 1/Analog input 0	-
14	PC4/ TIM1_CH4/ CLK_CCO/AIN2/[TIM1_CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4 /configurable clock output	Analog input 2 [AFR2]Timer 1 channel 2 [AFR7]
15	PC5/SPI_SCK [TIM5_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 5 channel 1 [AFR0]

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF
0x00 5208 to 0x00 520F	Reserved area (8 byte)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C own address register low	0x00
0x00 5214		I2C_OARH	I2C own address register high	0x00
0x00 5215		Reserved area (1 byte)		
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C clock control register low	0x00
0x00 521C		I2C_CCRH	I2C clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02
0x00 521E		I2C_PECR	I2C packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 byte)			

6.2.2 CPU/SWIM/debug module/interrupt controller registers

Table 12. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 byte)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)			

Table 12. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 byte)			

1. Accessible by debug module only

Figure 9. f_{CPUmax} versus V_{DD}

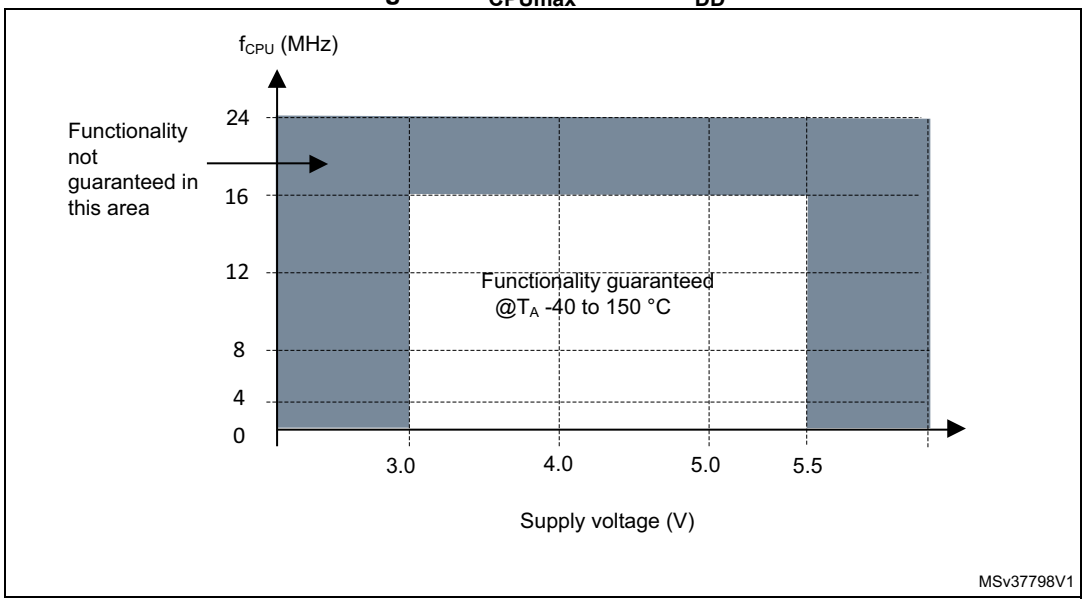


Table 27. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2(1)	-	∞	µs/V
	V_{DD} fall time rate(2)	-	2(1)	-	∞	
t_{TEMP}	Reset release delay	V_{DD} rising	-	-	1.7	ms
V_{IT+}	Power-on reset threshold(3)	-	2.6(1)	2.7	2.85	V
V_{IT-}	Brown-out reset threshold	-	2.5	2.65	2.8(1)	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70(1)	-	mV

1. Guaranteed by design.
2. Reset is always generated after a t_{TEMP} delay. The application must ensure that V_{DD} is still above the minimum operating voltage (V_{DD} min) when the t_{TEMP} delay has elapsed.
3. There is inrush current into V_{DD} present after device power on to charge C_{EXT} capacitor. This inrush energy depends from C_{EXT} capacitor value. For example, a C_{EXT} of 1µF requires Q=1 µF x 1.8V = 1.8 µC.

Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

Figure 11. Typ $I_{DD(RUN)}$ vs. V_{DD} HSE user external clock, f_{CPU} = 16 MHz

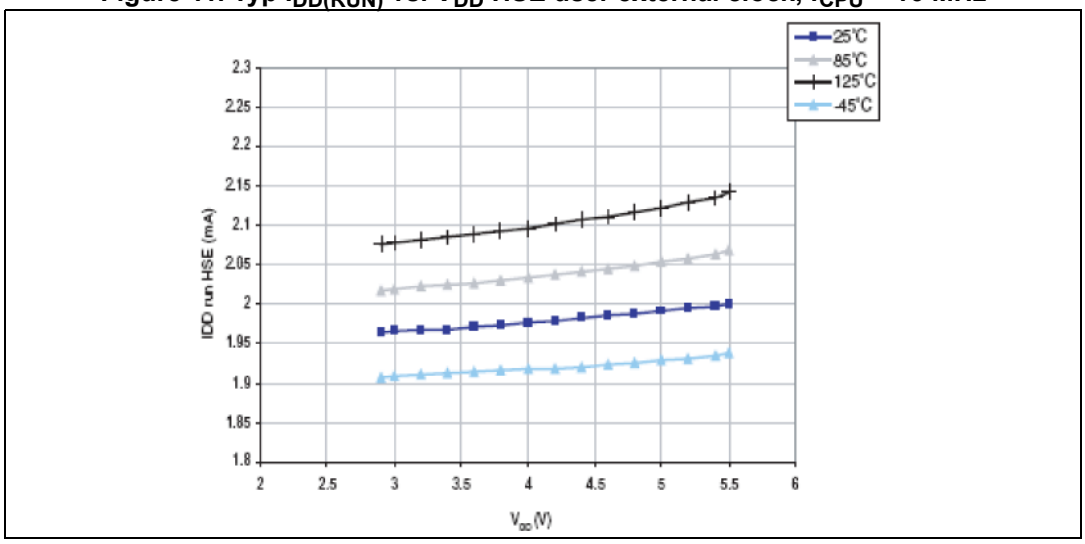
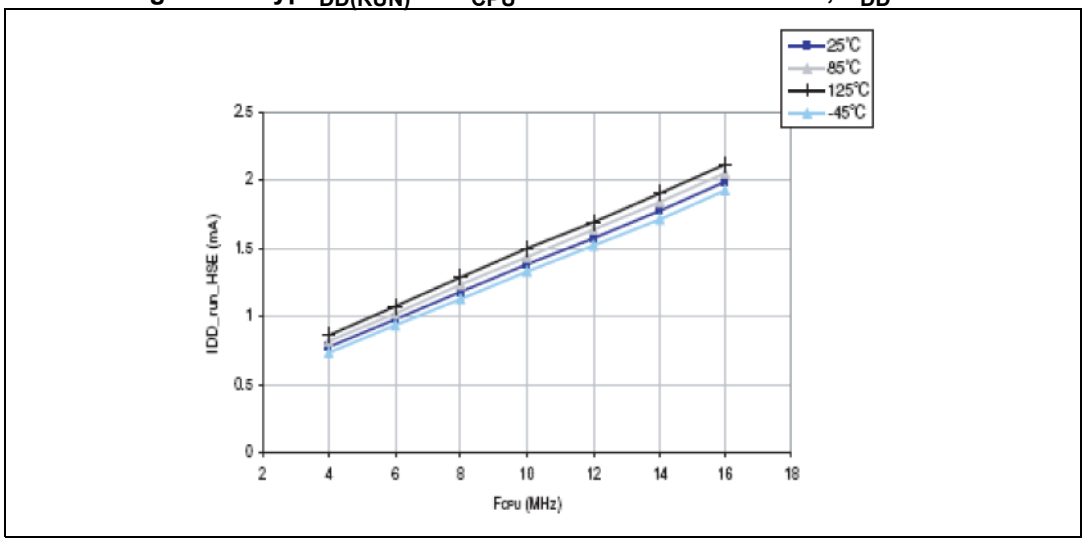


Figure 12. Typ $I_{DD(RUN)}$ vs. f_{CPU} HSE user external clock, V_{DD} = 5 V



9.3.3 External clock sources and timing characteristics

HSE user external clock

Subject to general operating conditions for V_{DD} and T_A.

Table 39. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	-	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage	-	0.7 x V_{DD}	-	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage	-	V_{SS}	-	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	-	+1	µA

1. Guaranteed by characterization results.

Figure 17. HSE external clock source

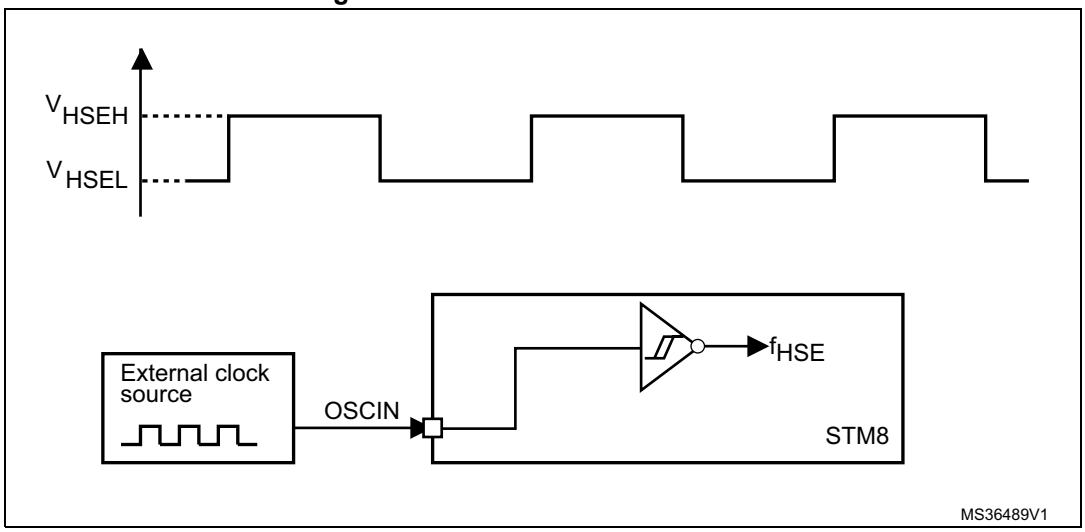


Table 45. Flash program memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Flash program memory endurance (erase/write cycles)(1)	T_A = 25 °C	1000	-	cycles
t_{RET}	Data retention time	T_A = 25 °C	40	-	years
		T_A = 55 °C	20	-	

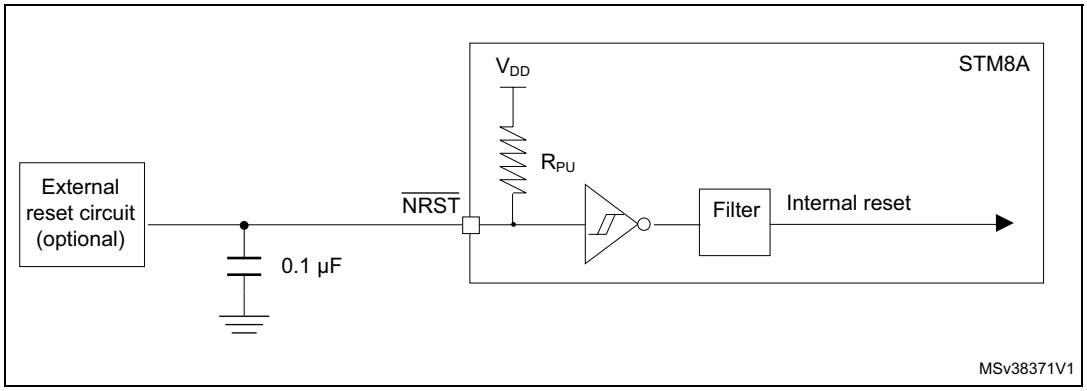
1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.

Table 46. Data memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Data memory endurance(1) (erase/write cycles)	T_A = 25 °C	300 k	-	cycles
		T_A = -40°C to 125 °C	100 k(2)	-	
t_{RET}	Data retention time	T_A = 25 °C	40(3)	-	years
		T_A = 55 °C	20(2)(3)	-	

1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

Figure 35. Recommended reset pin protection



9.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 52. SPI characteristics

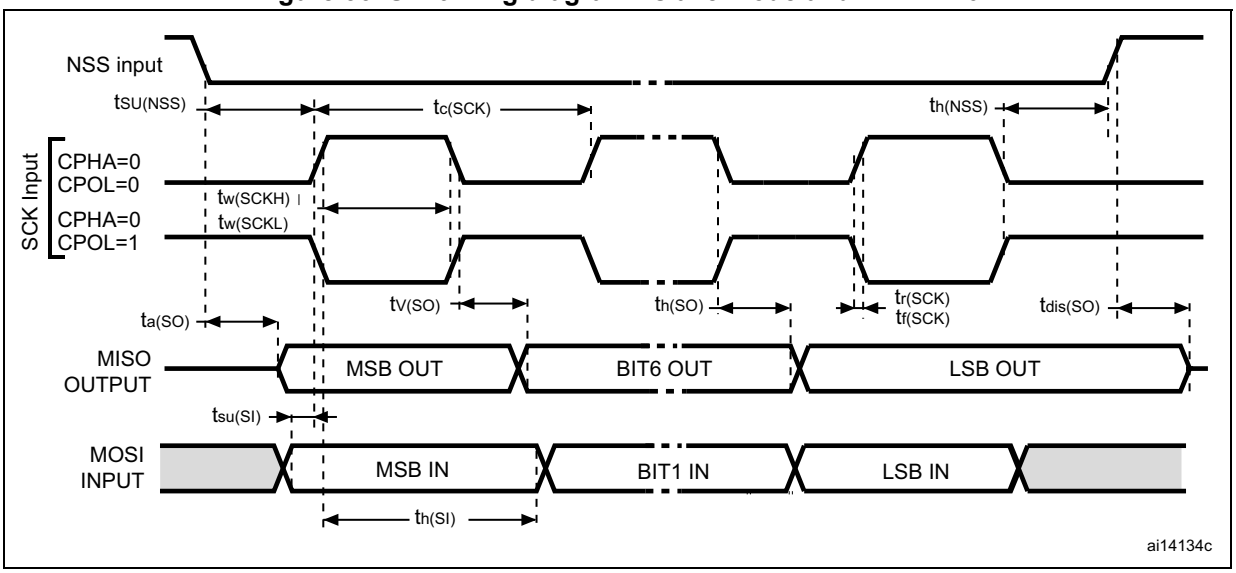
Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	6	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	25	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 * t_{MASTER}	-	
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	70	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master mode	7	-	
		Slave mode	10	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode	-	3* t_{MASTER}	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	25	-	
$t_{v(SO)}$(2)	Data output valid time	Slave mode (after enable edge)	-	65	
$t_{v(MO)}$(2)	Data output valid time	Master mode (after enable edge)	-	36	

Table 52. SPI characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Max	Unit
$t_{h(SO)}$[2]	Data output hold time	Slave mode (after enable edge)	27	-	ns
$t_{h(MO)}$[2]		Master mode (after enable edge)	11	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 36. SPI timing diagram - slave mode and CPHA = 0



1. Measurement points are made at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

9.3.9 I²C interface characteristics

Table 53. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	3450	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
t_{SP}	Pulse width of spikes suppressed by the input filter	0	50(5)	0	50	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL
5. The minimum width of the spikes filtered by the analog filter is above $t_{SP(max)}$

9.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

Table 54. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DD} = 3 to 5.5 V	1	-	4	MHz
		V_{DD} = 4.5 to 5.5 V	1	-	6	
V_{AIN}	Conversion voltage range(1)	-	V_{SS}	-	V_{DD}	V
V_{BGREF}	Internal bandgap reference voltage	V_{DD} = 3 to 5.5 V	1.19(2)	1.22	1.25(2)	V
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
t_S(1)	Minimum sampling time	f_{ADC} = 4MHz	-	0.75	-	µs
		f_{ADC} = 6 MHz	-	0.5	-	
t_{STAB}	Wakeup time from standby	-	-	7	-	
t_{CONV}	Minimum total conversion time including sampling time, 10-bit resolution	f_{ADC} = 4 Hz	3.5			µs
		f_{ADC} = 6 MHz	2.33			
		-	14			$1/f_{ADC}$

1. During the sample time the input capacitance C_{AIN} (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.
2. Tested in production.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

Table 58. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f_{HSE}/f_{CPU}(1)		
				16 MHz/ 8 MHz	16 MHz/ 16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP32 package conforming to IEC 61967-2	0.1 MHz to 30 MHz	5	5	dBµV
			30 MHz to 130 MHz	4	5	
			130 MHz to 1 GHz	5	5	
	EMI level		—	2.5	2.5	level

1. Guaranteed by characterization results.

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (one positive then one negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 59. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine model)	T_A= 25°C, conforming to JESD22-A115	B	200	

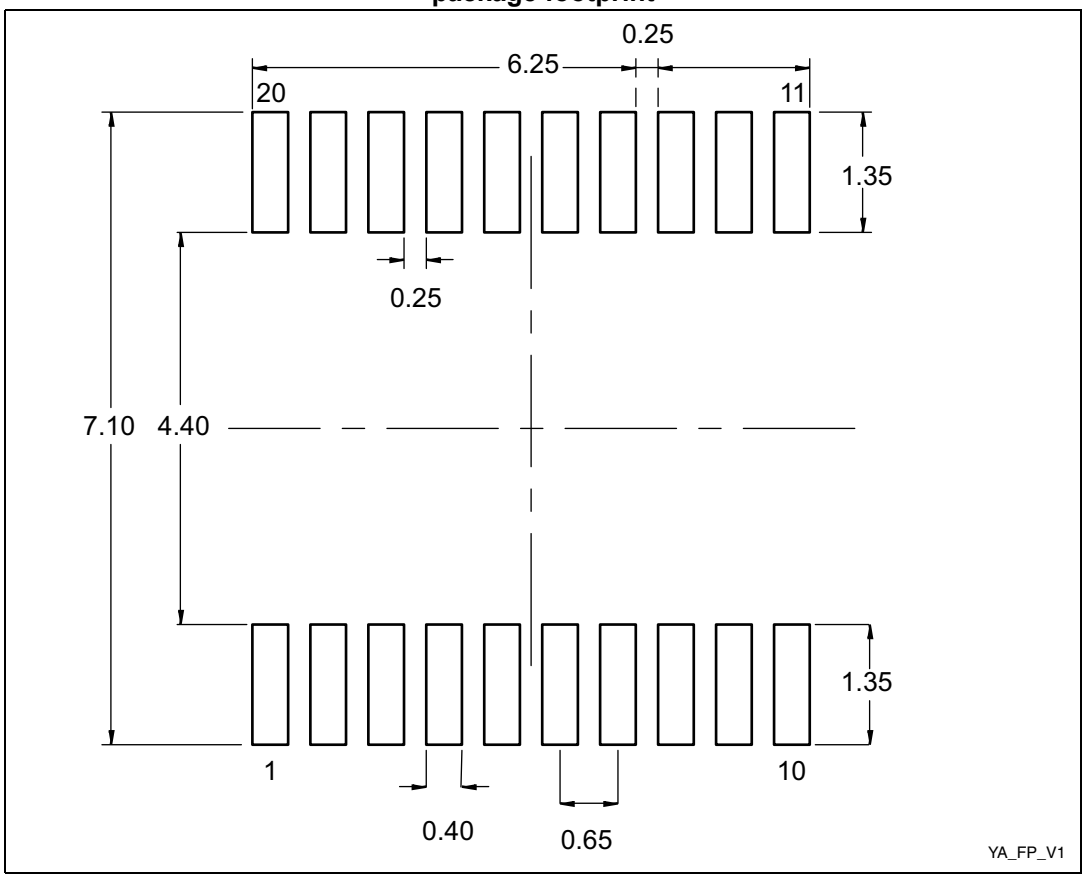
1. Guaranteed by characterization results.

Table 62. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 46. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint



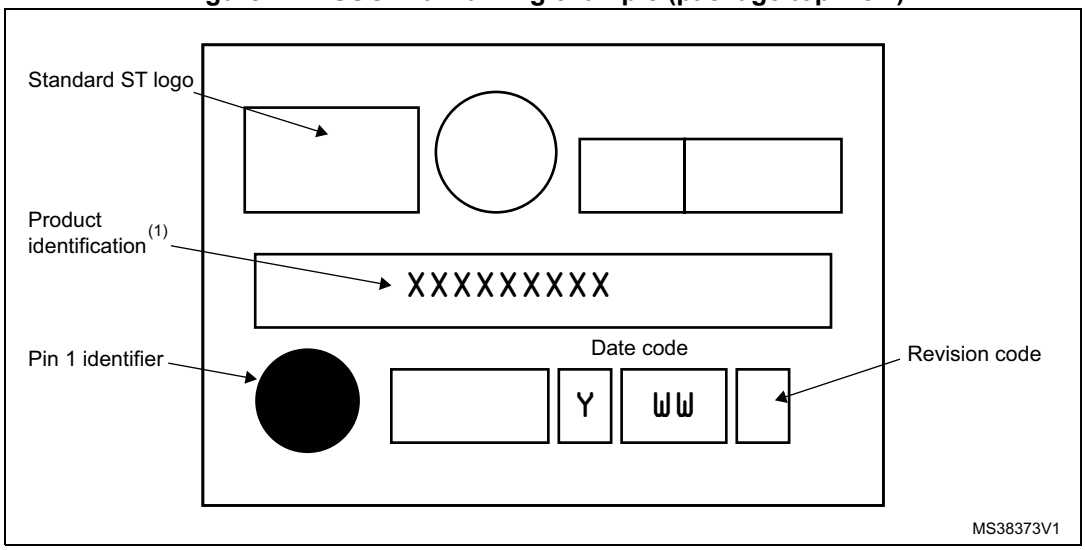
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 47. TSSOP20 marking example (package top view)



1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

10.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 26: General operating conditions*.

T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 64. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient TSSOP20 - 4 x 4 mm	110	°C/W
	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	60	
	Thermal resistance junction-ambient VFQFPN32 - 5 x 5 mm	TBD	

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

10.4.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

10.4.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Section 11: Ordering information*).

The following example shows how to calculate the temperature range needed for a given application.