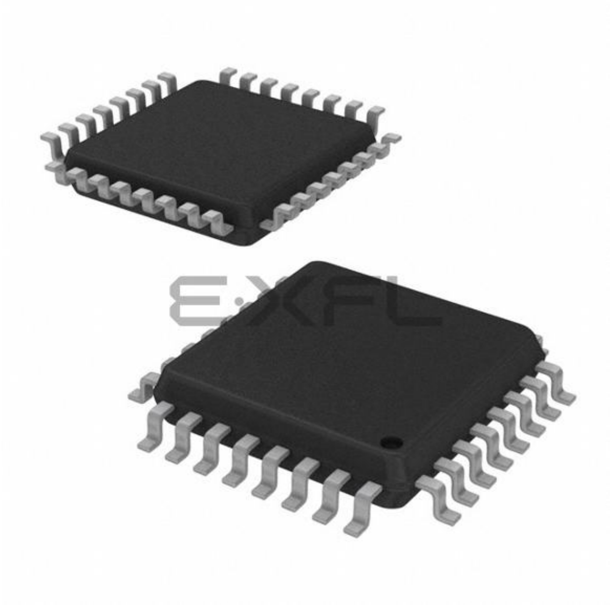
STMicroelectronics - STM8AF6226ITCX Datasheet



Details	
Product Status	Active
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6226itcx

List of tables

2 Description

The STM8AF6213, STM8AF6223, STM8AF6223A and STM8AF6226 automotive 8-bit microcontrollers offer 4 to 8 Kbytes of Flash program memory, plus integrated true data EEPROM. The STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits: performance, robustness and reduced system cost.

Device performance and robustness are ensured by advanced core and peripherals made in a state-of-the-art technology, a 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 kwrite/erase cycles and a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

Table 1. STM8AF6213/23/23A/26 features

Device	STM8AF6226	STM8AF6223	STM8AF6223A	STM8AF6213
Pin count	32	20		
Max. number of GPIOs	28 including 21 high-sink I/Os	16 including 12 high-sink I/Os		
Ext. interrupt pins	28	16		
Timer CAPCOM channels	6	7	6	7
Timer complementary outputs	3	1	2	1
A/D converter channels	7	5	7	5
Low-density Flash program memory (byte)	8 K			4 K
Data EEPROM (byte)	640[1]			
RAM (byte)	1 K			
Peripheral set	Multipurpose timer (TIM1), SPI, I2C, LINUART, window WDG, independent WDG, ADC, PWM timer (TIM5), 8-bit timer (TIM6)			

1. No read-while-write (RWW) capability

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure.

The IWDG time base spans from 60 µs to 1 s

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down auto-reload counter with 16-bit fractional prescaler.
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output.
- Synchronization module to control the timer with external signals or to synchronise with TIM5 or TIM6
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM5 - 16-bit general purpose timer

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- 3 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update
- Synchronization module to control the timer with external signals or to synchronize with TIM1 or TIM6

4.12 TIM6 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update
- Synchronization module to control the timer with external signals or to synchronize with TIM1 or TIM5.

Table 3. TIM timer features

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complementary outputs	Ext. trigger	Timer synchronization/ chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	Yes
TIM5	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM6	8	Any power of 2 from 1 to 128	Up	0	0	No	

4.13 Analog-to-digital converter (ADC1)

The STM8AF6213, STM8AF6223, STM8AF6223A and STM8AF6226 products contain a 10-bit successive approximation A/D converter (ADC1) with up to 7 external and 1 internal multiplexed input channels and the following main features:

- Input voltage range: 0 to V_{DD}
- Input voltage range: 0 to V_{DDA}
- Conversion time: 14 clock cycles
- Single and continuous and buffered continuous conversion modes
- Buffer size (n x 10 bits) where n = number of input channels
- Scan mode for single and continuous conversion of a sequence of channels
- Analog watchdog capability with programmable upper and lower thresholds
- Internal reference voltage on channel AIN7
- Analog watchdog interrupt
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

Note: Additional AIN12 analog input is not selectable in ADC scan mode or with analog watchdog. Values converted from AIN12 are stored only into the ADC_DRH/ADC_DRL registers.

Internal bandgap reference voltage

Channel AIN7 is internally connected to the internal bandgap reference voltage. The internal bandgap reference is constant and can be used, for example, to monitor V_{DD}. It is independent of variations in V_{DD} and ambient temperature T_A.

4.14 Communication interfaces

The following communication interfaces are implemented:

- LINUART: Full feature UART, synchronous mode, SPI master mode, Smartcard mode, IrDA mode, single wire mode, LIN2.2 capability
- SPI: full and half-duplex, 8 Mbit/s
- I²C: up to 400 Kbit/s

Some peripheral names differ between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016 (see *Table 4*).

Table 4. Communication peripheral naming correspondence

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
LINUART	UART4

6.2.2 CPU/SWIM/debug module/interrupt controller registers

Table 12. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU[1]	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 byte)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)			

Table 19. STM8AF6226 alternate function remapping bits [1:0] for 32-pin packages

AFR1 option bit value	AFR0 option bit value	I/O port	Alternate function mapping
0	0	AFR1 and AFR0 remapping options inactive: Default alternate functions(1)	
0	1	PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
1	0	PA3	SPI_NSS
		PD2	TIM5_CH3
1(2)	1(2)	PD2	TIM5_CH3
		PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
		PC2	TIM1_CH3N
		PC1	TIM1_CH2N
		PE5	TIM1_CH1N
		PA3	LINUART_TX
		PF4	LINUART_RX

1. Refer to the pin descriptions.
2. If both AFR1 and AFR0 option bits are set, the SPI hardware NSS management feature is no more available. If this remapping option is selected and the SPI is enabled, the SSM bit must be configured in the SPI_CR2 register to select software NSS management.

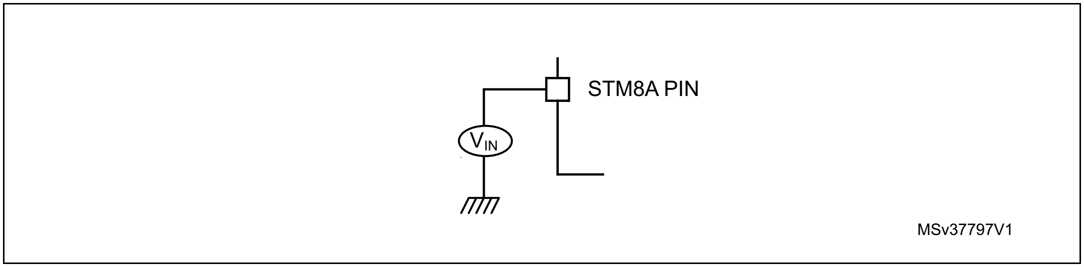
Table 20. STM8AF6213/STM8AF6223 alternate function remapping bits [1:0] for 20-pin packages

AFR1 option bit value	AFR0 option bit value	I/O port	Alternate function mapping
0	0	AFR1 and AFR0 remapping options inactive: Default alternate functions(1)	
0	1	PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
1	0	PA3	SPI_NSS
		PD2	TIM5_CH3

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 8. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 22: Voltage characteristics*, *Table 23: Current characteristics* and *Table 24: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device’s reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 22. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (2)	V_{SS} - 0.3	6.5	V
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\|V_{DDx}$ - $V_{DD}\|$	Variations between different power pins	-	50	mV
$\|V_{SSx}$ - $V_{SS}\|$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 89*		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 23. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(2)	80	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	
$I_{INJ(PIN)}$(3) (4)	Injected current on RST pin	±4	
	Injected current on OSCIN pin	±4	
	Injected current on any other pin(5)	±4	
$\sum I_{INJ(TOT)}$(3)	Total injected current (sum of all I/O and control pins)(5)	±20	

1. Guaranteed by characterization results.
2. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding VIN maximum must always be respected.
4. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and ∑IINJ(PIN) in the I/O port pin characteristics section does not affect the ADC accuracy
5. When several inputs are submitted to a current injection, the maximum ∑IINJ(PIN) is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with ∑IINJ(PIN) maximum current injection on four I/O port pins of the device.

Table 24. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

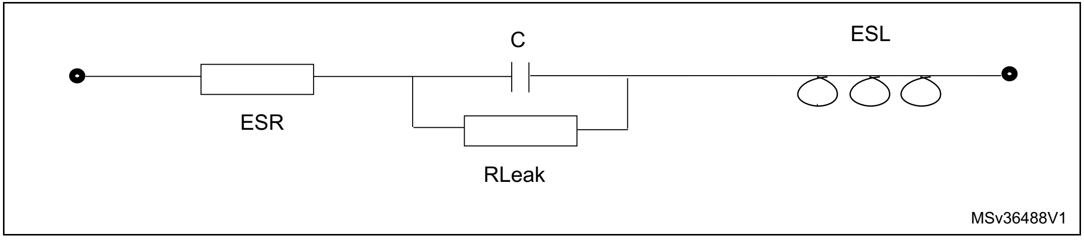
Table 25. Operating lifetime (OLF)

Symbol	Ratings	Value	Unit
OLF	Conforming to AEC-Q100	-40 to 150	°C

9.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 26*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 10. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

9.3.2 Supply current characteristics

The current consumption is measured as described in *Section 4.3: Interrupt controller*.

Total current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by peripheral clock gating registers) except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Unless otherwise specified, data are based on characterization results, and not tested in production.

Table 28. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.3	-	mA
			HSE user ext. clock (16 MHz)	2	2.35	
			HSI RC osc. (16 MHz)	1.7	2(1)	
		$f_{CPU} = f_{MASTER}$/128= 125 kHz	HSE user ext. clock (16 MHz)	0.86	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}$/128= 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 28 kHz	LSI RC osc. (128 kHz)	0.41	0.55	

Total current consumption and timing in forced reset state

Table 37. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max[1]	Unit
$I_{DD(R)}$	Supply current in reset state[2]	V_{DD}= 5 V	400	-	µA
		V_{DD}= 3.3 V	300	-	
$t_{RESETBL}$	Reset pin release to vector fetch	-	-	150	µs

1. Guaranteed by design.
2. Characterized with all I/Os tied to V_{SS}.

Current consumption for on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU} = f_{MASTER} = 16 MHz, V_{DD} = 5 V

Table 38. Peripheral current consumption

Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current[1]	210	µA
$I_{DD(TIM5)}$	TIM5 supply current[1]	130	
$I_{DD(TIM6)}$	TIM6 supply current[1]	50	
$I_{DD(UART1)}$	LINUART supply current[2]	120	
$I_{DD(SPI)}$	SPI supply current[2]	45	
$I_{DD(I2C)}$	I2C supply current[2]	65	
$I_{DD(ADC1)}$	ADC1 supply current[3]	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions. Not tested in production.

9.3.3 External clock sources and timing characteristics

HSE user external clock

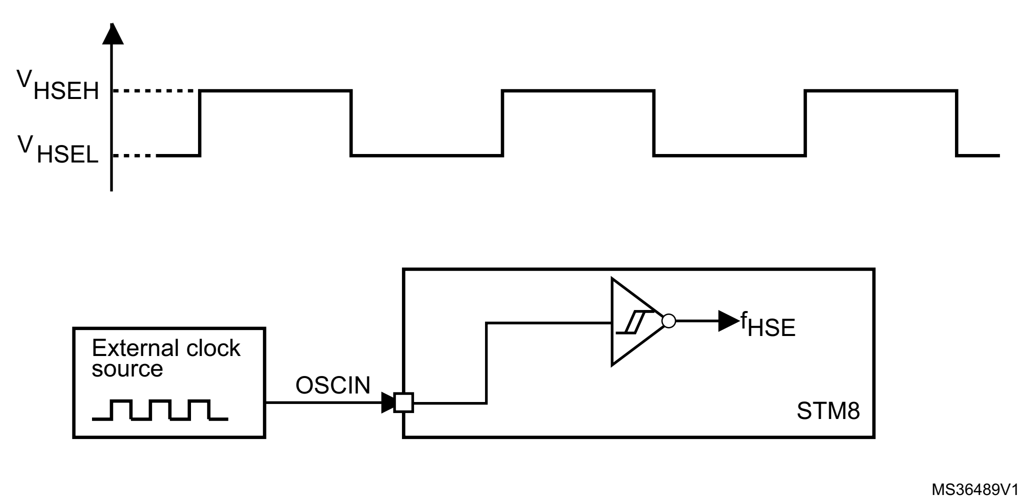
Subject to general operating conditions for V_{DD} and T_A.

Table 39. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	-	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage	-	0.7 x V_{DD}	-	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage	-	V_{SS}	-	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	-	+1	µA

1. Guaranteed by characterization results.

Figure 17. HSE external clock source



Low speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 42. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	110(1)	128	150(1)	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7	µs
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	5	-	µA

1. Tested in production.

9.3.5 Memory characteristics

RAM and hardware registers

Table 43. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	V_{IT-max}(2)	V

1. Minimum supply voltage without losing the data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design.
2. Refer to the operating conditions for the value of V_{IT-max}

Flash program memory/data EEPROM memory

General conditions: T_A = -40 to 150 °C.

Table 44. Flash program memory/data EEPROM memory

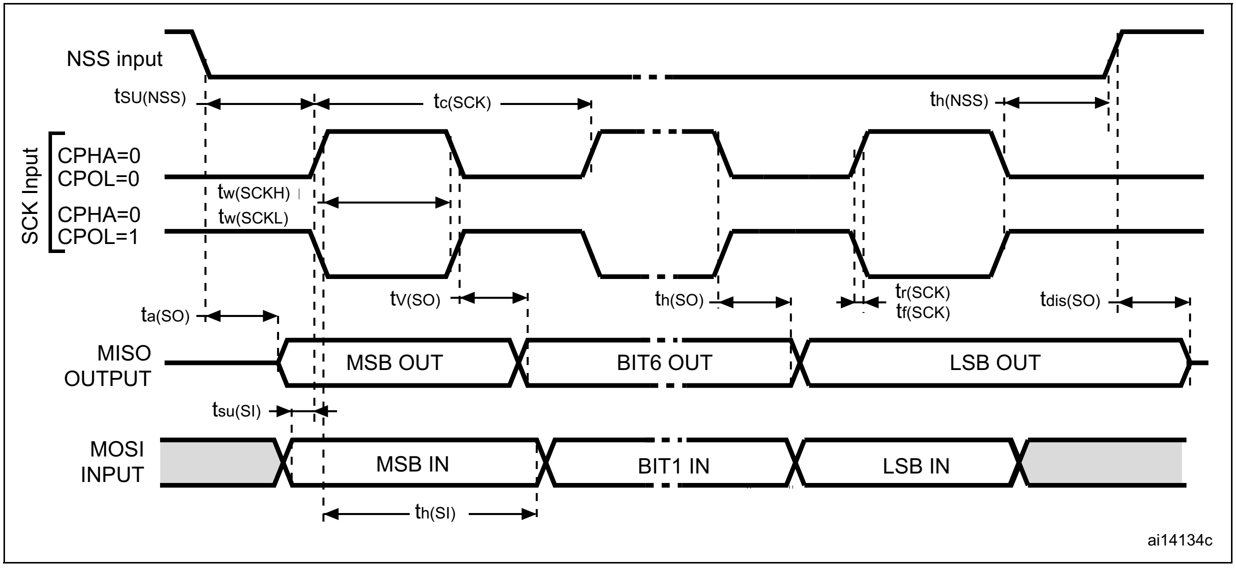
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU} is 0 to 16 MHz with 0 ws	3.0	-	5.5	V
	Operating voltage (code execution)		2.6	-	5.5	
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 byte/64 byte)	-	-	6.0	6.6	ms
	Fast programming time for 1 block (64 byte)	-	-	3.0	3.3	
t_{ERASE}	Erase time for 1 block (64 byte)	-	-	3.0	3.3	

Table 52. SPI characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Max	Unit
$t_{h(SO)}$[2]	Data output hold time	Slave mode (after enable edge)	27	-	ns
$t_{h(MO)}$[2]		Master mode (after enable edge)	11	-	

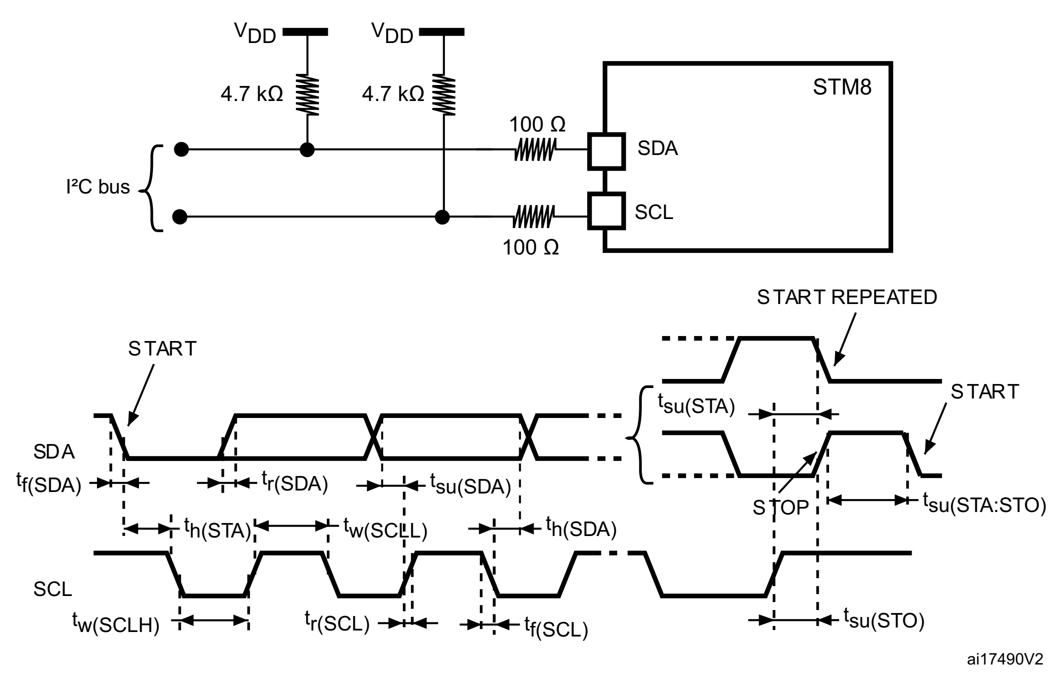
1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 36. SPI timing diagram - slave mode and CPHA = 0



1. Measurement points are made at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 39. Typical application with I2C bus and timing diagram



1. Measurement points are made at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

Table 58. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f_{HSE}/f_{CPU}(1)		
				16 MHz/ 8 MHz	16 MHz/ 16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP32 package conforming to IEC 61967-2	0.1 MHz to 30 MHz	5	5	dBμV
			30 MHz to 130 MHz	4	5	
			130 MHz to 1 GHz	5	5	
	EMI level		—	2.5	2.5	level

1. Guaranteed by characterization results.

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (one positive then one negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 59. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine model)	T_A= 25°C, conforming to JESD22-A115	B	200	

1. Guaranteed by characterization results.

Table 62. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

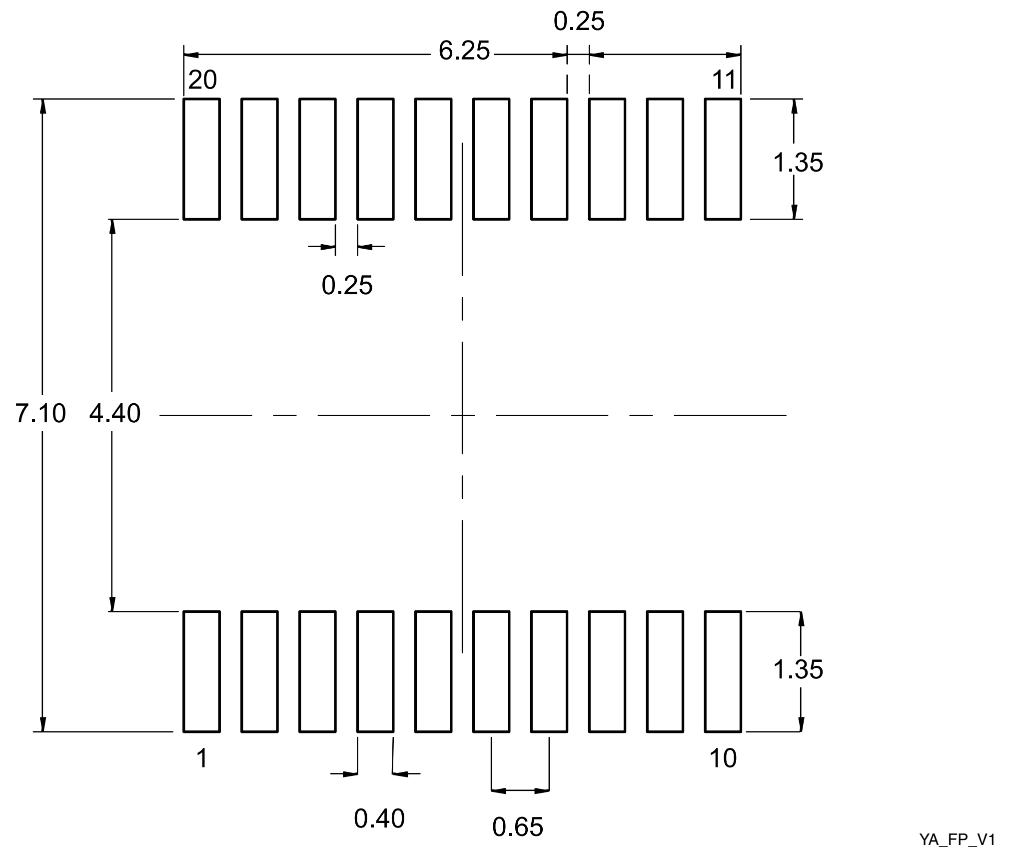


Figure 46. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint

1. Dimensions are expressed in millimeters.

Table 63. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.200	-	-	0.0079	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D2	3.500	3.600	3.700	0.1378	0.1417	0.1457
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E2	3.500	3.600	3.700	0.1378	0.1417	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

11 Ordering information

Table 65. STM8AF6213/23/23A/26 ordering information scheme(1)

Example	STM8A	F	62	2	3	I	P	C	A	U

Product Class

8-bit automotive microcontroller

Program memory type

F = Flash + EEPROM

Device family

62 = LIN only

Program memory size

1 = 4 Kbyte
2 = 8 Kbyte

Pin count

3 = 20 pins
6 = 32 pins

HSI accuracy

Blank = ± 5%
I = ± 3%

Package type

T = LQFP
P = TSSOP
U = VFQFPN

Temperature range

A = -40 to 85 °C
C = -40 to 125 °C
D = -40 to 150 °C

Number of ADC analog inputs

Blank = 5 analog inputs
A = 7 analog inputs

Packing

Y = Tray
U = Tube
X = Tape and reel compliant with EIA 481-C

1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.

Table 66. Document revision history (continued)

Date	Revision	Changes
10-Jul-2014	4	Extended the applicability to STM8AF6213 devices. Updated the program memory feature, the power management, and the clock management features on the cover page. Added the table in *Section: Memory map*. Updated the *Figure:* f_{CPUmax} *versus* V_{DD} in *Section: Operating conditions.* Updated *Section: Ordering information*.
26-Jun-2015	5	Added: – the footnote about the inrush current below *Table 27: Operating conditions at power-up/power-down*, – *Figure 44: LQFP32 marking example (package top view)*, – *Figure 47: TSSOP20 marking example (package top view)*. Updated – LIN standard version, – the register label for LINUART block in *Table 11: General hardware register map*, – the power dissipation in *Table 26: General operating conditions*, – *Table 41: HSI oscillator characteristics* for HSI oscillator accuracy, – the standard for EMI in *Electromagnetic interference (EMI)*, – *Figure 48: STM8AF6213/23/23A/26 ordering information scheme*(1) (2) to add HSI accuracy. Moved *Section 10.4: Thermal characteristics* to *Section 10: Package information*.
28-Mar-2017	6	Updated *Table 6: STM8AF6213/STM8AF6223 TSSOP20 pin description* Added VFQFPN32 (5x5 mm) package information updating: – *Section : Features* on the cover page: added VFQFPN32 (5x5 mm) figure – Added *Section 10.3: VFQFPN32 package information*: – Updated *Table 26: General operating conditions* – Updated *Table 64: Thermal characteristics* – Updated *Section 5.2: LQFP32/VFQPN32 pinout and pin description* – Updated *Section 11: Ordering information* Additional updates (not related to VFQFPN32): – Table footnotes on *Section 9: Electrical characteristics* – Updated *Section : Device marking on page 93*, *Section : Device marking on page 96* and *Section : Device marking on page 100* – *Section 9.2: Absolute maximum ratings*