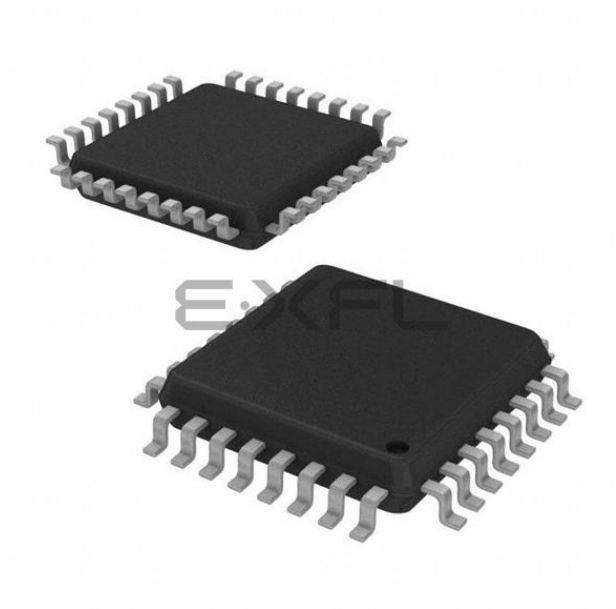

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6226tcy

Contents

1 Introduction

The datasheet contains the description of STM8AF6213, STM8AF6223, STM8AF6223A and STM8AF6226 features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8 Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

2 Description

The STM8AF6213, STM8AF6223, STM8AF6223A and STM8AF6226 automotive 8-bit microcontrollers offer 4 to 8 Kbytes of Flash program memory, plus integrated true data EEPROM. The STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits: performance, robustness and reduced system cost.

Device performance and robustness are ensured by advanced core and peripherals made in a state-of-the-art technology, a 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 kwrite/erase cycles and a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

Table 1. STM8AF6213/23/23A/26 features

Device	STM8AF6226	STM8AF6223	STM8AF6223A	STM8AF6213
Pin count	32	20		
Max. number of GPIOs	28 including 21 high-sink I/Os	16 including 12 high-sink I/Os		
Ext. interrupt pins	28	16		
Timer CAPCOM channels	6	7	6	7
Timer complementary outputs	3	1	2	1
A/D converter channels	7	5	7	5
Low-density Flash program memory (byte)	8 K			4 K
Data EEPROM (byte)	640(1)			
RAM (byte)	1 K			
Peripheral set	Multipurpose timer (TIM1), SPI, I2C, LINUART, window WDG, independent WDG, ADC, PWM timer (TIM5), 8-bit timer (TIM6)			

1. No read-while-write (RWW) capability

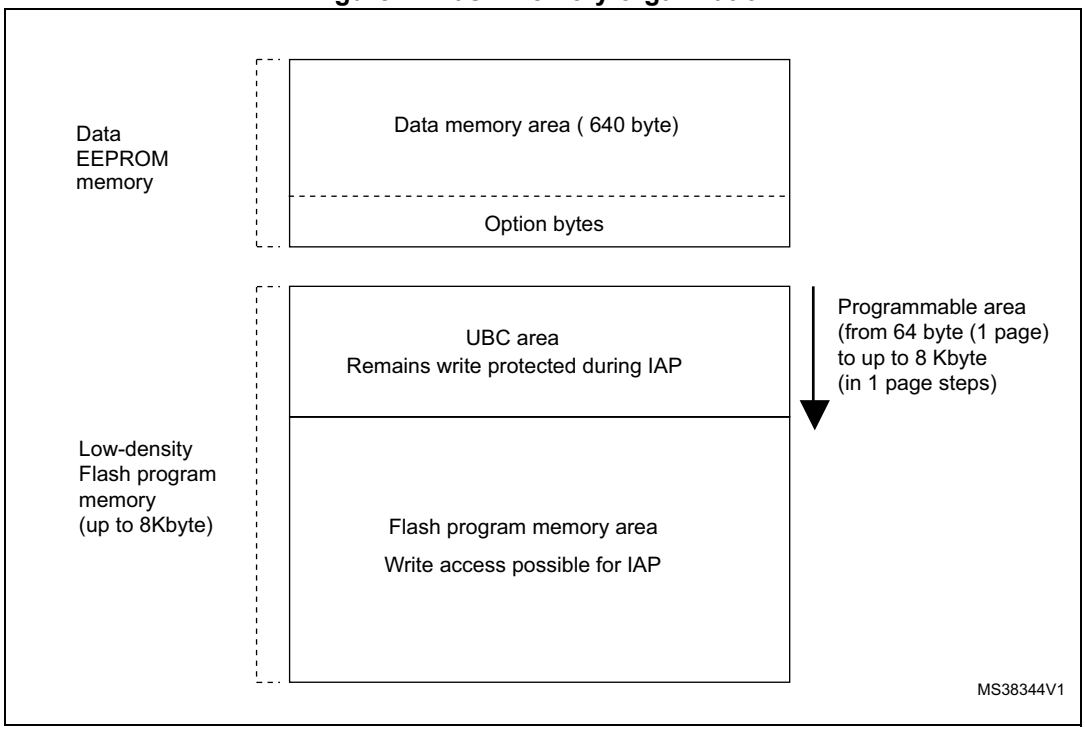
The size of the UBC is programmable through the UBC option byte, in increments of 1 page (64-byte block) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: up to 8 Kbyte minus UBC
- User-specific boot code (UBC): configurable up to 8 Kbyte

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



4.4.2 Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

4.14.2 Serial peripheral interface (SPI)

- Maximum speed: 8 Mbit/s (f_{MASTER}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave /master selection input pin

4.14.3 Inter integrated circuit (I^2C) interface

- I^2C master features:
  - Clock generation
  - Start and stop generation
- I^2C slave features:
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)

5 Pinout and pin description

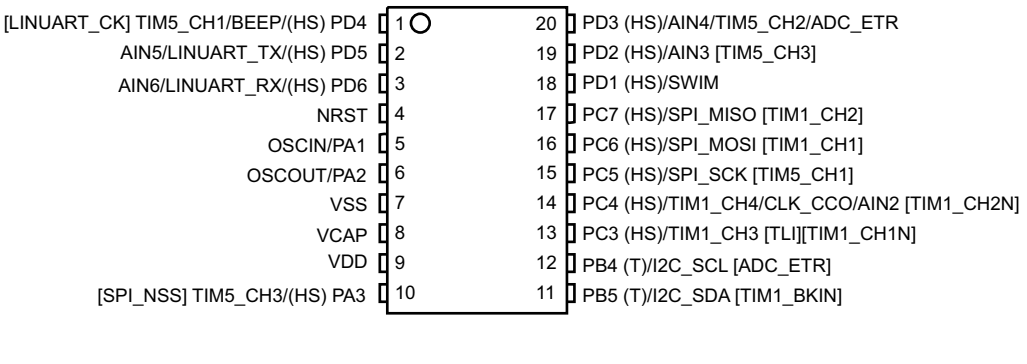
The following table presents the meaning of the abbreviations in use in the pin description tables in this section.

Table 5. Legend/abbreviations for pinout tables

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS (standard for all I/Os)
	Output	HS = High sink
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after internal reset release). Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release.	

5.1 TSSOP20 pinouts and pin descriptions

Figure 3. STM8AF6213/STM8AF6223 TSSOP20 pinout



1. (HS) high sink capability.
2. (T) true open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 6. STM8AF6213/STM8AF6223 TSSOP20 pin description (continued)

TSSOP	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
10	PA3/ TIM5_CH3 [SPI_NSS]	I/O	**X**	X	X	HS	O3	X	X	Port A3	Timer 5 channel 3	SPI master/ slave select [AFR1]
11	PB5/ I2C_SDA [TIM1_BKIN]	I/O	**X**	-	X	-	O1	T(3)	-	Port B5	I2C data	Timer 1 - break input [AFR4]
12	PB4/ I2C_SCL [ADC_ETR]	I/O	**X**	-	X	-	O1	T(3)	-	Port B4	I2C clock	ADC external trigger [AFR4]
13	PC3/ TIM1_CH3/[TLI]/[TIM1_CH1N]	I/O	**X**	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	Top level interrupt [AFR3] Timer 1 inverted channel 1 [AFR7]
14	PC4/ TIM1_CH4/ CLK_CCO/AIN2/[TIM1_CH2N]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4 /configurabl e clock output	Analog input 2 [AFR2]Time r 1 inverted channel 2 [AFR7]
15	PC5/SPI_SCK [TIM5_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 5 channel 1 [AFR0]
16	PC6/ SPI_MOSI [TIM1_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C6	PI master out/slave in	Timer 1 channel 1 [AFR0]
17	PC7/ SPI_MISO [TIM1_CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 channel 2[AFR0]
18	PD1/ SWIM(4)	I/O	**X**	X	X	HS	O4	X	X	Port D1	SWIM data interface	-

Table 7. STM8AF6223A TSSOP20 pin description (continued)

TSSOP	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
16	PC6/ SPI_MOSI [TIM1_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C6	PI master out/slave in	Timer 1 channel 1 [AFR0]
17	PC7/ SPI_MISO [TIM1_CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 channel 2[AFR0]
18	PD1/ SWIM(4)	I/O	**X**	X	X	HS	O4	X	X	Port D1	SWIM data interface	-
19	PD2/AIN3/ TLI[TIM5_CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	-	Analog input 3 [AFR2] Timer 5 - channel 3 [AFR1]
20	PD3/ AIN4/ TIM5_CH2/ ADC_ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Analog input 4 Timer 52 - channel 2/ADC external trigger	-

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 9.2: Absolute maximum ratings*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

Table 9. Memory model for the devices covered in this datasheet

Flash program memory size	Flash program memory end address	RAM size	RAM end address	Stack roll-over address
8 K	0x00 9FFF	1 K	0x00 03FF	0x00 0200
4 K	0x00 8FFF			

6.2 Register map

6.2.1 I/O port hardware register map

Table 10. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX(1)
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX(1)
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX(1)
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX(1)
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 17. STM8AF6213 and STM8AF6223 alternate function remapping bits [7:2] for 20-pin packages

Option byte number	Description(1)
OPT2	**AFR7: Alternate function remapping option 7** 0: AFR7 remapping option inactive: default alternate function (2) 1: Port C3 alternate function = = TIM1_CH1N; port C4 alternate function = TIM1_CH2N **AFR6: Alternate function remapping option 6** Reserved **AFR5: Alternate function remapping option 5** Reserved **AFR4: Alternate function remapping option 4** 0: AFR4 remapping option inactive: default alternate function (2). 1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN. **AFR3: Alternate function remapping option 3** 0: AFR3 remapping option inactive: default alternate function (2) 1: Port C3 alternate function = TLI **AFR2: Alternate function remapping option 2** 0: AFR2 remapping option inactive: default alternate function (2) 1: Port D4 alternate function = LINUART_CK

1. Do not use more than one remapping option in the same port.
2. Refer to the pin description.

Table 18. STM8AF6223A alternate function remapping bits [7:2] for 20-pin packages

Option byte number	Description(1)
OPT2	**AFR7: Alternate function remapping option 7** 0: AFR7 remapping option inactive: default alternate function (2) 1: Port C4 alternate function = TIM1_CH2N **AFR6: Alternate function remapping option 6** Reserved **AFR5: Alternate function remapping option 5** Reserved **AFR4: Alternate function remapping option 4** 0: AFR4 remapping option inactive: default alternate function (2). 1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN. **AFR3: Alternate function remapping option 3** Reserved. **AFR2: Alternate function remapping option 2** 0: AFR2 remapping option inactive: default alternate function (2) 1: Port D4 alternate function = LINUART_CK

1. Do not use more than one remapping option in the same port.
2. Refer to the pin description.

Table 19. STM8AF6226 alternate function remapping bits [1:0] for 32-pin packages

AFR1 option bit value	AFR0 option bit value	I/O port	Alternate function mapping
0	0	AFR1 and AFR0 remapping options inactive: Default alternate functions(1)	
0	1	PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
1	0	PA3	SPI_NSS
		PD2	TIM5_CH3
1(2)	1(2)	PD2	TIM5_CH3
		PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
		PC2	TIM1_CH3N
		PC1	TIM1_CH2N
		PE5	TIM1_CH1N
		PA3	LINUART_TX
		PF4	LINUART_RX

1. Refer to the pin descriptions.
2. If both AFR1 and AFR0 option bits are set, the SPI hardware NSS management feature is no more available. If this remapping option is selected and the SPI is enabled, the SSM bit must be configured in the SPI_CR2 register to select software NSS management.

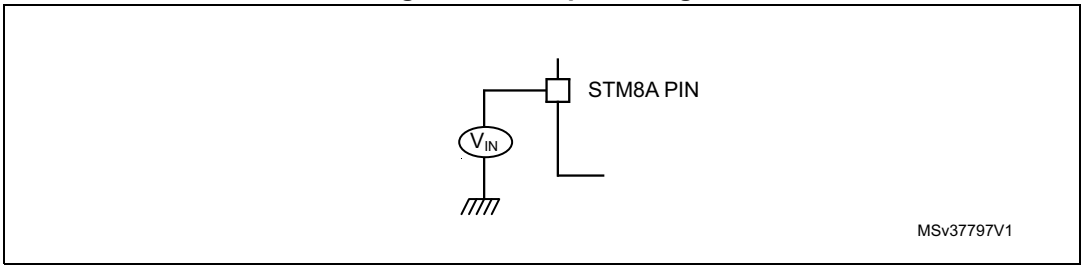
Table 20. STM8AF6213/STM8AF6223 alternate function remapping bits [1:0] for 20-pin packages

AFR1 option bit value	AFR0 option bit value	I/O port	Alternate function mapping
0	0	AFR1 and AFR0 remapping options inactive: Default alternate functions(1)	
0	1	PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
1	0	PA3	SPI_NSS
		PD2	TIM5_CH3

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 8. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 22: Voltage characteristics*, *Table 23: Current characteristics* and *Table 24: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 22. Voltage characteristics

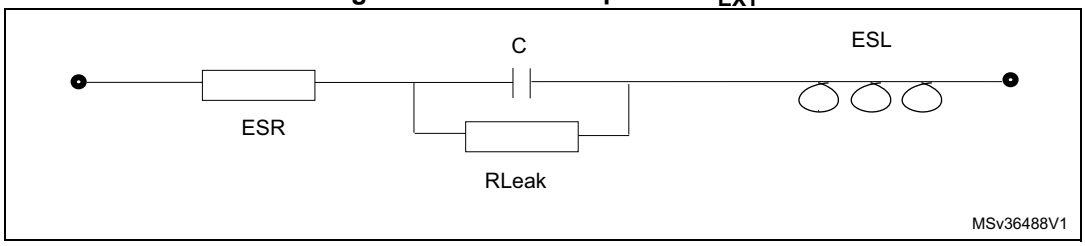
Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (2)	V_{SS} - 0.3	6.5	V
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 89*		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

9.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 26*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 10. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

9.3.2 Supply current characteristics

The current consumption is measured as described in *Section 4.3: Interrupt controller*.

Total current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by peripheral clock gating registers) except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Unless otherwise specified, data are based on characterization results, and not tested in production.

Table 28. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.3	-	mA
			HSE user ext. clock (16 MHz)	2	2.35	
			HSI RC osc. (16 MHz)	1.7	2(1)	
		$f_{CPU} = f_{MASTER}/128$= 125 kHz	HSE user ext. clock (16 MHz)	0.86	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}/128$= 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 28 kHz	LSI RC osc. (128 kHz)	0.41	0.55	

Table 50. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	0.8	V
	Output low level with 4 pins sunk	I_{IO} = 10 mA, V_{DD} = 3.3 V	-	1.0(1)	
		I_{IO} = 20 mA, V_{DD} = 5 V		1.5(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	4.0	-	
	Output high level with 4 pins sourced	I_{IO} = 10 mA, V_{DD} = 3.3 V	2.1(1)	-	
		I_{IO} = 20 mA, V_{DD} = 5 V	3.3(1)	-	

1. Guaranteed by characterization results.

Figure 22. Typ. V_{OL} @ V_{DD} = 5 V (standard ports)

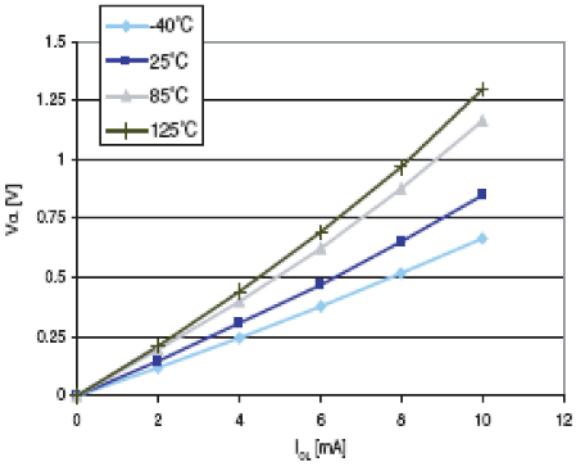


Figure 23. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

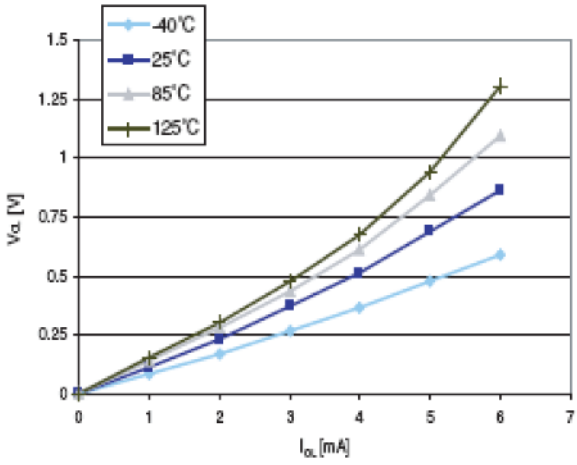


Figure 30. Typ. V_{DD}- V_{OH} @ V_{DD} = 5 V (high sink ports)

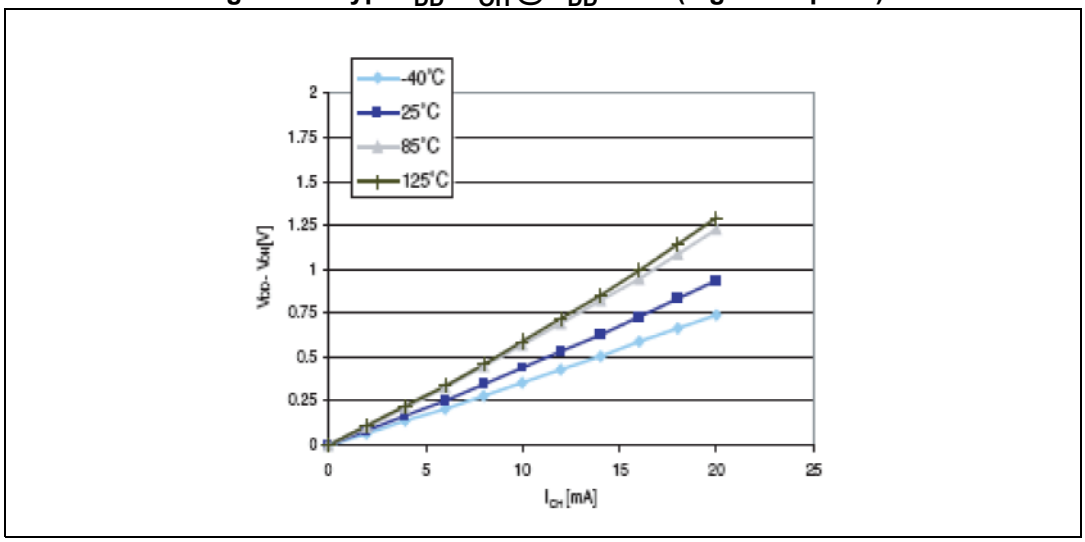
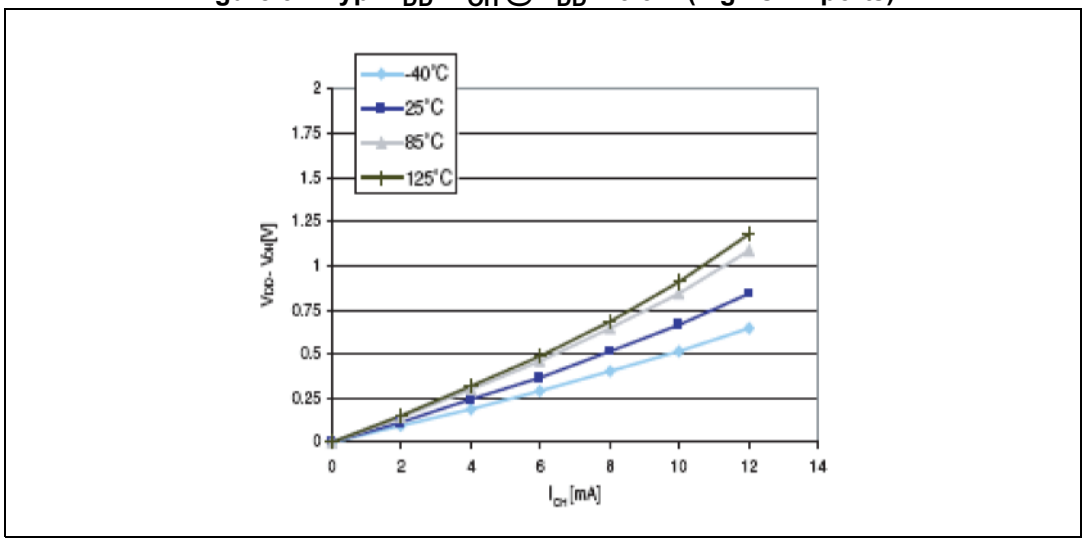


Figure 31. Typ. V_{DD}- V_{OH} @ V_{DD} = 3.3 V (high sink ports)



9.3.9 I²C interface characteristics

Table 53. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	3450	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
t_{SP}	Pulse width of spikes suppressed by the input filter	0	50(5)	0	50	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL
5. The minimum width of the spikes filtered by the analog filter is above $t_{SP(max)}$

Table 55. ADC accuracy with RAIN < 10 kΩ, V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	2.2	4	
		f_{ADC} = 6 MHz	2.4	4.5	
$\|E_O\|$	Offset error(2)	f_{ADC} = 2 MHz	1.1	2.5	
		f_{ADC} = 4 MHz	1.5	3	
		f_{ADC} = 6 MHz	1.8	3	
$\|E_G\|$	Gain error(2)	f_{ADC} = 2 MHz	1.5	3	
		f_{ADC} = 4 MHz	2.1	3	
		f_{ADC} = 6 MHz	2.2	4	
$\|E_D\|$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	0.7	1.5	
		f_{ADC} = 6 MHz	0.7	1.5	
$\|E_L\|$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	
		f_{ADC} = 6 MHz	0.8	2	

1. Max value is based on characterization, not tested in production.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristics section does not affect the ADC accuracy.

Table 56. ADC accuracy with RAIN < 10 kΩ, V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	1.9	4	
$\|E_O\|$	Offset error	f_{ADC} = 2 MHz	1	2.5	
		f_{ADC} = 4 MHz	1.5	2.5	
$\|E_G\|$	Gain error	f_{ADC} = 2 MHz	1.3	3	
		f_{ADC} = 4 MHz	2	3	
$\|E_D\|$	Differential linearity error	f_{ADC} = 2 MHz	0.7	1	
		f_{ADC} = 4 MHz	0.7	1.5	
$\|E_L\|$	Integral linearity error	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	

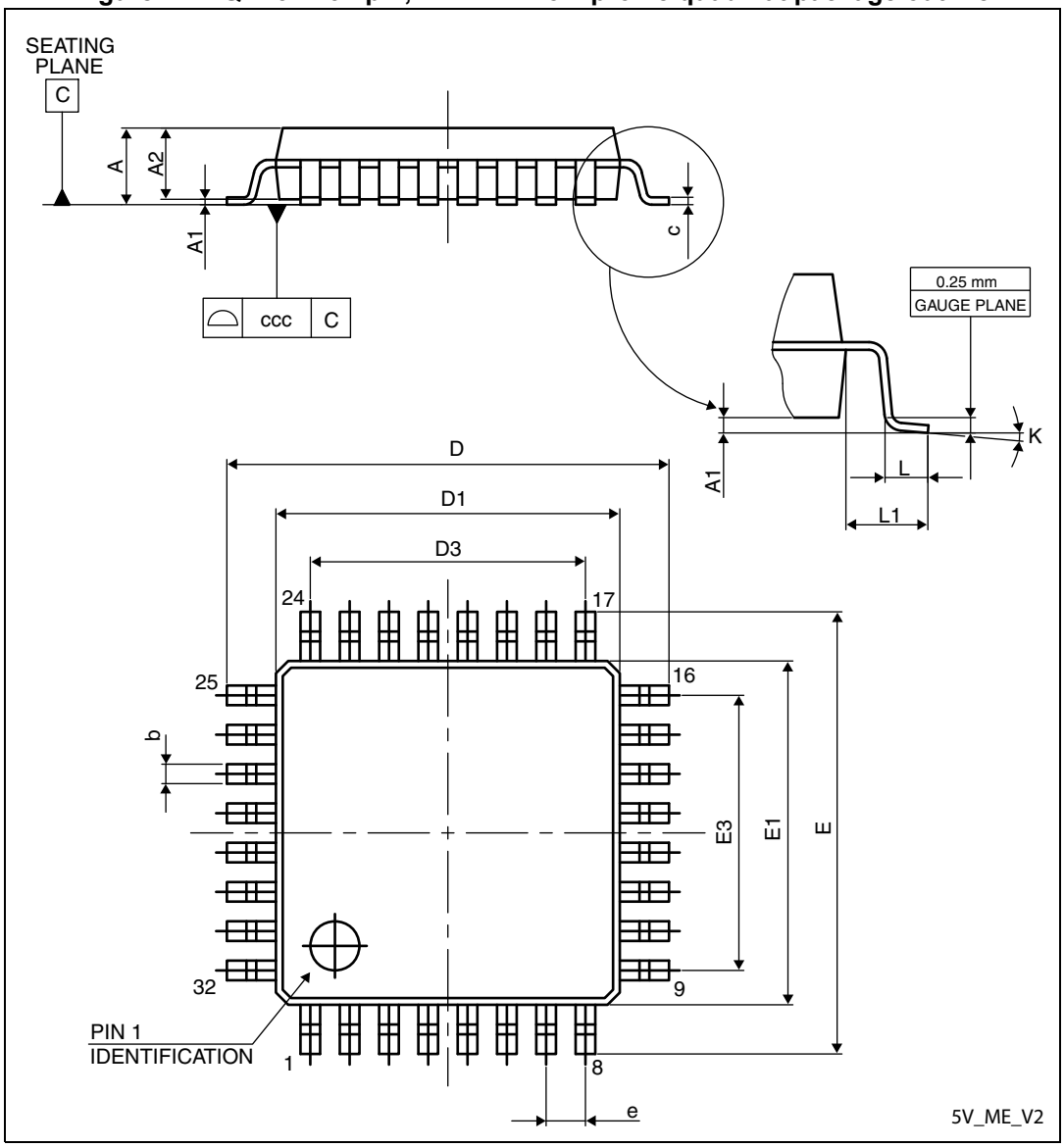
1. Max value is based on characterization, not tested in production.

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

10.1 LQFP32 package information

Figure 42. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax}= 75 °C (measured according to JESD51-2), I_{DDmax} = 8 mA, V_{DD} = 5 V

Maximum 20 I/Os used at the same time in output at low level with:
I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 8 mA x 5 V= 400 mW

P_{IOmax} = 20 x 8 mA x 0.4 V = 64 mW

This gives: P_{INTmax} = 400 mW and P_{IOmax} 64 mW:

P_{Dmax} = 400 mW + 64 mW

Thus: P_{Dmax} = 464 mW.

Using the values obtained in *Table 64: Thermal characteristics on page 101* T_{Jmax} is calculated as follows:

For LQFP32 60 °C/W

T_{Jmax} = 75 °C + (60 °C/W x464 mW) = 75 °C + 27.8 °C = 102.8 °C

This is within the range of the suffix C version parts (-40 < T_J < 125 °C).

Parts must be ordered at least with the temperature range suffix C.