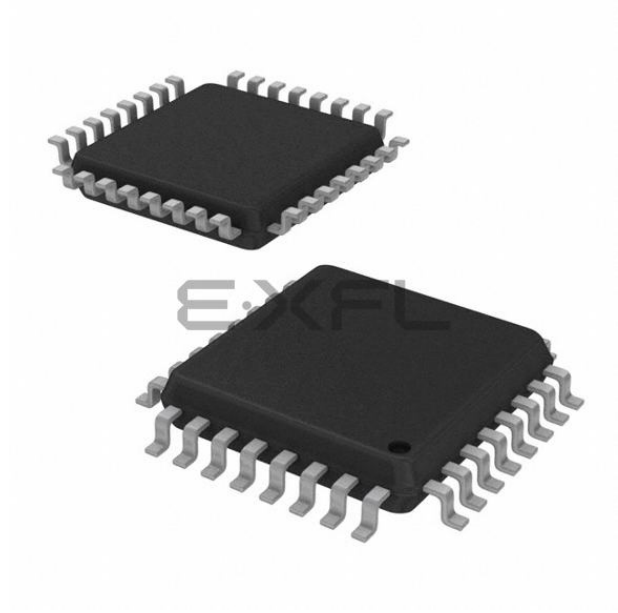

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6246itcx

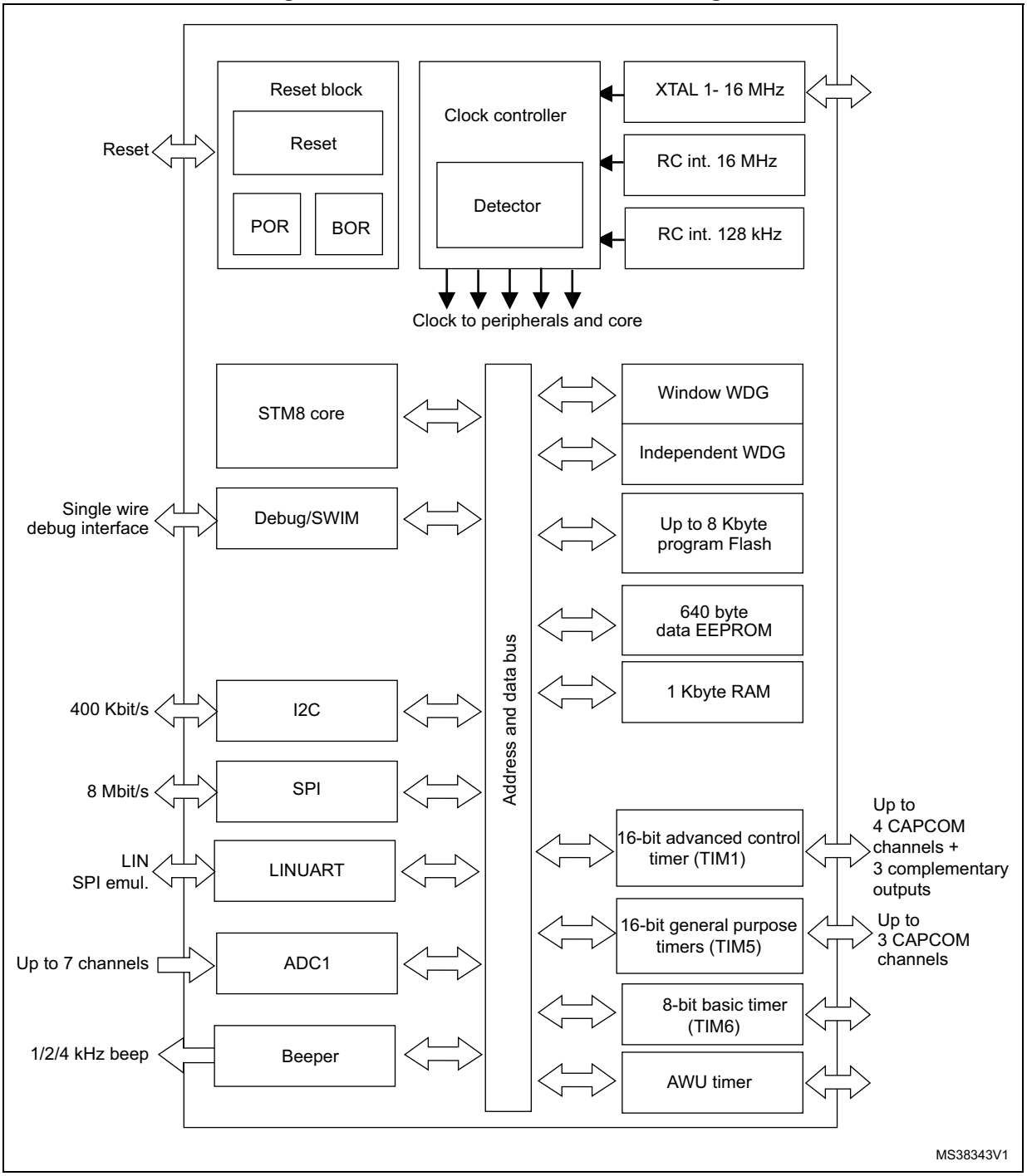
1 Introduction

The datasheet contains the description of STM8AF6213, STM8AF6223, STM8AF6223A and STM8AF6226 features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8 Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

3 Block diagram

Figure 1. STM8AF6213/23/23A/26 block diagram



1. **Legend:** ADC (Analog-to-digital converter), beCAN (Controller area network), BOR (Brownout reset), I²C (Inter-integrated circuit multimaster interface),IWDG (Independent window watchdog), LINUART (Local interconnect network universal asynchronous receiver transmitter), POR (Power on reset), SPI (Serial peripheral interface), SWIM (Single wire interface module), USART (Universal synchronous asynchronous receiver transmitter), Window WDG (Window watchdog).

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure.

The IWDG time base spans from 60 µs to 1 s

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down auto-reload counter with 16-bit fractional prescaler.
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output.
- Synchronization module to control the timer with external signals or to synchronise with TIM5 or TIM6
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.14.1 LINUART

Main features

- 1 Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN mode
- Single wire half duplex mode

LIN mode

Master mode:

- LIN break and delimiter generation
- LIN break and delimiter detection with separate flag and interrupt source for read back checking.

Slave mode:

- Autonomous header handling – one single interrupt per valid header
- Mute mode to filter responses
- Identifier parity error checking
- LIN automatic resynchronization, allowing operation with internal RC oscillator (HSI) clock source
- Break detection at any time, even during a byte reception
- Header errors detection:
  - Delimiter too short
  - Synch field error
  - Deviation error (if automatic resynchronization is enabled)
  - Framing error in synch field or identifier field
  - Header time-out

Table 6. STM8AF6213/STM8AF6223 TSSOP20 pin description (continued)

TSSOP	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
19	PD2/AIN3 [TIM5_CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	-	Analog input 3 [AFR2] Timer 52 - channel 3 [AFR1]
20	PD3/ AIN4/ TIM5_CH2/ ADC_ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Analog input 4 Timer 52 - channel 2/ADC external trigger	-

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 9.2: Absolute maximum ratings*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented)
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

Table 7. STM8AF6223A TSSOP20 pin description

TSSOP	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
1	PD4/ TIM5_CH1/ BEEP/SPI_NSS [LINUART_CK]	I/O	**X**	X	X	HS	O3	X	X	Port D4	Timer 5 - channel 1/BEEP output	LINUART clock [AFR2]
2	PD5/ AIN5/ LINUART_TX	I/O	**X**	X	X	HS	O3	X	X	Port D5	Analog input 5/ LINUART data transmit	-

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	LINUART	UART4_SR	LINUART status register	0xC0
0x00 5231		UART4_DR	LINUART data register	0xXX
0x00 5232		UART4_BRR1	LINUART baud rate register 1	0x00
0x00 5233		UART4_BRR2	LINUART baud rate register 2	0x00
0x00 5234		UART4_CR1	LINUART control register 1	0x00
0x00 5235		UART4_CR2	LINUART control register 2	0x00
0x00 5236		UART4_CR3	LINUART control register 3	0x00
0x00 5237		UART4_CR4	LINUART control register 4	0x00
0x00 5238		Reserved		
0x00 5239		UART4_CR6	LINUART control register 6	0x00
0x00 523A		UART4_GTR	LINUART guard time register	0x00
0x00 523B		UART4_PSCR	LINUART prescaler	0x00
0x00 523C to 0x00 523F	Reserved area (20 byte)			

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM5	TIM5_CR1	TIM5 control register 1	0x00
0x00 5301		TIM5_CR2	TIM5 control register 2	0x00
0x00 5302		TIM5_SMCR	TIM5 slave mode control register	0x00
0x00 5303		TIM5_IER	TIM5 interrupt enable register	0x00
0x00 5304		TIM5_SR1	TIM5 status register 1	0x00
0x00 5305		TIM5_SR2	TIM5 status register 2	0x00
0x00 5306		TIM5_EGR	TIM5 event generation register	0x00
0x00 5307		TIM5_CCMR1	TIM5 capture/compare mode register 1	0x00
0x00 5308		TIM5_CCMR2	TIM5 capture/compare mode register 2	0x00
0x00 5309		TIM5_CCMR3	TIM5 capture/compare mode register 3	0x00
0x00 530A		TIM5_CCER1	TIM5 capture/compare enable register 1	0x00
0x00 530B		TIM5_CCER2	TIM5 capture/compare enable register 2	0x00
00 530C0x		TIM5_CNTRH	TIM5 counter high	0x00
0x00 530D		TIM5_CNTRL	TIM5 counter low	0x00
0x00 530E		TIM5_PSCR	TIM5 prescaler register	0x00
0x00 530F		TIM5_ARRH	TIM5 auto-reload register high	0xFF
0x00 5310		TIM5_ARRL	TIM5 auto-reload register low	0xFF
0x00 5311		TIM5_CCR1H	TIM5 capture/compare register 1 high	0x00
0x00 5312		TIM5_CCR1L	TIM5 capture/compare register 1 low	0x00
0x00 5313		TIM5_CCR2H	TIM5 capture/compare reg. 2 high	0x00
0x00 5314		TIM5_CCR2L	TIM5 capture/compare register 2 low	0x00
0x00 5315		TIM5_CCR3H	TIM5 capture/compare register 3 high	0x00
0x00 5316		TIM5_CCR3L	TIM5 capture/compare register 3 low	0x00
0x00 5317 to 0x00 533F	Reserved area (43 byte)			
0x00 5340	TIM6	TIM6_CR1	TIM6 control register 1	0x00
0x00 5341		TIM6_CR2	TIM6 control register 2	0x00
0x00 5342		TIM6_SMCR	TIM6 slave mode control register	0x00
0x00 5343		TIM6_IER	TIM6 interrupt enable register	0x00
0x00 5344		TIM6_SR	TIM6 status register	0x00
0x00 5345		TIM6_EGR	TIM6 event generation register	0x00
0x00 5346		TIM6_CNTR	TIM6 counter	0x00
0x00 5347		TIM6_PSCR	TIM6 prescaler register	0x00
0x00 5348		TIM6_ARR	TIM6 auto-reload register	0xFF

Table 15. Option byte description (continued)

Option byte no.	Description
OPT4	**EXTCLK: External clock selection** 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: Auto-wakeup unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0]: AWU clock prescaler 0x: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]: HSE crystal oscillator stabilization time** 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles

8.2 STM8AF6213/23/23A/26 alternate function remapping bits

Table 16. STM8AF6226 alternate function remapping bits [7:2] for 32-pin packages

Option byte number	Description(1)
OPT2	**AFR7: Alternate function remapping option 7** 0: AFR7 remapping option inactive: default alternate function (2) 1: Port C3 alternate function = = TIM1_CH1N; port C4 alternate function = TIM1_CH2N **AFR6: Alternate function remapping option 6** 0: AFR6 remapping option inactive: default alternate function (2) 1: Port D7 alternate function = TIM1_CH4. **AFR5: Alternate function remapping option 5** 0: AFR5 remapping option inactive: default alternate function (2). 1: Port D0 alternate function = CLK_CCO. **AFR4: Alternate function remapping option 4** 0: AFR4 remapping option inactive: default alternate function (2). 1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN. **AFR3: Alternate function remapping option 3** 0: AFR3 remapping option inactive: default alternate function (2) 1: Port C3 alternate function = TLI **AFR2: Alternate function remapping option 2** 0: AFR2 remapping option inactive: default alternate function (2) 1: Port C4 alternate function = AIN2; port D2 alternate function = AIN3; port D4 alternate function = LINUART_CK

1. Do not use more than one remapping option in the same port.
2. Refer to the pin description.

Figure 9. f_{CPUmax} versus V_{DD}

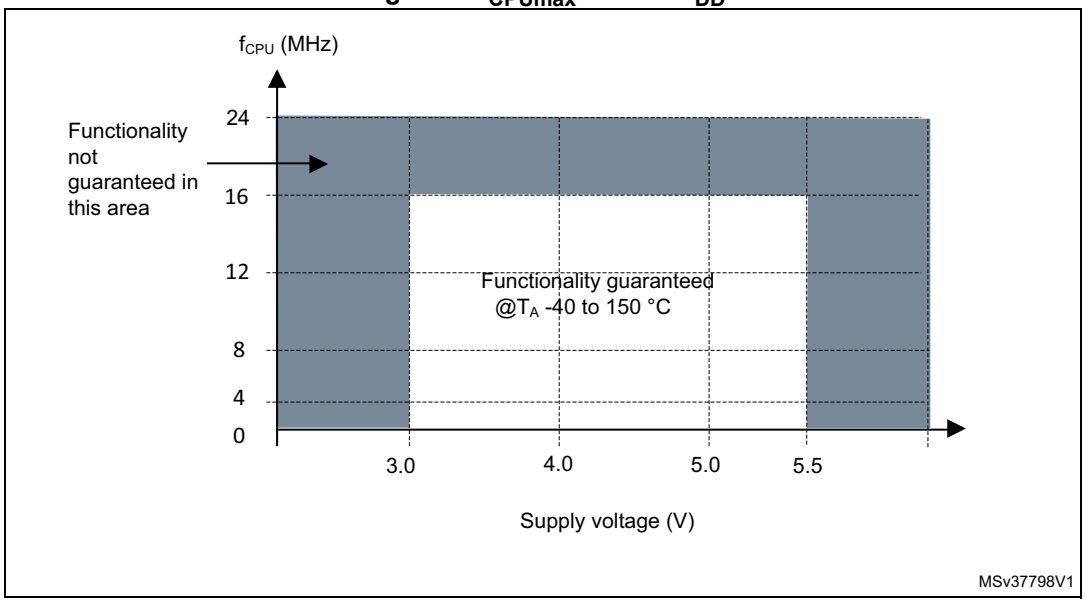


Table 27. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2(1)	-	∞	µs/V
	V_{DD} fall time rate(2)	-	2(1)	-	∞	
t_{TEMP}	Reset release delay	V_{DD} rising	-	-	1.7	ms
V_{IT+}	Power-on reset threshold(3)	-	2.6(1)	2.7	2.85	V
V_{IT-}	Brown-out reset threshold	-	2.5	2.65	2.8(1)	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70(1)	-	mV

1. Guaranteed by design.
2. Reset is always generated after a t_{TEMP} delay. The application must ensure that V_{DD} is still above the minimum operating voltage (V_{DD} min) when the t_{TEMP} delay has elapsed.
3. There is inrush current into V_{DD} present after device power on to charge C_{EXT} capacitor. This inrush energy depends from C_{EXT} capacitor value. For example, a C_{EXT} of 1µF requires Q=1 µF x 1.8V = 1.8 µC.

Total current consumption and timing in forced reset state

Table 37. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$I_{DD(R)}$	Supply current in reset state(2)	V_{DD}= 5 V	400	-	µA
		V_{DD}= 3.3 V	300	-	
$t_{RESETBL}$	Reset pin release to vector fetch	-	-	150	µs

1. Guaranteed by design.
2. Characterized with all I/Os tied to V_{SS}.

Current consumption for on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU} = f_{MASTER} = 16 MHz, V_{DD} = 5 V

Table 38. Peripheral current consumption

Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)	210	µA
$I_{DD(TIM5)}$	TIM5 supply current(1)	130	
$I_{DD(TIM6)}$	TIM6 supply current(1)	50	
$I_{DD(UART1)}$	LINUART supply current(2)	120	
$I_{DD(SPI)}$	SPI supply current(2)	45	
$I_{DD(I2C)}$	I2C supply current(2)	65	
$I_{DD(ADC1)}$	ADC1 supply current(3)	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions. Not tested in production.

Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

Figure 11. Typ $I_{DD(RUN)}$ vs. V_{DD} HSE user external clock, f_{CPU} = 16 MHz

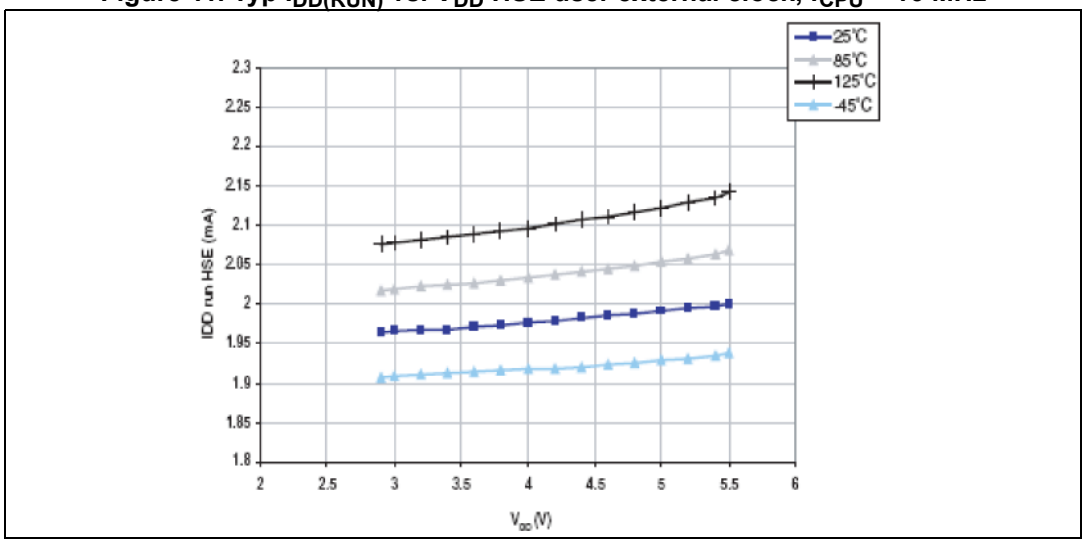
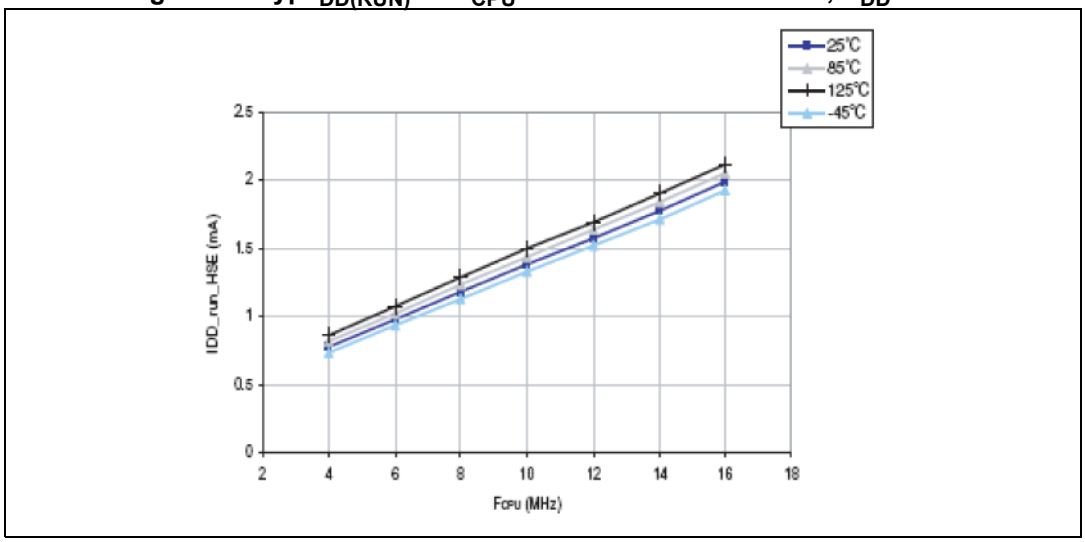


Figure 12. Typ $I_{DD(RUN)}$ vs. f_{CPU} HSE user external clock, V_{DD} = 5 V



HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 40. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high-speed oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	220	-	kΩ
$C^{(1)}$	Recommended load capacitance(2)	-	-	-	20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz	-	-	6 (startup) 1.6 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} = 16 MHz	-	-	6 (startup) 1.2 (stabilized)(3)	
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. C is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value. Refer to the crystal manufacturer for more details.
3. Guaranteed by characterization results.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) until a stabilized 16 MHz oscillation is reached. The value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 18. HSE oscillator circuit diagram

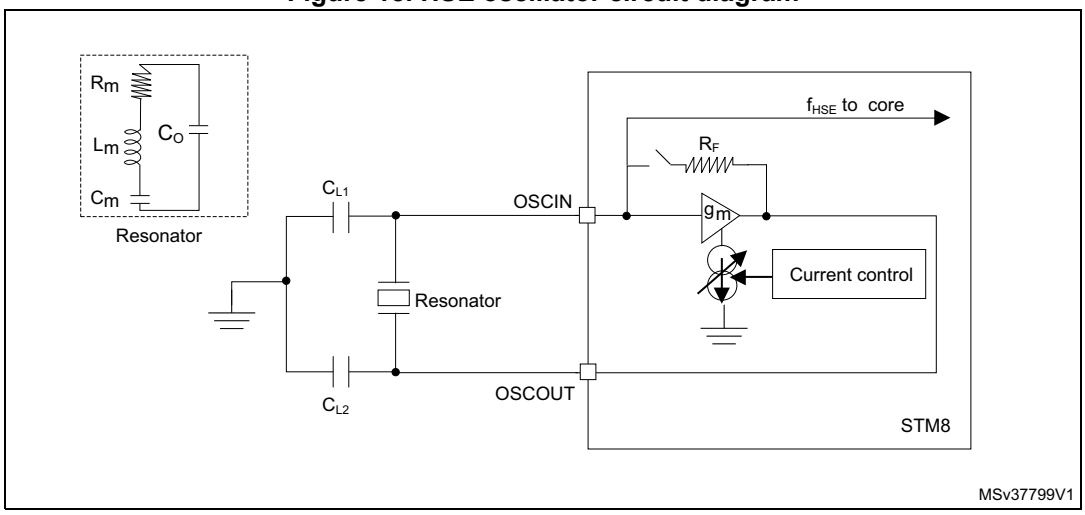


Figure 21. Typical pull-up current I_{pu} vs V_{DD} @ 4 temperatures

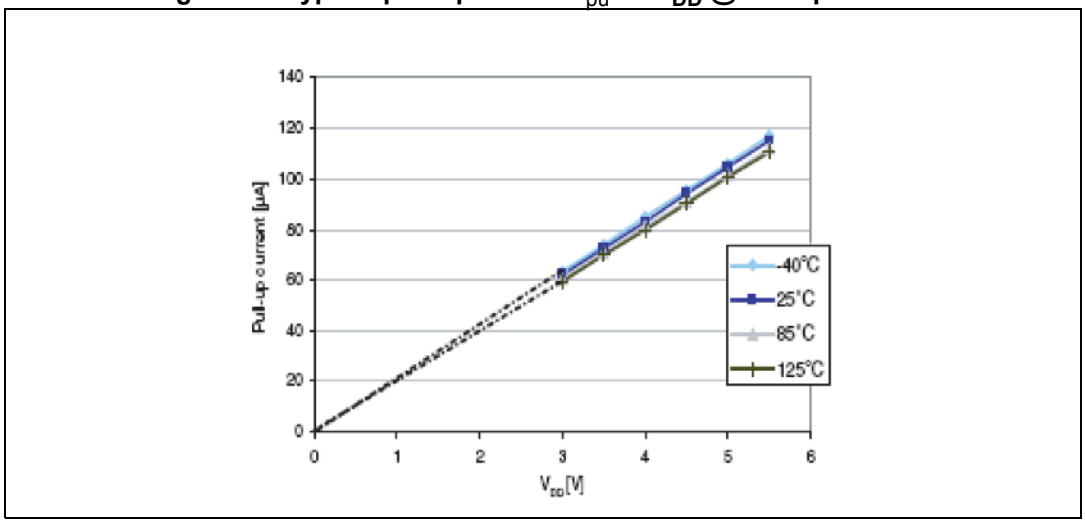


Table 48. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	2.0	V
	Output low level with 4 pins sunk	I_{IO} = 4 mA, V_{DD} = 3.3 V	-	1.0(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	2.8	-	
	Output high level with 4 pins sourced	I_{IO} = 4 mA, V_{DD} = 3.3 V	2.1(1)	-	

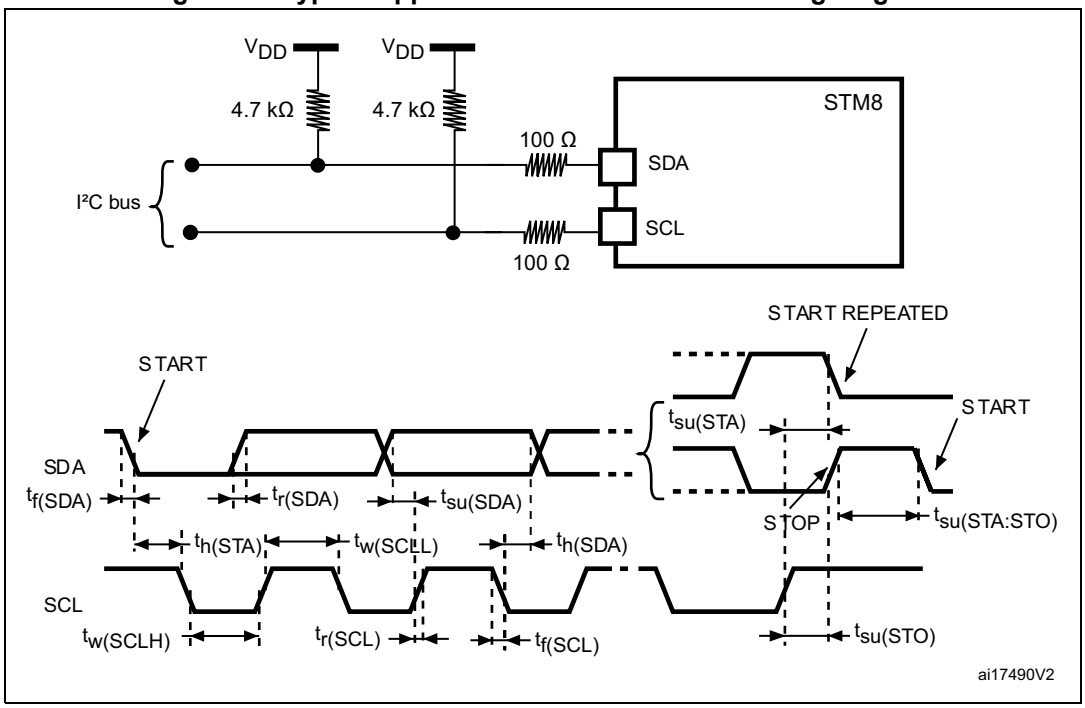
1. Guaranteed by characterization results.

Table 49. Output driving current (true open drain ports)

Symbol	Parameter	Conditions	Max	Unit
V_{OL}	Output low level with 2 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	1.0	V
		I_{IO} = 10 mA, V_{DD} = 3.3 V	1.5(1)	
		I_{IO} = 20 mA, V_{DD} = 5 V	2.0(1)	

1. Guaranteed by characterization results.

Figure 39. Typical application with I2C bus and timing diagram



1. Measurement points are made at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}.

9.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **FESD**: Functional electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see the application note reference AN1015).

Table 57. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 61000-4-2	2/B(1)
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}= 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 61000-4-4	4/A

1. Data obtained with HSI clock configuration, after applying hardware recommendations described in AN2860 (EMC guidelines for STM8S microcontrollers).

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage (applied to each power supply pin),
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 60. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = 25 °C	A
		T_A = 85 °C	
		T_A = 125 °C	
		T_A = 150 °C	

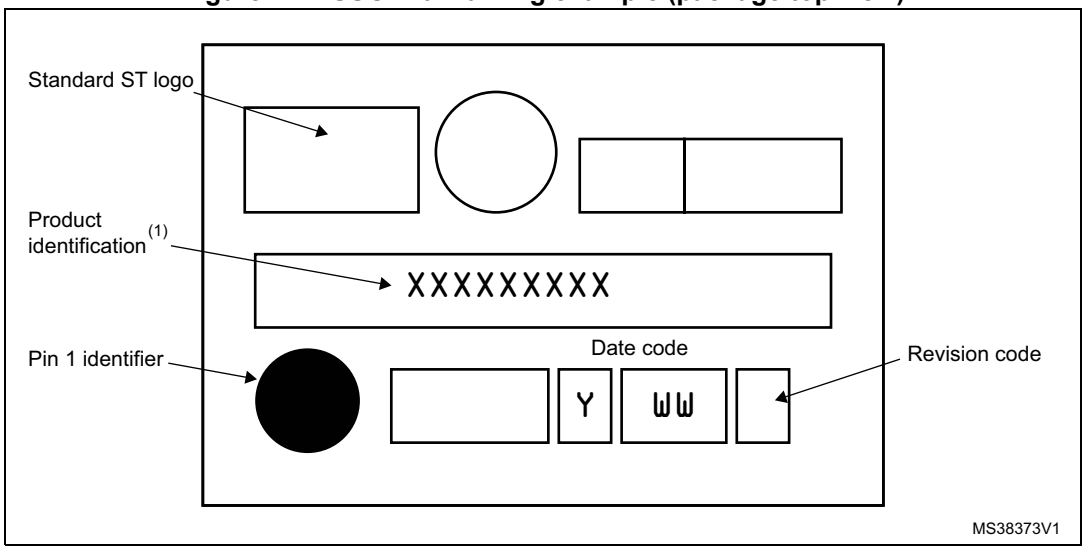
1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

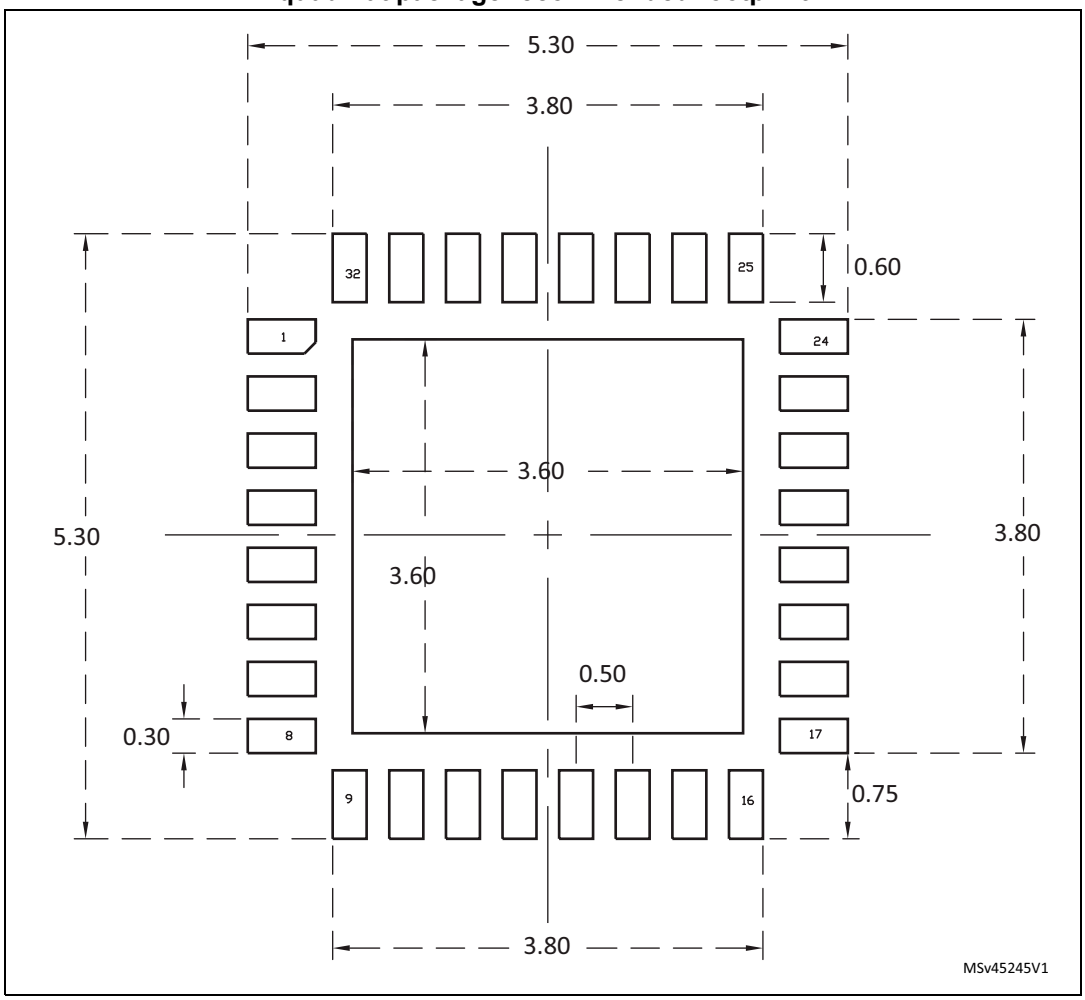
Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 47. TSSOP20 marking example (package top view)



1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Figure 49. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.