Infineon Technologies - MB96F313ASBPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

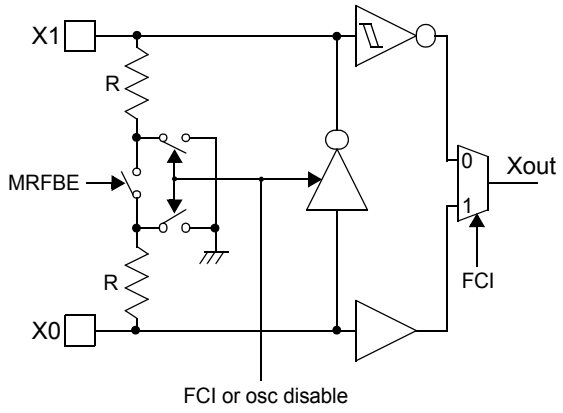
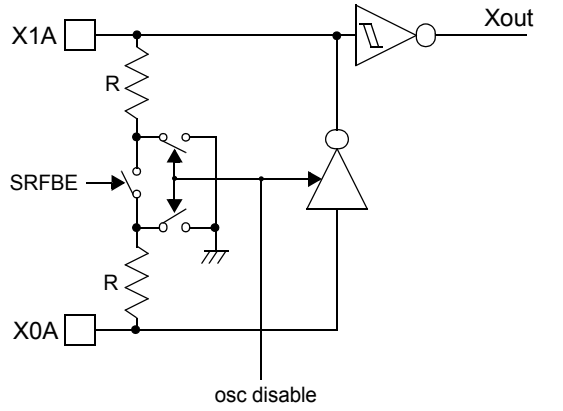
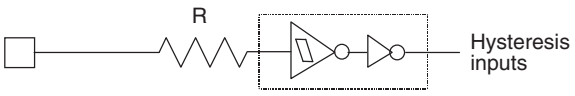
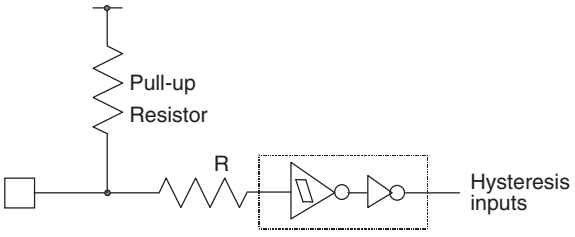
Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	36
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f313asbpmc-gse2

4. Pin Function Description

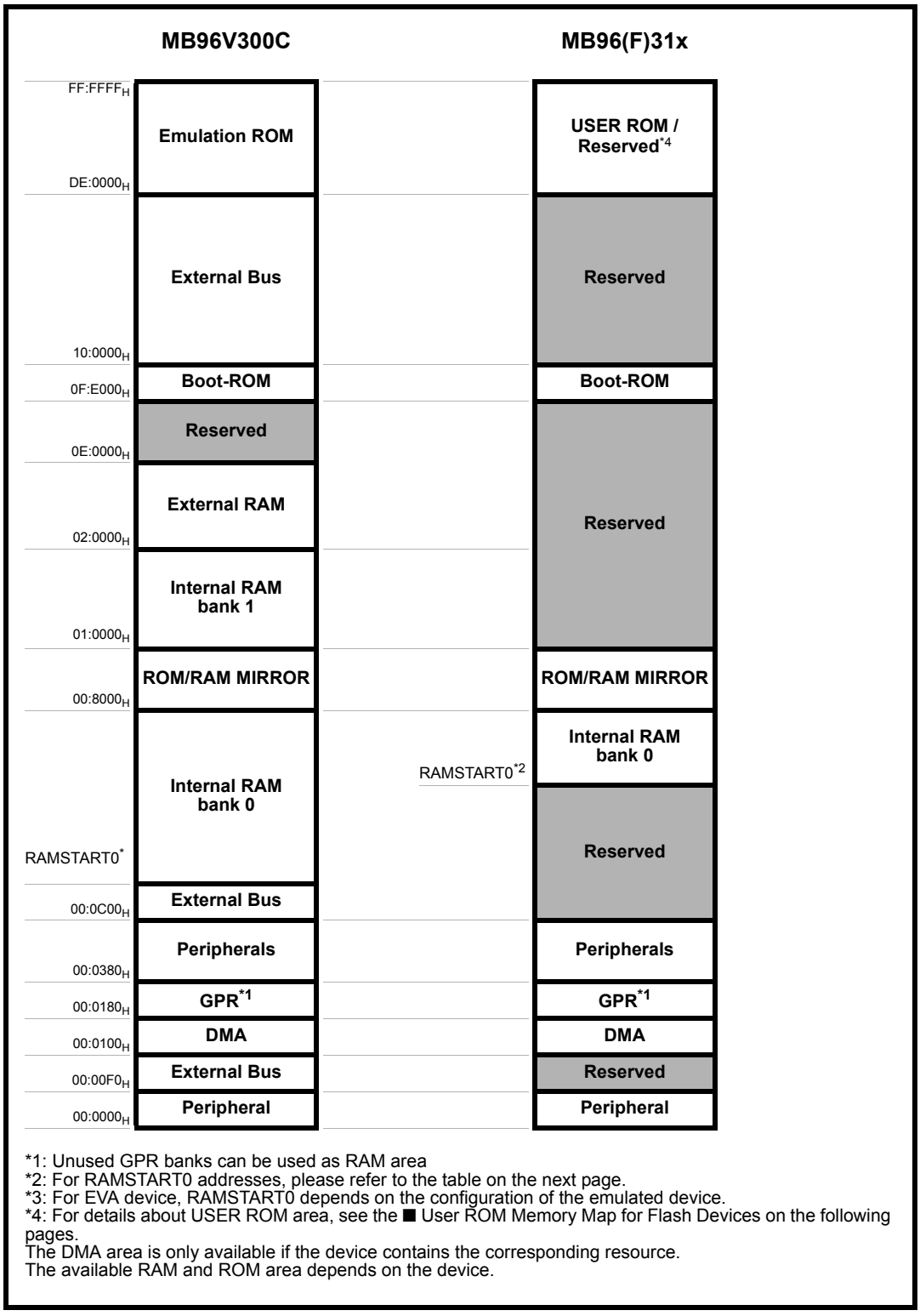
Pin Function description (1 of 2)

Pin name	Feature	Description
ADTG_R	ADC	Relocated A/D converter trigger input
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TINn_R	Reload Timer	Relocated Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TOTn_R	Reload Timer	Relocated Reload Timer n output

6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: • Programmable feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled
C		• Mask ROM and EVA device: CMOS Hysteresis input pin • Flash device: CMOS input pin
E		• CMOS Hysteresis input pin • Pull-up resistor value: approx. 50 kΩ

7. Memory Map



*1: Unused GPR banks can be used as RAM area
*2: For RAMSTART0 addresses, please refer to the table on the next page.
*3: For EVA device, RAMSTART0 depends on the configuration of the emulated device.
*4: For details about USER ROM area, see the ■ User ROM Memory Map for Flash Devices on the following pages.
The DMA area is only available if the device contains the corresponding resource.
The available RAM and ROM area depends on the device.

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD[2:0] = 010)

MB96F31x		
Pin number	**USART Number**	**Normal function**
LQFP-48		
7	USART2	SIN2
8		SOT2
9		SCK2
20	USART7	SIN7_R
19		SOT7_R
18		SCK7_R
22	USART8	SIN8_R
21		SOT8_R
23		SCK8_R

Note: If a Flash programmer and its software needs to use a handshaking pin, Cypress suggests to the tool vendor to support at least port P00_1 on pin 19.
If handshaking is used by the tool but P00_1 is not available in customer's application, Cypress suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

I/O map MB96(F)315x (Sheet 5 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000097_H	PPG3 - Control status register High	PCNH3		R/W
000098_H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099_H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
$00009A_H$	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
$00009B_H$	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
$00009C_H$	PPG4 - Timer register		PTMR4	R
$00009D_H$	PPG4 - Timer register			R
$00009E_H$	PPG4 - Period setting register		PCSR4	W
$00009F_H$	PPG4 - Period setting register			W
$0000A0_H$	PPG4 - Duty cycle register		PDUT4	W
$0000A1_H$	PPG4 - Duty cycle register			W
$0000A2_H$	PPG4 - Control status register Low	PCNL4	PCN4	R/W
$0000A3_H$	PPG4 - Control status register High	PCNH4		R/W
$0000A4_H$-$0000D3_H$	Reserved			-
$0000D4_H$	USART2 - Serial Mode Register	SMR2		R/W
$0000D5_H$	USART2 - Serial Control Register	SCR2		R/W
$0000D6_H$	USART2 - TX Register	TDR2		W
$0000D6_H$	USART2 - RX Register	RDR2		R
$0000D7_H$	USART2 - Serial Status	SSR2		R/W
$0000D8_H$	USART2 - Control/Com. Register	ECCR2		R/W
$0000D9_H$	USART2 - Ext. Status Register	ESCR2		R/W
$0000DA_H$	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
$0000DB_H$	USART2 - Baud Rate Generator Register High	BGRH2		R/W
$0000DC_H$	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
$0000DD_H$-$0000FF_H$	Reserved			-
000100_H	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101_H	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102_H	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103_H	DMA0 - DMA control register	DMACS0		R/W

I/O map MB96(F)315x (Sheet 11 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000435_H	I/O Port P05 - Data Direction Register	DDR05		R/W
000436_H	I/O Port P06 - Data Direction Register	DDR06		R/W
000437_H	I/O Port P07 - Data Direction Register	DDR07		R/W
000438_H-000443_H	Reserved			-
000444_H	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445_H	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446_H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447_H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448_H	Reserved			-
000449_H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
$00044A_H$	I/O Port P06 - Port Input Enable Register	PIER06		R/W
$00044B_H$	I/O Port P07 - Port Input Enable Register	PIER07		R/W
$00044C_H$-000457_H	Reserved			-
000458_H	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459_H	I/O Port P01 - Port Input Level Register	PILR01		R/W
$00045A_H$	I/O Port P02 - Port Input Level Register	PILR02		R/W
$00045B_H$	I/O Port P03 - Port Input Level Register	PILR03		R/W
$00045C_H$	Reserved			-
$00045D_H$	I/O Port P05 - Port Input Level Register	PILR05		R/W
$00045E_H$	I/O Port P06 - Port Input Level Register	PILR06		R/W
$00045F_H$	I/O Port P07 - Port Input Level Register	PILR07		R/W
000460_H-$00046B_H$	Reserved			-
$00046C_H$	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
$00046D_H$	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
$00046E_H$	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
$00046F_H$	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470_H	Reserved			-
000471_H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472_H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W

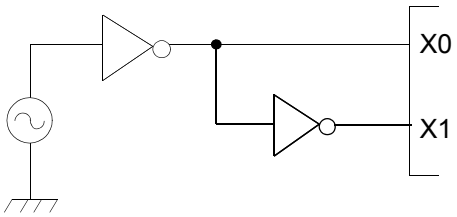
I/O map MB96(F)315x (Sheet 17 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000588_H-000597_H	Reserved			-
000598_H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599_H	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
$00059A_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
$00059B_H$	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
$00059C_H$	PPG12 - Timer register		PTMR12	R
$00059D_H$	PPG12 - Timer register			R
$00059E_H$	PPG12 - Period setting register		PCSR12	W
$00059F_H$	PPG12 - Period setting register			W
$0005A0_H$	PPG12 - Duty cycle register		PDUT12	W
$0005A1_H$	PPG12 - Duty cycle register			W
$0005A2_H$	PPG12 - Control status register Low	PCNL12	PCN12	R/W
$0005A3_H$	PPG12 - Control status register High	PCNH12		R/W
$0005A4_H$-$0005AB_H$	Reserved			-
$0005AC_H$	PPG14 - Timer register		PTMR14	R
$0005AD_H$	PPG14 - Timer register			R
$0005AE_H$	PPG14 - Period setting register		PCSR14	W
$0005AF_H$	PPG14 - Period setting register			W
$0005B0_H$	PPG14 - Duty cycle register		PDUT14	W
$0005B1_H$	PPG14 - Duty cycle register			W
$0005B2_H$	PPG14 - Control status register Low	PCNL14	PCN14	R/W
$0005B3_H$	PPG14 - Control status register High	PCNH14		R/W
$0005B4_H$-$0005BB_H$	Reserved			-
$0005BC_H$	PPG19-PPG16 - General Control register 1 Low	GCN1L4	GCN14	R/W
$0005BD_H$	PPG19-PPG16 - General Control register 1 High	GCN1H4		R/W
$0005BE_H$	PPG19-PPG16 - General Control register 2 Low	GCN2L4	GCN24	R/W
$0005BF_H$	PPG19-PPG16 - General Control register 2 High	GCN2H4		R/W
$0005C0_H$	PPG16 - Timer register		PTMR16	R
$0005C1_H$	PPG16 - Timer register			R

I/O map MB96(F)315x (Sheet 19 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0005E0_H$-$00065F_H$	Reserved			-
000660_H	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661_H	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662_H	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663_H	Peripheral Resource Relocation Register 13	PRRR13		W
000664_H-$0008FF_H$	Reserved			-
000900_H	CAN2 - Control register Low	CTRLRL2	CTRLR2	R/W
000901_H	CAN2 - Control register High (reserved)	CTRLRH2		R
000902_H	CAN2 - Status register Low	STATRL2	STATR2	R/W
000903_H	CAN2 - Status register High (reserved)	STATRH2		R
000904_H	CAN2 - Error Counter Low (Transmit)	ERRCNTL2	ERRCNT2	R
000905_H	CAN2 - Error Counter High (Receive)	ERRCNTH2		R
000906_H	CAN2 - Bit Timing Register Low	BTRL2	BTR2	R/W
000907_H	CAN2 - Bit Timing Register High	BTRH2		R/W
000908_H	CAN2 - Interrupt Register Low	INTRL2	INTR2	R
000909_H	CAN2 - Interrupt Register High	INTRH2		R
$00090A_H$	CAN2 - Test Register Low	TESTRL2	TESTR2	R/W
$00090B_H$	CAN2 - Test Register High (reserved)	TESTRH2		R
$00090C_H$	CAN2 - BRP Extension register Low	BRPERL2	BRPER2	R/W
$00090D_H$	CAN2 - BRP Extension register High (reserved)	BRPERH2		R
$00090E_H$-$00090F_H$	Reserved			-
000910_H	CAN2 - IF1 Command request register Low	IF1CREQL2	IF1CREQ2	R/W
000911_H	CAN2 - IF1 Command request register High	IF1CREQH2		R/W
000912_H	CAN2 - IF1 Command Mask register Low	IF1CMSKL2	IF1CMSK2	R/W
000913_H	CAN2 - IF1 Command Mask register High (reserved)	IF1CMSKH2		R
000914_H	CAN2 - IF1 Mask 1 Register Low	IF1MSK1L2	IF1MSK12	R/W
000915_H	CAN2 - IF1 Mask 1 Register High	IF1MSK1H2		R/W
000916_H	CAN2 - IF1 Mask 2 Register Low	IF1MSK2L2	IF1MSK22	R/W
000917_H	CAN2 - IF1 Mask 2 Register High	IF1MSK2H2		R/W

2. Opposite phase external clock
   - When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



13.4 Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

13.5 Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.6 Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

13.7 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

13.8 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.9 Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as AV_{CC} = V_{CC}, AV_{SS} = AVRH = AVRL = V_{SS}.

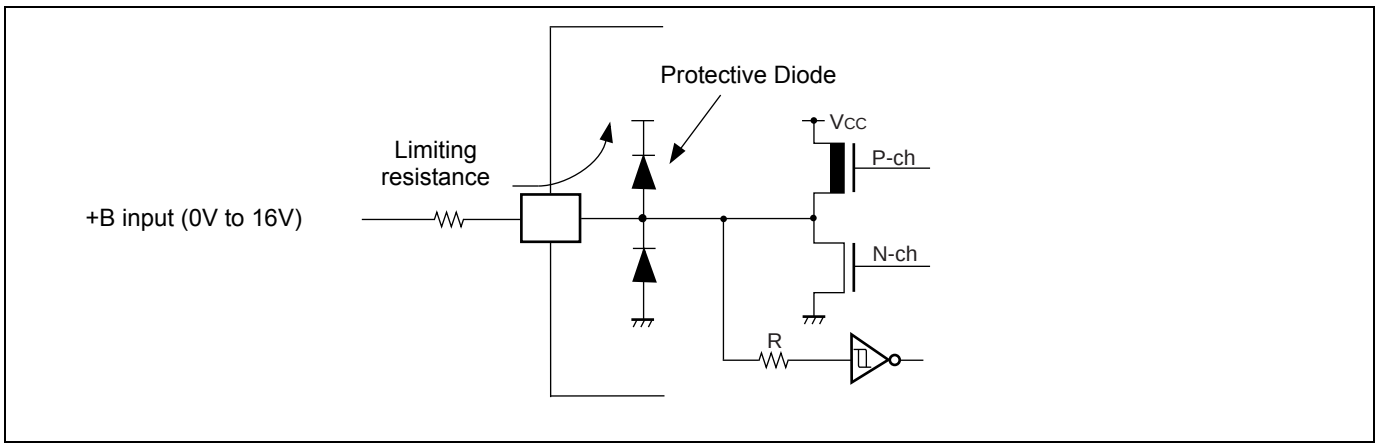
13.10 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50μs from 0.2 V to 2.7 V.

*1: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

*2: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

*3:
- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).
- Sample recommended circuits:



*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “3. DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.
I_A is the analog current consumption into AV_{CC}.

*5: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*6: Please contact Cypress for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.2 Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	3.5	4.7	15	μF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.
Users considering application outside the listed conditions are advised to contact their representatives beforehand.

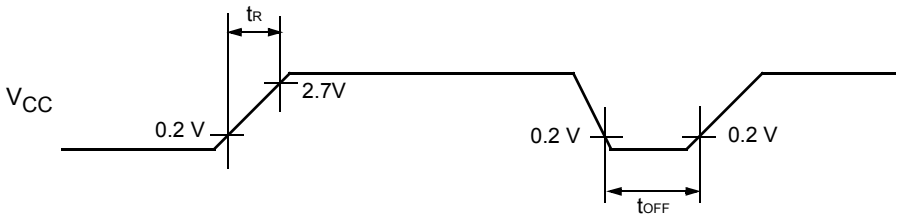
(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value		Unit	Remarks
				Typ	Max		
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped)	+25°C	1.3	1.8	mA	
			+125°C	1.9	4.8		
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.11	0.2	mA	
			+125°C	0.63	3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.08	0.15	mA	
			+125°C	0.6	2.9		
Power supply current in Timer modes*	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.1	0.2	mA	
			+125°C	0.63	3		
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.07	0.15	mA	
			+125°C	0.6	2.9		
	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.06	0.15	mA	
			+125°C	0.56	2.95		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.03	0.1	mA	
			+125°C	0.53	2.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.035	0.1	mA	
			+125°C	0.53	2.85		

Power On Reset timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



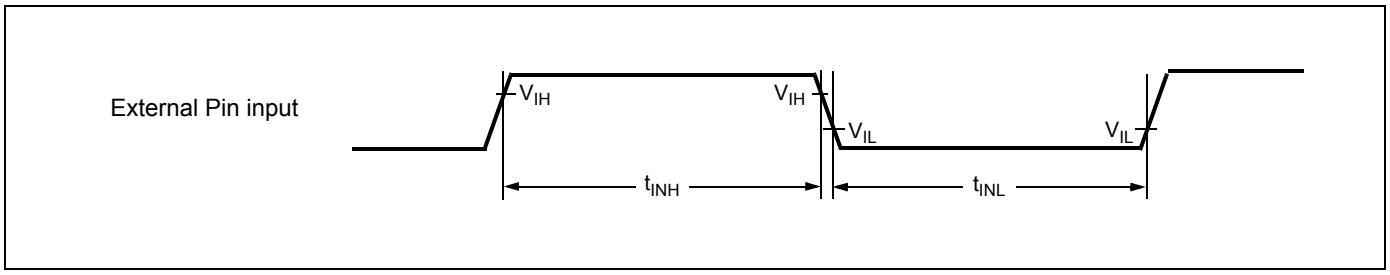
If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

External Input timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn(_R)	—	200	—	ns	External Interrupt
		NMI					NMI
		Pnn_m		$2*t_{CLKP1}$ + 200 ($t_{CLKP1}=1/f_{CLKP1}$)	—	ns	General Purpose IO
		TINn					Reload Timer
		TTGn(_R)					PPG Trigger input
		ADTG_R					AD Converter Trigger
		INn					Input Capture

Note : Relocated Resource Inputs have same characteristics



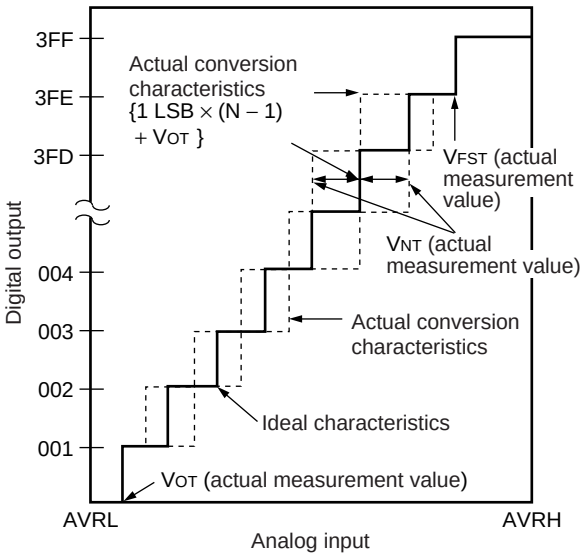
14.5 Analog Digital Converter

(T_A = -40 °C to +125 °C, 3.0 V ≤ AVRH - AVRL, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

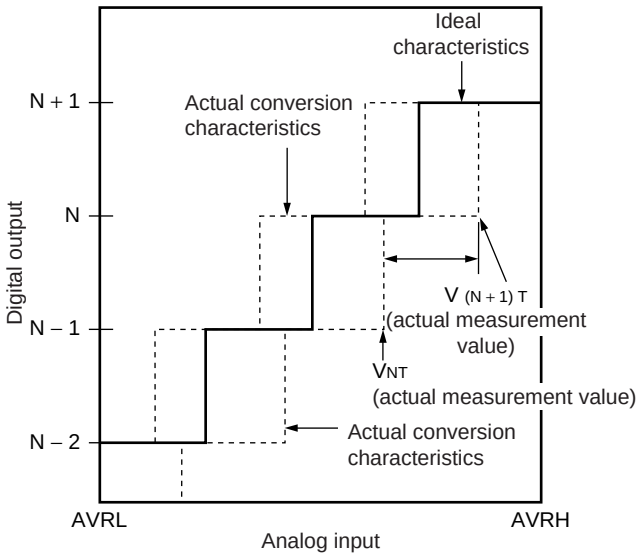
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-	-	± 3	LSB	
Nonlinearity error	-	-	-	-	± 2.5	LSB	
Differential nonlinearity error	-	-	-	-	± 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	AVRL - 1.5 LSB	AVRL+ 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale transition voltage	V_{FST}	ANn	AVRH - 3.5 LSB	AVRH - 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	-	-	1.0	-	16,500	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.0	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Analog input leakage current (during conversion)	I_{AIN}	ANn	-1	-	+1	µA	T_A ≤ 105 °C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
			-1.2	-	+1.2	µA	105 °C < T_A ≤ 125 °C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH	0.75 AVcc	-	AVcc	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AVcc	-	2.5	5	mA	A/D Converter active
	I_{AH}	AVcc	-	-	5	µA	A/D Converter not operated
Reference voltage current	I_R	AVRH/AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/AVRL	-	-	5	µA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

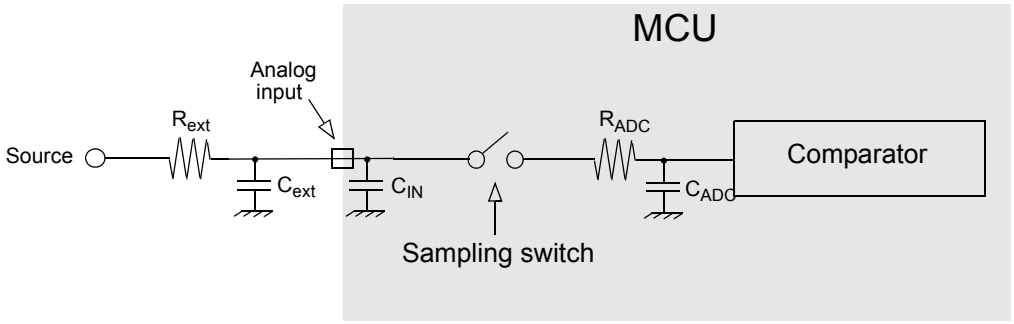
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H."
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$."

Accuracy and setting of the A/D Converter sampling time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{cc} voltage level. The following replacement model can be used for the calculation:



R_{ext}: external driving impedance

C_{ext}: capacitance of PCB at A/D converter input

C_{IN}: capacitance of MCU input pin: 15pF (max)

R_{ADC}: resistance within MCU: 2.6kΩ (max) for $4.5V \le AV_{cc} \le 5.5V$
12kΩ (max) for $3.0V \le AV_{cc} < 4.5V$

C_{ADC}: sampling capacitance within MCU: 10pF (max)

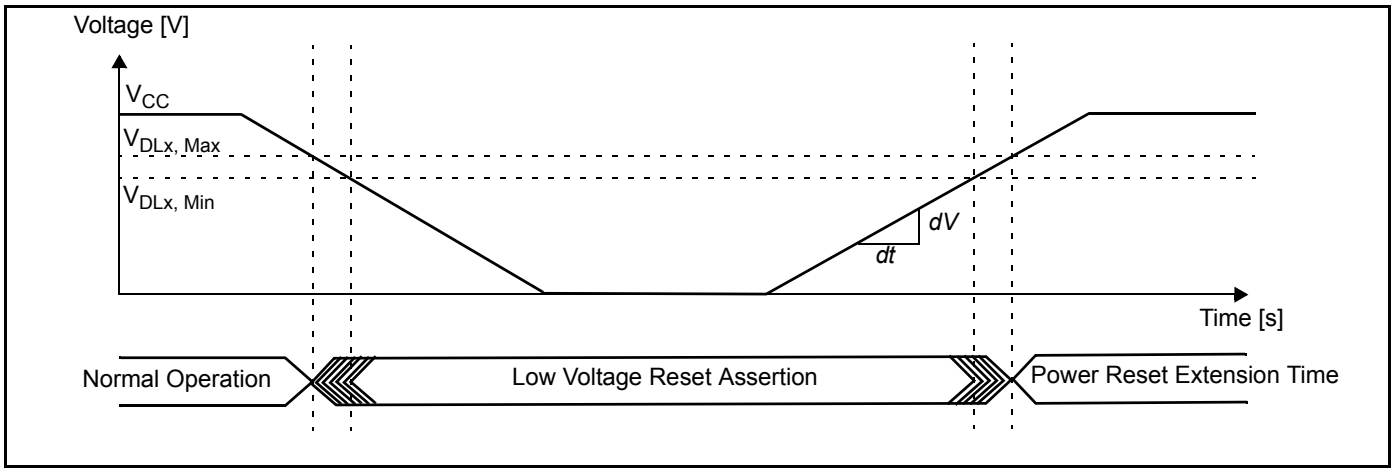
The sampling time should be set to minimum "7τ". The following approximation formula for the replacement model above can be used:

$$T_{samp}\ [min] = 7 \times (R_{ext} \times (C_{ext} + C_{IN}) + (R_{ext} + R_{ADC}) \times C_{ADC})$$

- Do not select a sampling time below the absolute minimum permitted value ($0.5\mu s$ for $4.5V \le AV_{cc} \le 5.5V$; $1.2\ \mu s$ for $3.0V \le AV_{cc} < 4.5V$).
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin. In this case the internal sampling capacitance C_{ADC} will be charged out of this external capacitance.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current I_{IL} (static current before the sampling switch) or the analog input leakage current I_{AIN} (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current I_{IL} cannot be compensated by an external capacitor.
- The accuracy gets worse as |AVRH - AVRL| becomes smaller.

Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



14.7 FLASH memory program/erase characteristics

(T_A = -40°C to 105°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Without erasure pre-programming time
Chip erase time	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Word (16-bit width) programming time	-	23	370	us	Without overhead time for submitting write command
Program/Erase cycle	10000	-	-	cycle	
Flash data retention time	20	-	-	year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

17. Ordering Information

MCU with CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F313YSB PMC-GSE2	Flash A (96KB)	No	Yes	48 pins Plastic LQFP (FPT-48P-M26)
MB96F313RSB PMC-GSE1			No	
MB96F313RSB PMC-GSE2			No	
MB96F313YWB PMC-GSE2		Yes	Yes	
MB96F313RWB PMC-GSE2			No	
MB96F315YSB PMC-GSE2	Flash A (160KB)	No	Yes	
MB96F315RSB PMC-GSE1			No	
MB96F315RSB PMC-GSE2			No	
MB96F315YWB PMC-GSE2		Yes	Yes	
MB96F315RWB PMC-GSE2			No	
MB96V300CRB-ES (for evaluation)	Emulated by ext. RAM	Yes	No	416 pin Plastic BGA (BGA-416P-M02)

MCU without CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F313ASB PMC-GSE2	Flash A (96KB)	No	No	48 pins Plastic LQFP (FPT-48P-M26)
MB96F313AWB PMC-GSE2		Yes		
MB96F315ASB PMC-GSE2	Flash A (160KB)	No		
MB96F315AWB PMC-GSE2		Yes		