Infineon Technologies - MB96F313RSBPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	36
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f313rsbpmc-gse2

USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device

A/D converter

- SAR-type
- 10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$,$1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, falling edge or rising & falling edge sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with 16-bit I/O Timer occurs
- A pair of compare registers can be used to generate an output signal.

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer underflow as clock input
- Can be triggered by software or reload timer

Real Time Clock

- Can be clocked either from sub oscillator (devices with part number suffix “W”), main oscillator or from the RC oscillator
- Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge sensitive or level sensitive
- Interrupt mask and pending bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

Non Maskable Interrupt

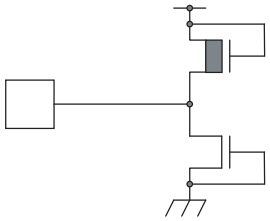
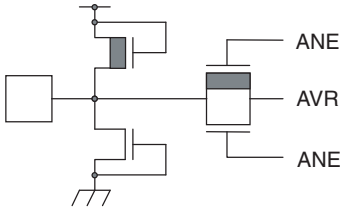
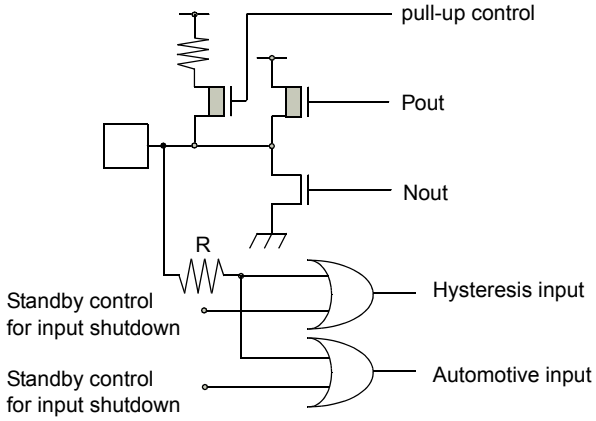
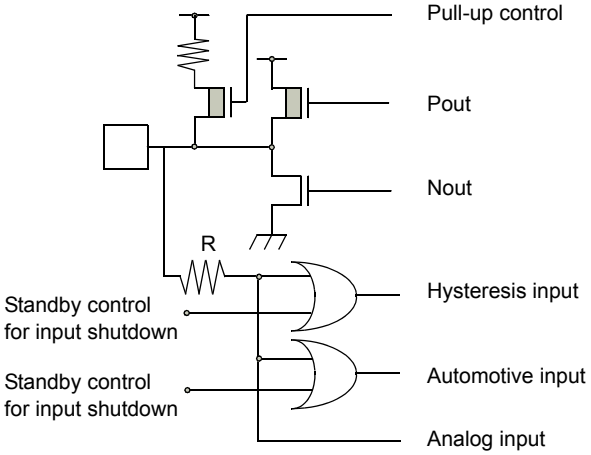
- Disabled after reset
- Once enabled, can not be disabled other than by reset.
- Level high or level low sensitive
- Pin shared with external interrupt 0.

I/O Ports

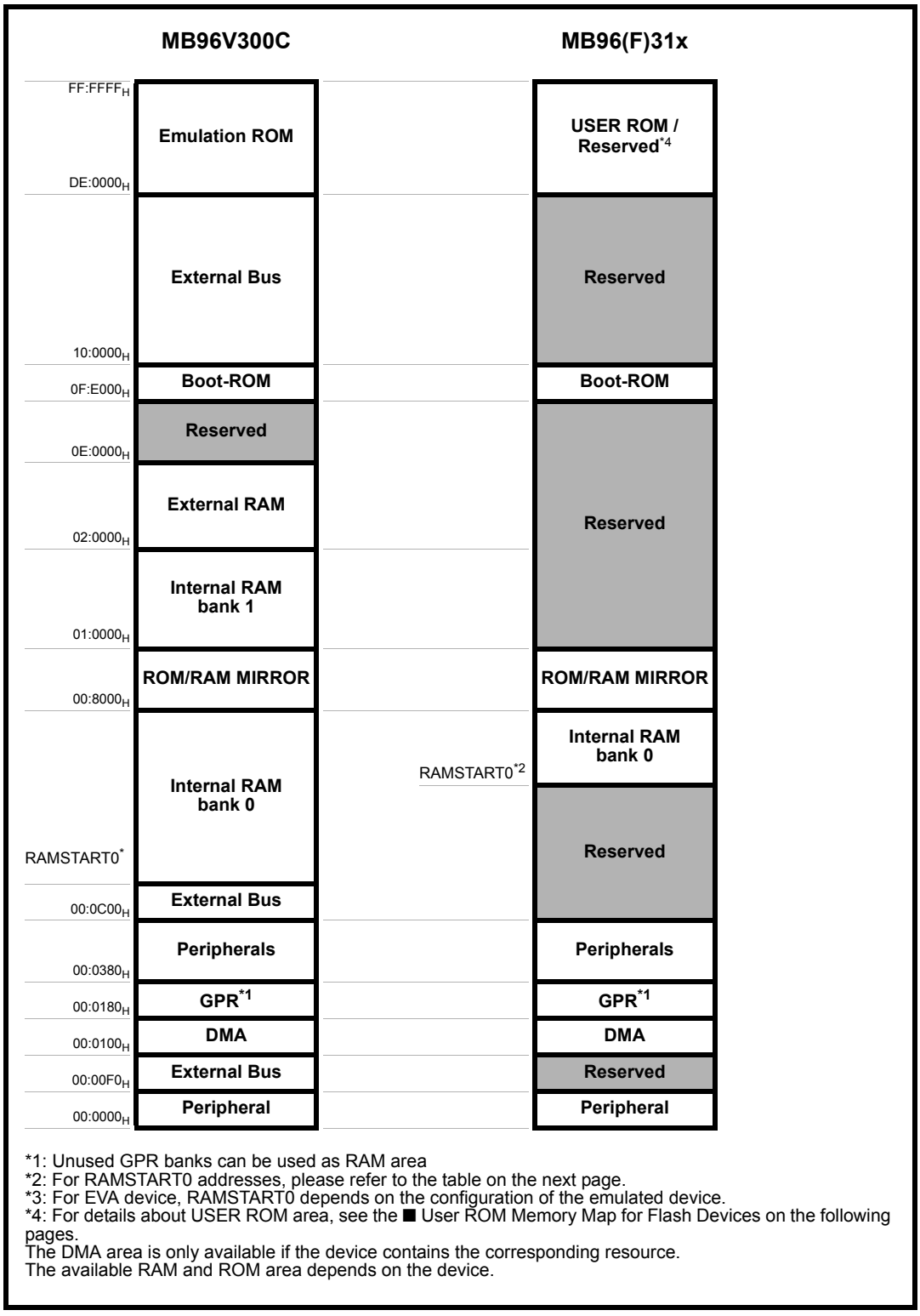
- Virtually all external pins can be used as general purpose I/O
- All push-pull outputs
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL
- Bit-wise programmable pull-up resistor
- Bit-wise programmable output driving strength for EMI optimization

Packages

- 48-pin plastic LQFP M26

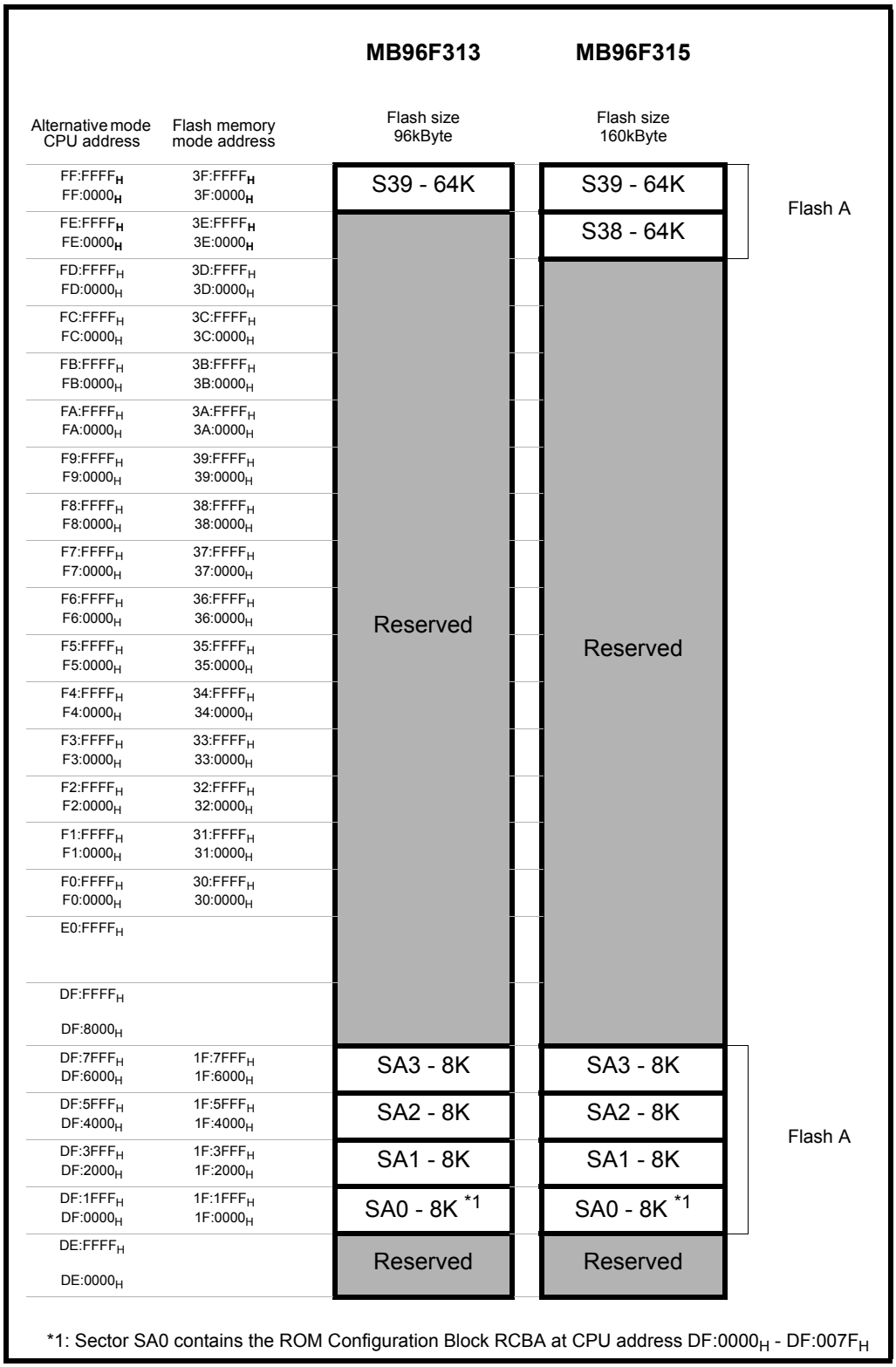
Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pin AVRH
H		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • CMOS hysteresis input with input shutdown function • Automotive input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.
I		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • CMOS hysteresis input with input shutdown function • Automotive input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. • Analog input

7. Memory Map



*1: Unused GPR banks can be used as RAM area
*2: For RAMSTART0 addresses, please refer to the table on the next page.
*3: For EVA device, RAMSTART0 depends on the configuration of the emulated device.
*4: For details about USER ROM area, see the ■ User ROM Memory Map for Flash Devices on the following pages.
The DMA area is only available if the device contains the corresponding resource.
The available RAM and ROM area depends on the device.

9. User ROM Memory Map for Flash Devices



*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

I/O map MB96(F)315x (Sheet 6 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000104_H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105_H	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106_H	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107_H	DMA0 - Data counter high byte	DCTH0		R/W
000108_H	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109_H	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
$00010A_H$	DMA1 - Buffer address pointer high byte	BAPH1		R/W
$00010B_H$	DMA1 - DMA control register	DMACS1		R/W
$00010C_H$	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W
$00010D_H$	DMA1 - I/O register address pointer high byte	IOAH1		R/W
$00010E_H$	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
$00010F_H$	DMA1 - Data counter high byte	DCTH1		R/W
000110_H	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111_H	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112_H	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113_H	DMA2 - DMA control register	DMACS2		R/W
000114_H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115_H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116_H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117_H	DMA2 - Data counter high byte	DCTH2		R/W
000118_H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119_H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
$00011A_H$	DMA3 - Buffer address pointer high byte	BAPH3		R/W
$00011B_H$	DMA3 - DMA control register	DMACS3		R/W
$00011C_H$	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
$00011D_H$	DMA3 - I/O register address pointer high byte	IOAH3		R/W
$00011E_H$	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
$00011F_H$	DMA3 - Data counter high byte	DCTH3		R/W
000120_H-$00017F_H$	Reserved			-

I/O map MB96(F)315x (Sheet 14 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0004ED_H$	CAL - Duration Timer Data Register High	CUTDH		R/W
$0004EE_H$	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
$0004EF_H$	CAL - Calibration Timer Register 2 High	CUTR2H		R
$0004F0_H$	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
$0004F1_H$	CAL - Calibration Timer Register 1 High	CUTR1H		R
$0004F2_H$-$0004F9_H$	Reserved			-
$0004FA_H$	RLT - Timer input select (for Cascading)	TMISR		R/W
$0004FB_H$-$0004FF_H$	Reserved			-
000500_H	FRT2 - Data register of free-running timer		TCDT2	R/W
000501_H	FRT2 - Data register of free-running timer			R/W
000502_H	FRT2 - Control status register of free-running timer Low	TCCSL2	TCCS2	R/W
000503_H	FRT2 - Control status register of free-running timer High	TCCSH2		R/W
000504_H	FRT3 - Data register of free-running timer		TCDT3	R/W
000505_H	FRT3 - Data register of free-running timer			R/W
000506_H	FRT3 - Control status register of free-running timer Low	TCCSL3	TCCS3	R/W
000507_H	FRT3 - Control status register of free-running timer High	TCCSH3		R/W
000508_H-000513_H	Reserved			-
000514_H	ICU8/ICU9 - Control Status Register	ICS89		R/W
000515_H	ICU8/ICU9 - Edge Register	ICE89		R/W
000516_H	ICU8 - Capture Register Low	IPCPL8	IPCP8	R
000517_H	ICU8 - Capture Register High	IPCPH8		R
000518_H	ICU9 - Capture Register Low	IPCPL9	IPCP9	R
000519_H	ICU9 - Capture Register High	IPCPH9		R
$00051A_H$	ICU10/ICU11 - Control Status Register	ICS1011		R/W
$00051B_H$	ICU10/ICU11 - Edge Register	ICE1011		R/W
$00051C_H$	ICU10 - Capture Register Low	IPCPL10	IPCP10	R
$00051D_H$	ICU10 - Capture Register High	IPCPH10		R
$00051E_H$	ICU11 - Capture Register Low	IPCPL11	IPCP11	R
$00051F_H$	ICU11 - Capture Register High	IPCPH11		R

I/O map MB96(F)315x (Sheet 15 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000520_H-$00053D_H$	Reserved			-
$00053E_H$	USART7 - Serial Mode Register	SMR7		R/W
$00053F_H$	USART7 - Serial Control Register	SCR7		R/W
000540_H	USART7 - Serial TX Register	TDR7		W
000540_H	USART7 - Serial RX Register	RDR7		R
000541_H	USART7 - Serial Status Register	SSR7		R/W
000542_H	USART7 - Ext. Control/Com. Register	ECCR7		R/W
000543_H	USART7 - Ext. Status Com. Register	ESCR7		R/W
000544_H	USART7 - Baud Rate Generator Register Low	BGRL7	BGR7	R/W
000545_H	USART7 - Baud Rate Generator Register High	BGRH7		R/W
000546_H	USART7 - Extended Serial Interrupt Register	ESIR7		R/W
000547_H	Reserved			-
000548_H	USART8 - Serial Mode Register	SMR8		R/W
000549_H	USART8 - Serial Control Register	SCR8		R/W
$00054A_H$	USART8 - Serial TX Register	TDR8		W
$00054A_H$	USART8 - Serial RX Register	RDR8		R
$00054B_H$	USART8 - Serial Status Register	SSR8		R/W
$00054C_H$	USART8 - Ext. Control/Com. Register	ECCR8		R/W
$00054D_H$	USART8 - Ext. Status Com. Register	ESCR8		R/W
$00054E_H$	USART8 - Baud Rate Generator Register Low	BGRL8	BGR8	R/W
$00054F_H$	USART8 - Baud Rate Generator Register High	BGRH8		R/W
000550_H	USART8 - Extended Serial Interrupt Register	ESIR8		R/W
000551_H-000563_H	Reserved			-
000564_H	PPG6 - Timer register		PTMR6	R
000565_H	PPG6 - Timer register			R
000566_H	PPG6 - Period setting register		PCSR6	W
000567_H	PPG6 - Period setting register			W
000568_H	PPG6 - Duty cycle register		PDUT6	W
000569_H	PPG6 - Duty cycle register			W

I/O map MB96(F)315x (Sheet 17 of 22)

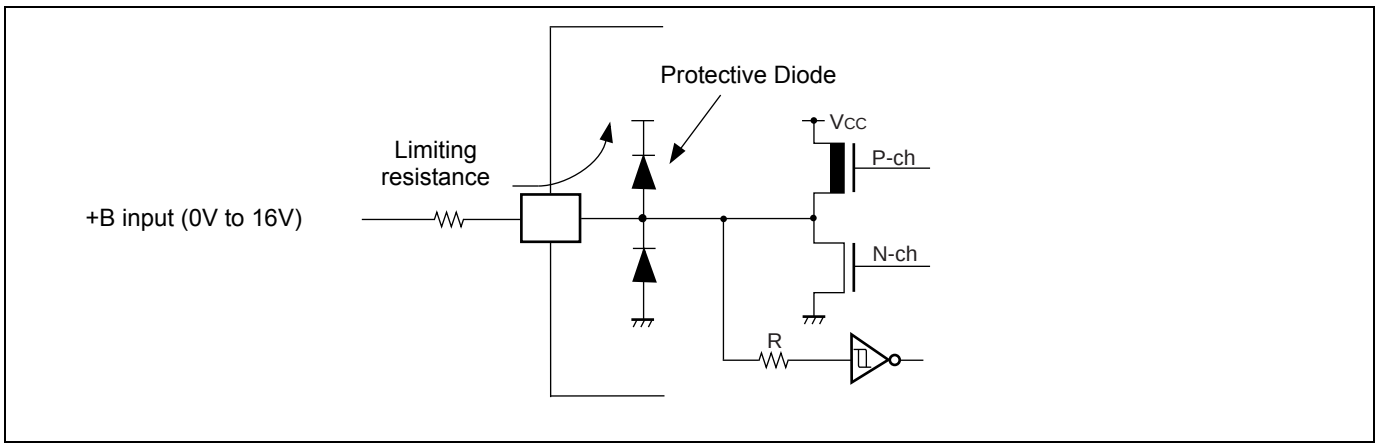
Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000588_H-000597_H	Reserved			-
000598_H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599_H	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
$00059A_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
$00059B_H$	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
$00059C_H$	PPG12 - Timer register		PTMR12	R
$00059D_H$	PPG12 - Timer register			R
$00059E_H$	PPG12 - Period setting register		PCSR12	W
$00059F_H$	PPG12 - Period setting register			W
$0005A0_H$	PPG12 - Duty cycle register		PDUT12	W
$0005A1_H$	PPG12 - Duty cycle register			W
$0005A2_H$	PPG12 - Control status register Low	PCNL12	PCN12	R/W
$0005A3_H$	PPG12 - Control status register High	PCNH12		R/W
$0005A4_H$-$0005AB_H$	Reserved			-
$0005AC_H$	PPG14 - Timer register		PTMR14	R
$0005AD_H$	PPG14 - Timer register			R
$0005AE_H$	PPG14 - Period setting register		PCSR14	W
$0005AF_H$	PPG14 - Period setting register			W
$0005B0_H$	PPG14 - Duty cycle register		PDUT14	W
$0005B1_H$	PPG14 - Duty cycle register			W
$0005B2_H$	PPG14 - Control status register Low	PCNL14	PCN14	R/W
$0005B3_H$	PPG14 - Control status register High	PCNH14		R/W
$0005B4_H$-$0005BB_H$	Reserved			-
$0005BC_H$	PPG19-PPG16 - General Control register 1 Low	GCN1L4	GCN14	R/W
$0005BD_H$	PPG19-PPG16 - General Control register 1 High	GCN1H4		R/W
$0005BE_H$	PPG19-PPG16 - General Control register 2 Low	GCN2L4	GCN24	R/W
$0005BF_H$	PPG19-PPG16 - General Control register 2 High	GCN2H4		R/W
$0005C0_H$	PPG16 - Timer register		PTMR16	R
$0005C1_H$	PPG16 - Timer register			R

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
73	$2D8_H$	OCU6	Yes	73	Output Compare Unit 6
74	$2D4_H$	OCU7	Yes	74	Output Compare Unit 7
75	$2D0_H$				Reserved
76	$2CC_H$				Reserved
77	$2C8_H$	FRT0	Yes	77	Free Running Timer 0
78	$2C4_H$	FRT1	Yes	78	Free Running Timer 1
79	$2C0_H$	FRT2	Yes	79	Free Running Timer 2
80	$2BC_H$	FRT3	Yes	80	Free Running Timer 3
81	$2B8_H$	RTC0	No	81	Real Timer Clock
82	$2B4_H$	CAL0	No	82	Clock Calibration Unit
83	$2B0_H$				Reserved
84	$2AC_H$	ADC0	Yes	84	A/D Converter
85	$2A8_H$	LINR2	Yes	85	LIN USART 2 RX
86	$2A4_H$	LINT2	Yes	86	LIN USART 2 TX
87	$2A0_H$				Reserved
88	$29C_H$				Reserved
89	298_H	LINR7	Yes	89	LIN USART 7 RX
90	294_H	LINT7	Yes	90	LIN USART 7 TX
91	290_H	LINR8	Yes	91	LIN USART 8 RX
92	$28C_H$	LINT8	Yes	92	LIN USART 8 TX
93	288_H	FLASH_A	No	93	Flash memory A (only Flash devices)

*1: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

*2: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

*3:
- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).
- Sample recommended circuits:



*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “3. DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.
I_A is the analog current consumption into AV_{CC}.

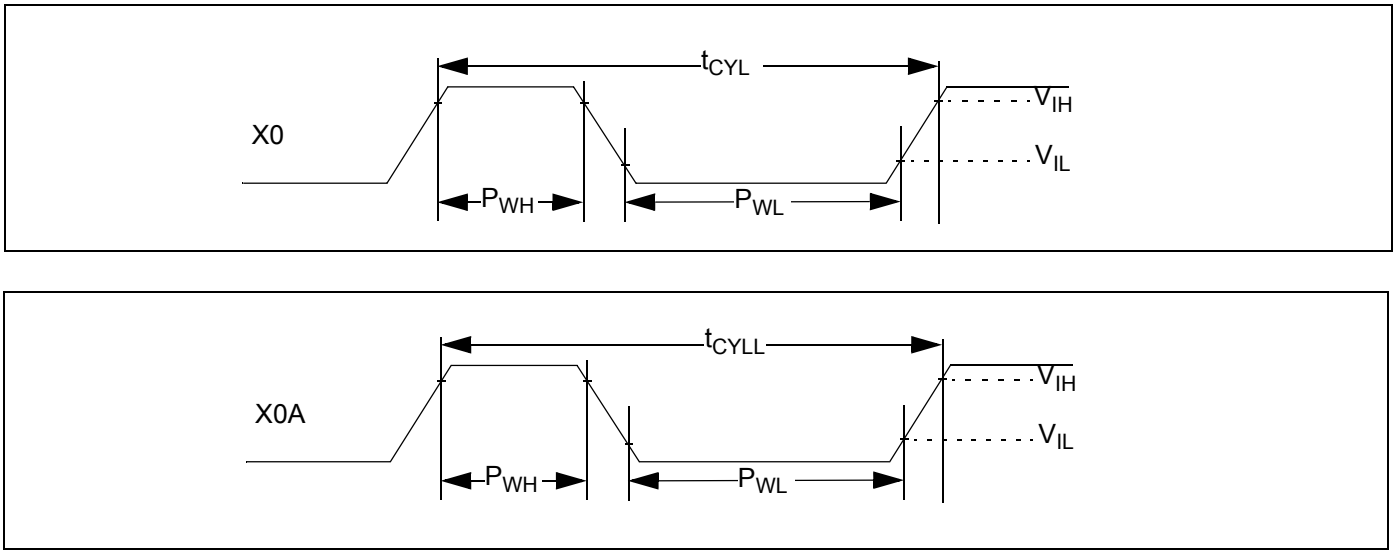
*5: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*6: Please contact Cypress for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

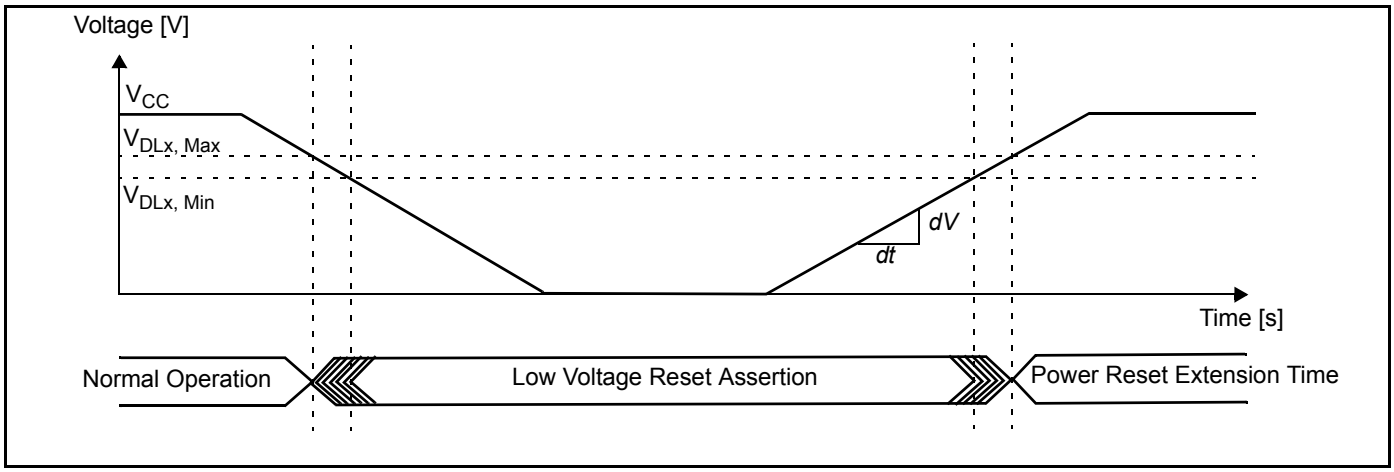
Parameter	Symbol	Condition (at T_A)		Value		Unit	Remarks
				Typ	Max		
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped)	+25°C	1.3	1.8	mA	
			+125°C	1.9	4.8		
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.11	0.2	mA	
			+125°C	0.63	3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.08	0.15	mA	
			+125°C	0.6	2.9		
Power supply current in Timer modes*	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.1	0.2	mA	
			+125°C	0.63	3		
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.07	0.15	mA	
			+125°C	0.6	2.9		
	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.06	0.15	mA	
			+125°C	0.56	2.95		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.03	0.1	mA	
			+125°C	0.53	2.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.035	0.1	mA	
			+125°C	0.53	2.85		


tCYL
X0
VIH
VIL
PWH
PWL

tCYLL
X0A
VIH
VIL
PWH
PWL

Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



14.7 FLASH memory program/erase characteristics

(T_A = -40°C to 105°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Without erasure pre-programming time
Chip erase time	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Word (16-bit width) programming time	-	23	370	us	Without overhead time for submitting write command
Program/Erase cycle	10000	-	-	cycle	
Flash data retention time	20	-	-	year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

15. Example Characteristics

15.1 Temperature dependency of power supply currents

The following diagrams show the current consumption of samples with typical wafer process parameters in different operation modes.

Common condition for all operation modes:

- V_{CC} = AV_{CC} = 5.0V
- Main clock = 4MHz external clock
- Sub clock = 32kHz external clock

Operation mode details:

Mode name	Details
PLL Run 56	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = 56MHz • f_{CLKP2} = 28MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • 2 Flash/ROM wait states (MTCRA=$233A_H$) • RC oscillator and Sub oscillator stopped
PLL Run 48	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = 96MHz • f_{CLKB} = f_{CLKP1} = 48MHz • f_{CLKP2} = 24MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • 1 Flash/ROM wait states (MTCRA=$6B09_H$) • RC oscillator and Sub oscillator stopped
PLL Run 24	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = 48MHz • f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 24MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • 0 Flash/ROM wait states (MTCRA=2208_H) • RC oscillator and Sub oscillator stopped
Main Run	Main Run mode current I_{CCMAIN} with the following settings: • f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 4MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, RC oscillator and Sub oscillator stopped
RC Run 2M	RC Run mode current I_{CCRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 2MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, Main oscillator and Sub oscillator stopped

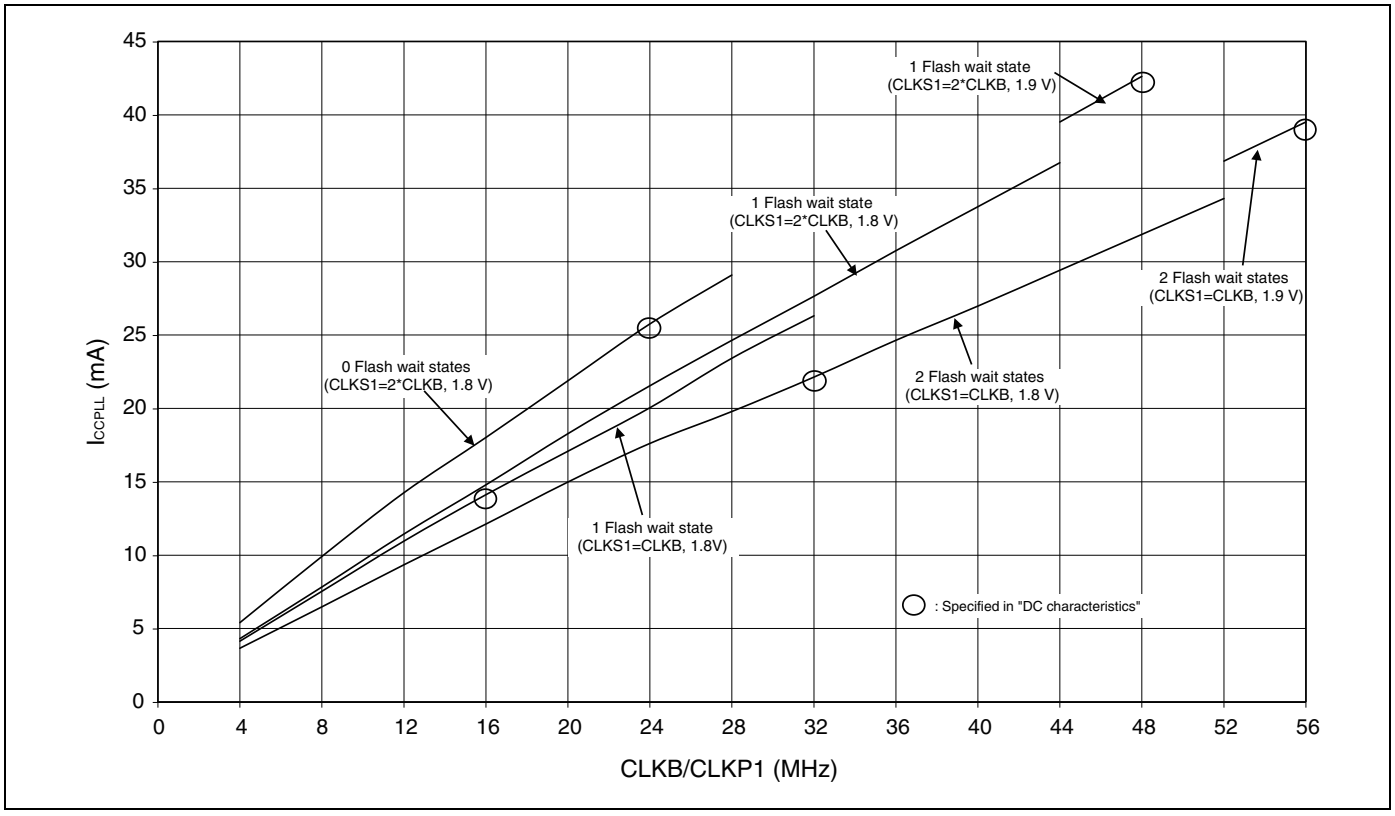
15.2 Frequency dependency of power supply currents in PLL Run mode

The following diagrams show the current consumption of samples with typical wafer process parameters in PLL Run mode at different frequencies and Flash timing settings.

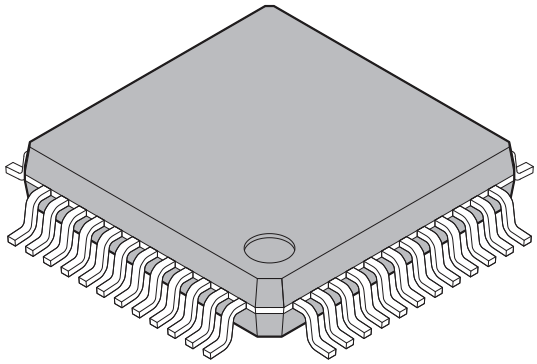
Measurement conditions:

- V_{CC} = AV_{CC} = 5.0V
- Ta = 25°C
- f_{CLKS1} = f_{CLKB} or f_{CLKS1} = 2*f_{CLKB} as described in diagram
- f_{CLKS2} = f_{CLKS1}
- f_{CLKP1} = f_{CLKB}
- f_{CLKP2} = f_{CLKB}/2
- Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) or 1.9V (VRCR:HPM[1:0] = 11_B) as described in diagram
- Main clock = 4MHz external clock
- Flash memory timing settings:
  - MTCRA=2128_H/2208_H (0 Flash wait states, f_{CLKS1} = 2*f_{CLKB})
  - MTCRA=0239_H/2129_H (1 Flash wait state, f_{CLKS1} = f_{CLKB})
  - MTCRA=$4C09_H$/$6B09_H$ (1 Flash wait state, f_{CLKS1} = 2*f_{CLKB})
  - MTCRA=$233A_H$ (2 Flash wait states, f_{CLKS1} = f_{CLKB})
- Average Flash access rate (number of read accesses to the Flash per CLKB clock cycle, no buffer hit):
  - 0 Flash wait states: 0.5
  - 1 Flash wait states: 0.33
  - 2 Flash wait states: 0.25

MB96F313/F315 PLL Run mode currents

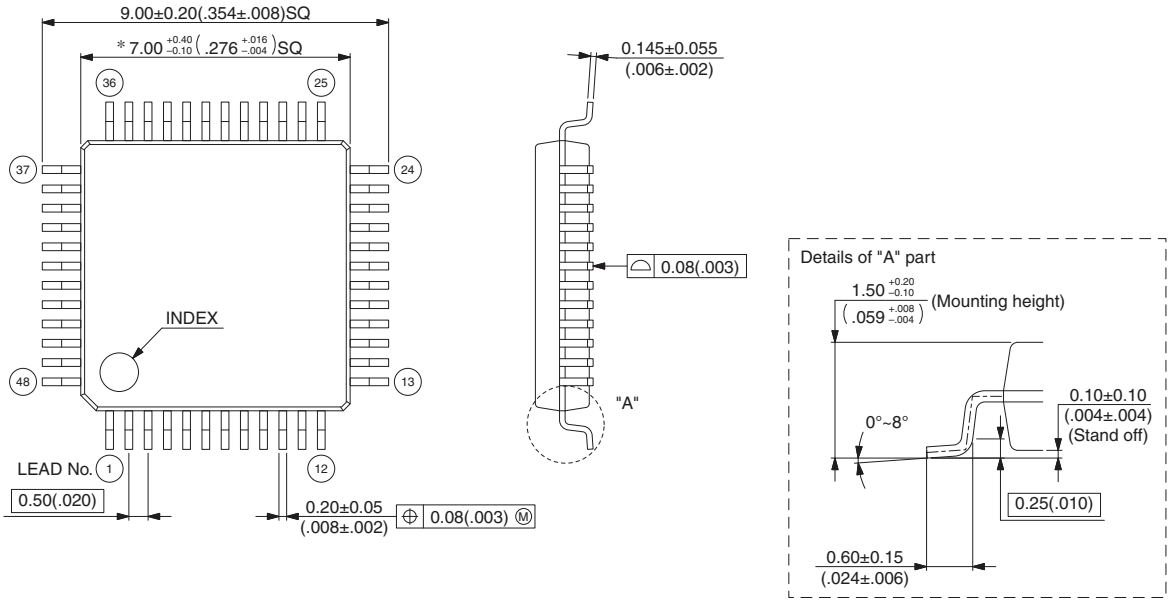


16. Package Dimension MB96(F)31x LQFP48

48-pin plastic LQFP		
 (FPT-48P-M26)	Lead pitch	0.50 mm
	Package width × package length	7 mm × 7 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g
	Code (Reference)	P-LFQFP48-7×7-0.50

48-pin plastic LQFP
(FPT-48P-M26)

Note 1) * : These dimensions include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

17. Ordering Information

MCU with CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F313YSB PMC-GSE2	Flash A (96KB)	No	Yes	48 pins Plastic LQFP (FPT-48P-M26)
MB96F313RSB PMC-GSE1			No	
MB96F313RSB PMC-GSE2			No	
MB96F313YWB PMC-GSE2		Yes	Yes	
MB96F313RWB PMC-GSE2			No	
MB96F315YSB PMC-GSE2	Flash A (160KB)	No	Yes	
MB96F315RSB PMC-GSE1			No	
MB96F315RSB PMC-GSE2			No	
MB96F315YWB PMC-GSE2		Yes	Yes	
MB96F315RWB PMC-GSE2			No	
MB96V300CRB-ES (for evaluation)	Emulated by ext. RAM	Yes	No	416 pin Plastic BGA (BGA-416P-M02)

MCU without CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F313ASB PMC-GSE2	Flash A (96KB)	No	No	48 pins Plastic LQFP (FPT-48P-M26)
MB96F313AWB PMC-GSE2		Yes		
MB96F315ASB PMC-GSE2	Flash A (160KB)	No		
MB96F315AWB PMC-GSE2		Yes		

18. Revision History

Revision	Date	Modification
Prelim 1	2008-12-09	Creation
Prelim 2	2009-01-09	• Interrupt vector table corrected (description of CAN2 interrupt) • Low voltage detector spec updated (detection levels and stabilization time) • C-Pin cap spec updated: 4.7uF-10uF capacitor with tolerance permitted

19. Major Changes

Spansion Publication Number: DS07-13808-2E

Page	Section	Change Results
3	Features	Corrected the sentence “Reload timer overflow” to “Reload timer underflow” for Programmable Pulse Generator.
5, 6	Product Lineup	Removed footnote. Changed name of evaluation sample.
8	Pin Assignments	Corrected pin number of X0. 34 → 35
14	Memory Map	Changed name of evaluation sample.
17	Serial Programming Communication Interface	Corrected device name, package name and pin numbers.
49-50	Electrical Characteristics 3.DC Characteristics	Note added in DC characteristics how to select driving strength of ports.
51-56	Electrical Characteristics 3.DC Characteristics	Updated Icc specs. Updated Power Supply current spec in Run/Sleep/Timer/Stop modes (new spec items in PLL Run/Sleep mode, small adjustment of most other values).
57	Electrical Characteristics 4.AC Characteristics	Note added that PLL phase jitter spec does not include jitter coming from Main clock. Added specification of RC clock stabilization time.
65	Electrical Characteristics 5. Analog Digital Converter	Changed the item for “Zero reading voltage” and “Full scale reading voltage”. AD converter I_{AIN} spec improved: 1uA valid up to 105deg, 1.2uA above 105deg.
68	Electrical Characteristics 5. Analog Digital Converter	“Notes on A/D Converter Section” was rewrite and renamed to “Accuracy and setting of the A/D Converter sampling time”. Impact of input pin capacitance and external capacitance added to formula for calculation of the sampling time.
69	Electrical Characteristics 6. Low Voltage Detector Characteristics	Detection levels updated.
72-77	Example Characteristics	Added.
78	Package Dimension MB96(F)31x LQFP48	Updated package figure. Added the following sentence under the figure: “Please check the latest package dimension at the following URL. http://edevice.fujitsu.com/package/en-search/”.
79	Ordering Information	Updated part number: MB96F313/F315**A → MB96F313/F315**B Removed footnote. Added Part Numbers “MB96F313RSB PMC-GSE1”, “MB96F315RSB PMC-GSE1”.

NOTE: Please see “Document History” about later revised information.