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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

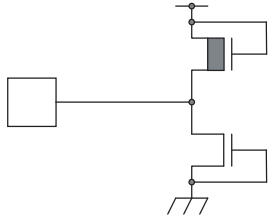
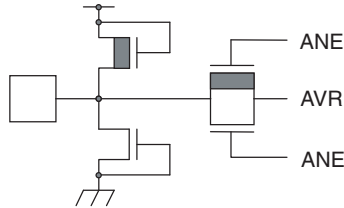
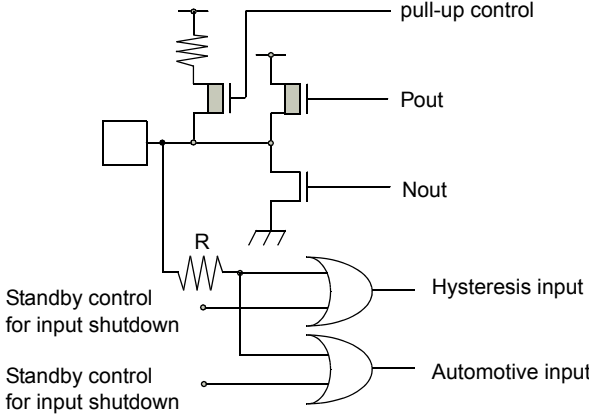
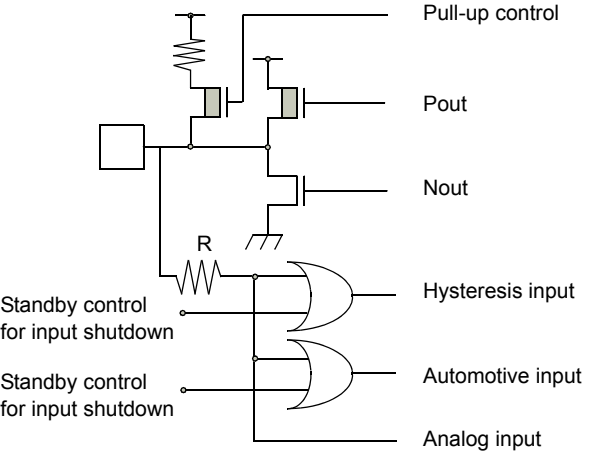
Product Status	Obsolete
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	36
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f315asbpmc-gse2

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Pin Function description (2 of 2)

Pin name	Feature	Description
TTGn	PPG	Programmable Pulse Generator n trigger input
TTGn_R	PPG	Relocated Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
V _{CC}	Supply	Power supply
V _{SS}	Supply	Power supply
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

Type	Circuit	Remarks
F		<ul style="list-style-type: none"> Power supply input protection circuit
G		<ul style="list-style-type: none"> A/D converter ref+ (AVRH) power supply input pin with protection circuit Flash devices do not have a protection circuit against VCC for pin AVRH
H		<ul style="list-style-type: none"> CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) CMOS hysteresis input with input shutdown function Automotive input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
I		<ul style="list-style-type: none"> CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) CMOS hysteresis input with input shutdown function Automotive input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

8. RAMSTART Addresses

Devices	RAM size	RAMSTART0
MB96F313/F315	8KByte	00:6240 _H

9. User ROM Memory Map for Flash Devices

		MB96F313	MB96F315		
Alternative mode CPU address	Flash memory mode address	Flash size 96kByte	Flash size 160kByte		
FF:FFF _H FF:0000 _H	3F:FFF _H 3F:0000 _H	S39 - 64K	S39 - 64K	Flash A	
FE:FFF _H FE:0000 _H	3E:FFF _H 3E:0000 _H	Reserved	S38 - 64K		
FD:FFF _H FD:0000 _H	3D:FFF _H 3D:0000 _H				
FC:FFF _H FC:0000 _H	3C:FFF _H 3C:0000 _H				
FB:FFF _H FB:0000 _H	3B:FFF _H 3B:0000 _H				
FA:FFF _H FA:0000 _H	3A:FFF _H 3A:0000 _H				
F9:FFF _H F9:0000 _H	39:FFF _H 39:0000 _H				
F8:FFF _H F8:0000 _H	38:FFF _H 38:0000 _H				
F7:FFF _H F7:0000 _H	37:FFF _H 37:0000 _H				
F6:FFF _H F6:0000 _H	36:FFF _H 36:0000 _H				
F5:FFF _H F5:0000 _H	35:FFF _H 35:0000 _H				
F4:FFF _H F4:0000 _H	34:FFF _H 34:0000 _H				
F3:FFF _H F3:0000 _H	33:FFF _H 33:0000 _H				
F2:FFF _H F2:0000 _H	32:FFF _H 32:0000 _H				
F1:FFF _H F1:0000 _H	31:FFF _H 31:0000 _H				
F0:FFF _H F0:0000 _H	30:FFF _H 30:0000 _H				
E0:FFF _H			Flash A		
DF:FFF _H DF:8000 _H					
DF:7FFF _H DF:6000 _H	1F:7FFF _H 1F:6000 _H	SA3 - 8K		SA3 - 8K	
DF:5FFF _H DF:4000 _H	1F:5FFF _H 1F:4000 _H	SA2 - 8K		SA2 - 8K	
DF:3FFF _H DF:2000 _H	1F:3FFF _H 1F:2000 _H	SA1 - 8K		SA1 - 8K	
DF:1FFF _H DF:0000 _H	1F:1FFF _H 1F:0000 _H	SA0 - 8K *1		SA0 - 8K *1	
DE:FFF _H DE:0000 _H		Reserved		Reserved	

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000H - DF:007FH

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD[2:0] = 010)

MB96F31x		
Pin number	USART Number	Normal function
LQFP-48		
7	USART2	SIN2
8		SOT2
9		SCK2
20	USART7	SIN7_R
19		SOT7_R
18		SCK7_R
22	USART8	SIN8_R
21		SOT8_R
23		SCK8_R

Note: If a Flash programmer and its software needs to use a handshaking pin, Cypress suggests to the tool vendor to support at least port P00_1 on pin 19.

If handshaking is used by the tool but P00_1 is not available in customer's application, Cypress suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

I/O map MB96(F)315x (Sheet 3 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00005F _H	EXTINT1 - External Interrupt Level Select High	ELVRH1		R/W
000060 _H	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	R/W
000061 _H	RLT0 - Timer Control Status Register High	TMCSRH0		R/W
000062 _H	RLT0 - Reload Register - for writing		TMRLR0	W
000062 _H	RLT0 - Reload Register - for reading		TMR0	R
000063 _H	RLT0 - Reload Register - for writing			W
000063 _H	RLT0 - Reload Register - for reading			R
000064 _H	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	R/W
000065 _H	RLT1 - Timer Control Status Register High	TMCSRH1		R/W
000066 _H	RLT1 - Reload Register - for writing		TMRLR1	W
000066 _H	RLT1 - Reload Register - for reading		TMR1	R
000067 _H	RLT1 - Reload Register - for writing			W
000067 _H	RLT1 - Reload Register - for reading			R
000068 _H	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2	R/W
000069 _H	RLT2 - Timer Control Status Register High	TMCSRH2		R/W
00006A _H	RLT2 - Reload Register - for writing		TMRLR2	W
00006A _H	RLT2 - Reload Register - for reading		TMR2	R
00006B _H	RLT2 - Reload Register - for writing			W
00006B _H	RLT2 - Reload Register - for reading			R
00006C _H	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3	R/W
00006D _H	RLT3 - Timer Control Status Register High	TMCSRH3		R/W
00006E _H	RLT3 - Reload Register - for writing		TMRLR3	W
00006E _H	RLT3 - Reload Register - for reading		TMR3	R
00006F _H	RLT3 - Reload Register - for writing			W
00006F _H	RLT3 - Reload Register - for reading			R
000070 _H	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071 _H	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		R/W
000072 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R

I/O map MB96(F)315x (Sheet 13 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004C4 _H - 0004CF _H	Reserved			-
0004D0 _H	ADC analog input enable register 0	ADER0		R/W
0004D1 _H	ADC analog input enable register 1	ADER1		R/W
0004D2 _H	ADC analog input enable register 2	ADER2		R/W
0004D3 _H	ADC analog input enable register 3	ADER3		R/W
0004D4 _H	ADC analog input enable register 4	ADER4		R/W
0004D5 _H	Reserved			-
0004D6 _H	Peripheral Resource Relocation Register 0	PRRR0		R/W
0004D7 _H	Peripheral Resource Relocation Register 1	PRRR1		R/W
0004D8 _H	Peripheral Resource Relocation Register 2	PRRR2		R/W
0004D9 _H	Peripheral Resource Relocation Register 3	PRRR3		R/W
0004DA _H	Peripheral Resource Relocation Register 4	PRRR4		R/W
0004DB _H	Peripheral Resource Relocation Register 5	PRRR5		R/W
0004DC _H	Peripheral Resource Relocation Register 6	PRRR6		R/W
0004DD _H	Peripheral Resource Relocation Register 7	PRRR7		R/W
0004DE _H	Peripheral Resource Relocation Register 8	PRRR8		R/W
0004DF _H	Peripheral Resource Relocation Register 9	PRRR9		R/W
0004E0 _H	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
0004E1 _H	RTC - Sub Second Register M	WTBRH0		R/W
0004E2 _H	RTC - Sub-Second Register H	WTBR1		R/W
0004E3 _H	RTC - Second Register	WTSR		R/W
0004E4 _H	RTC - Minutes	WTMR		R/W
0004E5 _H	RTC - Hour	WTHR		R/W
0004E6 _H	RTC - Timer Control Extended Register	WTCER		R/W
0004E7 _H	RTC - Clock select register	WTCKSR		R/W
0004E8 _H	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
0004E9 _H	RTC - Timer Control Register High	WTCRH		R/W
0004EA _H	CAL - Calibration unit Control register	CUCR		R/W
0004EB _H	Reserved			-
0004EC _H	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W

I/O map MB96(F)315x (Sheet 18 of 22)

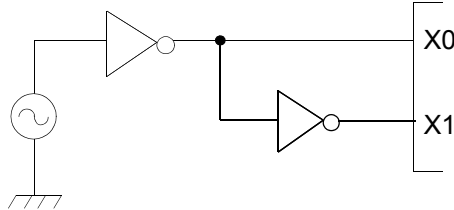
Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005C2 _H	PPG16 - Period setting register		PCSR16	W
0005C3 _H	PPG16 - Period setting register			W
0005C4 _H	PPG16 - Duty cycle register		PDUT16	W
0005C5 _H	PPG16 - Duty cycle register			W
0005C6 _H	PPG16 - Control status register Low	PCNL16	PCN16	R/W
0005C7 _H	PPG16 - Control status register High	PCNH16		R/W
0005C8 _H	PPG17 - Timer register		PTMR17	R
0005C9 _H	PPG17 - Timer register			R
0005CA _H	PPG17 - Period setting register		PCSR17	W
0005CB _H	PPG17 - Period setting register			W
0005CC _H	PPG17 - Duty cycle register		PDUT17	W
0005CD _H	PPG17 - Duty cycle register			W
0005CE _H	PPG17 - Control status register Low	PCNL17	PCN17	R/W
0005CF _H	PPG17 - Control status register High	PCNH17		R/W
0005D0 _H	PPG18 - Timer register		PTMR18	R
0005D1 _H	PPG18 - Timer register			R
0005D2 _H	PPG18 - Period setting register		PCSR18	W
0005D3 _H	PPG18 - Period setting register			W
0005D4 _H	PPG18 - Duty cycle register		PDUT18	W
0005D5 _H	PPG18 - Duty cycle register			W
0005D6 _H	PPG18 - Control status register Low	PCNL18	PCN18	R/W
0005D7 _H	PPG18 - Control status register High	PCNH18		R/W
0005D8 _H	PPG19 - Timer register		PTMR19	R
0005D9 _H	PPG19 - Timer register			R
0005DA _H	PPG19 - Period setting register		PCSR19	W
0005DB _H	PPG19 - Period setting register			W
0005DC _H	PPG19 - Duty cycle register		PDUT19	W
0005DD _H	PPG19 - Duty cycle register			W
0005DE _H	PPG19 - Control status register Low	PCNL19	PCN19	R/W
0005DF _H	PPG19 - Control status register High	PCNH19		R/W

I/O map MB96(F)315x (Sheet 19 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005E0 _H - 00065F _H	Reserved			-
000660 _H	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661 _H	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662 _H	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663 _H	Peripheral Resource Relocation Register 13	PRRR13		W
000664 _H - 0008FF _H	Reserved			-
000900 _H	CAN2 - Control register Low	CTRLRL2	CTRLR2	R/W
000901 _H	CAN2 - Control register High (reserved)	CTRLRH2		R
000902 _H	CAN2 - Status register Low	STATRL2	STATR2	R/W
000903 _H	CAN2 - Status register High (reserved)	STATRH2		R
000904 _H	CAN2 - Error Counter Low (Transmit)	ERRCNTL2	ERRCNT2	R
000905 _H	CAN2 - Error Counter High (Receive)	ERRCNTH2		R
000906 _H	CAN2 - Bit Timing Register Low	BTRL2	BTR2	R/W
000907 _H	CAN2 - Bit Timing Register High	BTRH2		R/W
000908 _H	CAN2 - Interrupt Register Low	INTRL2	INTR2	R
000909 _H	CAN2 - Interrupt Register High	INTRH2		R
00090A _H	CAN2 - Test Register Low	TESTRL2	TESTR2	R/W
00090B _H	CAN2 - Test Register High (reserved)	TESTRH2		R
00090C _H	CAN2 - BRP Extension register Low	BRPERL2	BRPER2	R/W
00090D _H	CAN2 - BRP Extension register High (reserved)	BRPERH2		R
00090E _H - 00090F _H	Reserved			-
000910 _H	CAN2 - IF1 Command request register Low	IF1CREQL2	IF1CREQ2	R/W
000911 _H	CAN2 - IF1 Command request register High	IF1CREQH2		R/W
000912 _H	CAN2 - IF1 Command Mask register Low	IF1CMSKL2	IF1CMSK2	R/W
000913 _H	CAN2 - IF1 Command Mask register High (reserved)	IF1CMSKH2		R
000914 _H	CAN2 - IF1 Mask 1 Register Low	IF1MSK1L2	IF1MSK12	R/W
000915 _H	CAN2 - IF1 Mask 1 Register High	IF1MSK1H2		R/W
000916 _H	CAN2 - IF1 Mask 2 Register Low	IF1MSK2L2	IF1MSK22	R/W
000917 _H	CAN2 - IF1 Mask 2 Register High	IF1MSK2H2		R/W

2. Opposite phase external clock

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



13.4 Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

13.5 Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.6 Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC} -level as well as all V_{SS} -level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

13.7 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

13.8 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC} , $AVRH$, $AVRL$) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed $AVRH$ or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

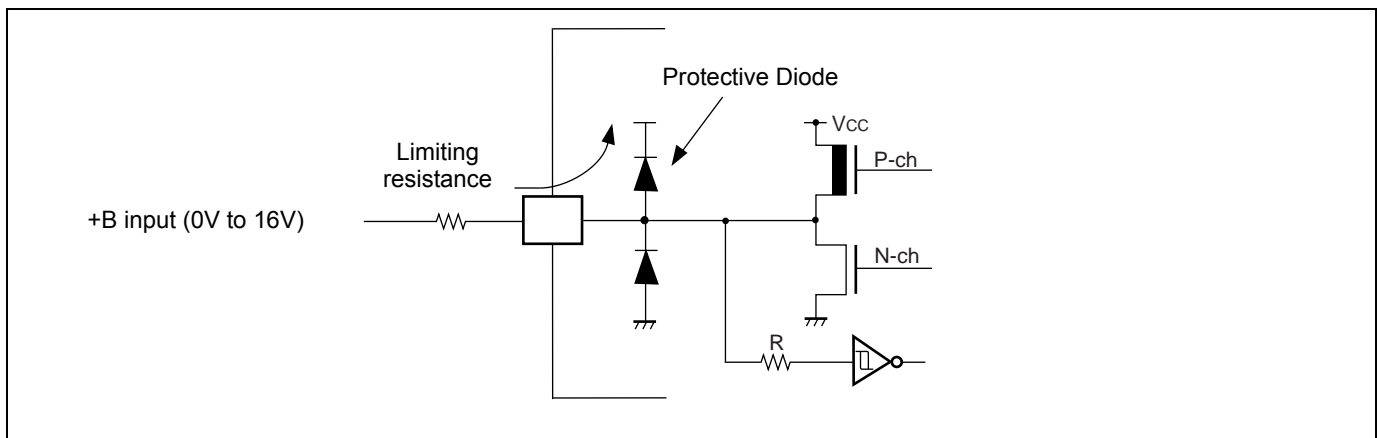
13.9 Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

13.10 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50 μs from 0.2 V to 2.7 V.

- *1: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.
- *2: V_I and V_O should not exceed $V_{CC} + 0.3$ V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC} .
- *3:
 - Applicable to all general purpose I/O pins (Pnn_m)
 - Use within recommended operating conditions.
 - Use at DC voltage (current)
 - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
 - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
 - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).
 - Sample recommended circuits:



- *4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:

$$P_D = P_{IO} + P_{INT}$$

$$P_{IO} = \sum (V_{OL} \cdot I_{OL} + V_{OH} \cdot I_{OH})$$
 (IO load power dissipation, sum is performed on all IO ports)

$$P_{INT} = V_{CC} \cdot (I_{CC} + I_A)$$
 (internal power dissipation)
 I_{CC} is the total core current consumption into V_{CC} as described in the "3. DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.
 I_A is the analog current consumption into AV_{CC} .
- *5: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.
- *6: Please contact Cypress for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.3 DC characteristics

($T_A = -40^\circ\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.7/0.3 input selected	$0.7 V_{CC}$	-	$V_{CC} + 0.3$	V	$V_{CC} \geq 4.5\text{V}$
				$0.74 V_{CC}$	-	$V_{CC} + 0.3$	V	$V_{CC} < 4.5\text{V}$
			AUTOMOTIVE Hysteresis input selected	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	
	V_{IH0F}	X0	External clock in "Fast Clock Input mode"	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	
	V_{IH0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	2.5	-	$V_{CC} + 0.3$	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.7/0.3 input selected	$V_{SS} - 0.3$	-	$0.3 V_{CC}$	V	
				$V_{SS} - 0.3$	-	$0.5 V_{CC}$	V	$V_{CC} \geq 4.5\text{V}$
			AUTOMOTIVE Hysteresis input selected	$V_{SS} - 0.3$	-	$0.46 V_{CC}$		$V_{CC} < 4.5\text{V}$
	V_{IL0F}	X0	External clock in "Fast Clock Input mode"	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	
	V_{IL0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	$V_{SS} - 0.3$	-	0.4	V	
	V_{ILR}	RSTX	-	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	$V_{SS} - 0.3$	-	$V_{SS} + 0.3$	V	
Output H voltage	V_{OH2}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -2\text{mA}$	$V_{CC} - 0.5$	-	-	V	Driving strength set to 2mA (PODR:OD=1)
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -1.6\text{mA}$					
	V_{OH5}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -5\text{mA}$	$V_{CC} - 0.5$	-	-	V	Driving strength set to 5mA (PODR:OD=0)
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -3\text{mA}$					

14.4 AC Characteristics

Source Clock timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using a crystal oscillator, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL off
			3.5	-	56	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	-	256 RC clock cycles				Applied after any reset and when activating the RC oscillator.
PLL Clock frequency	f_{CLKVCO}	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T_{PSKEW}	-	-	-	± 5	ns	For CLKMC (PLL input clock) \square 4MHz, jitter coming from external oscillator, crystal or resonator is not covered
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	μs	

Internal Clock timing

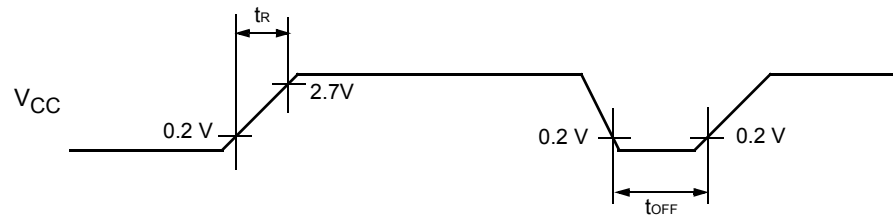
($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f _{CLKS1} , f _{CLKS2}	0	92	0	96	MHz	
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f _{CLKB} , f _{CLKP1}	0	52	0	56	MHz	
Internal peripheral clock frequency (CLKP2)	f _{CLKP2}	0	28	0	32	MHz	

Power On Reset timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	V _{CC}	0.05	-	30	ms	
Power off time	t_{OFF}	V _{CC}	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.



Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

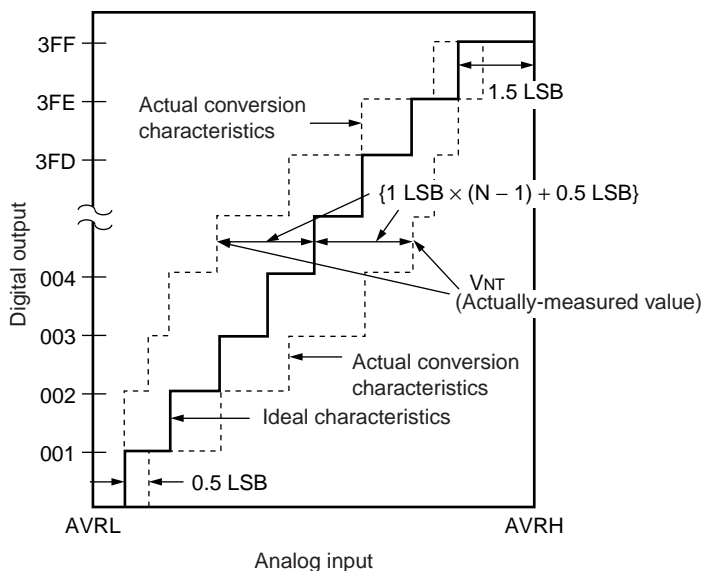
Nonlinearity error: Deviation between a line across zero-transition line ("00 0000 0000" <--> "00 0000 0001") and full-scale transition line ("11 1111 1110" <--> "11 1111 1111") and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$1 \text{ LSB} = (\text{Ideal value}) \frac{AVRH - AVRL}{1024} \quad [\text{V}]$$

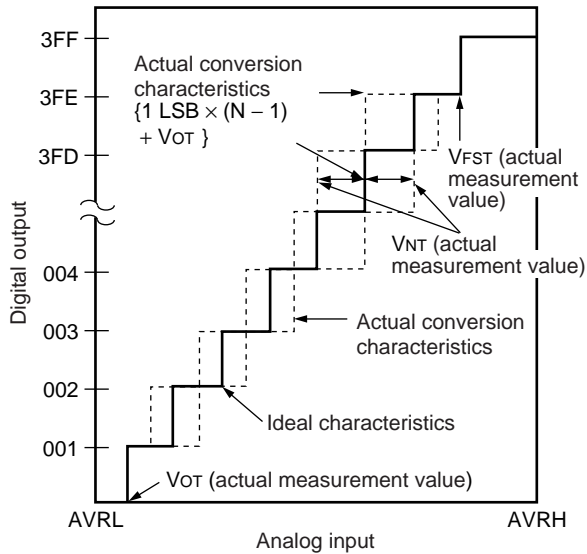
N: A/D converter digital output value

$$V_{OT} (\text{Ideal value}) = AVRL + 0.5 \text{ LSB} \quad [\text{V}]$$

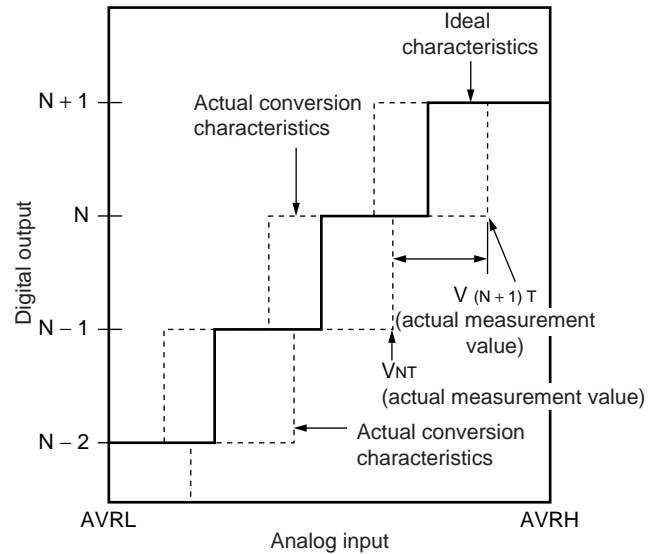
$$V_{FST} (\text{Ideal value}) = AVRH - 1.5 \text{ LSB} \quad [\text{V}]$$

V_{NT} : A voltage at which digital output transitions from (N - 1) to N.

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$\text{Differential nonlinearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB} \quad [\text{LSB}]$$

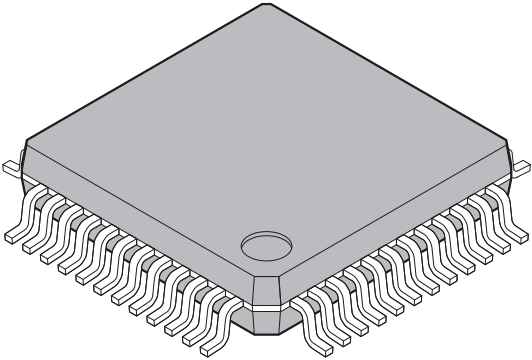
$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

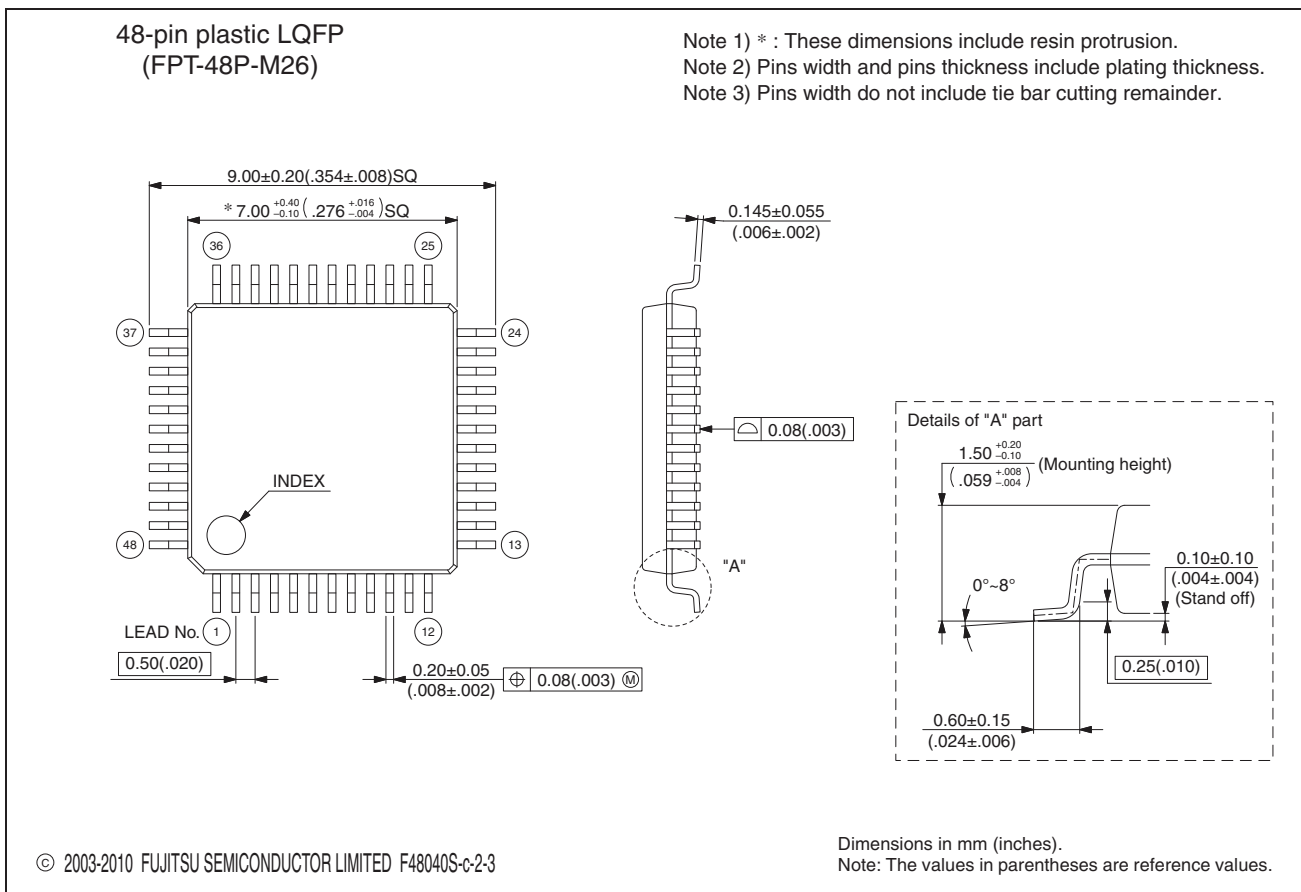
N : A/D converter digital output value

V_{OT} : Voltage at which digital output transits from "000_H" to "001_H."

V_{FST} : Voltage at which digital output transits from "3FE_H" to "3FF_H."

16. Package Dimension MB96(F)31x LQFP48

<p>48-pin plastic LQFP</p>  <p>(FPT-48P-M26)</p>	Lead pitch	0.50 mm
	Package width × package length	7 mm × 7 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g
	Code (Reference)	P-LFQFP48-7×7-0.50



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