Infineon Technologies - MB96F315ASBPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

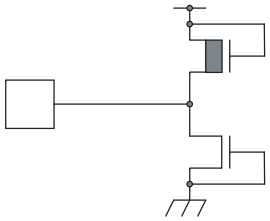
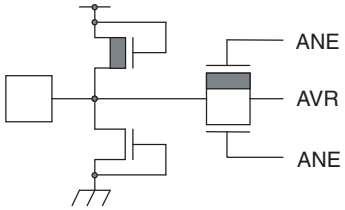
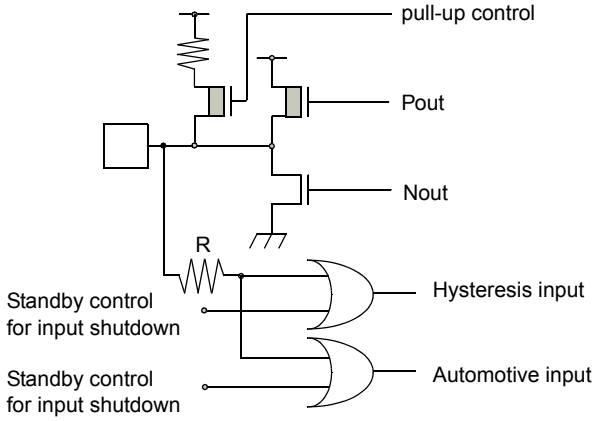
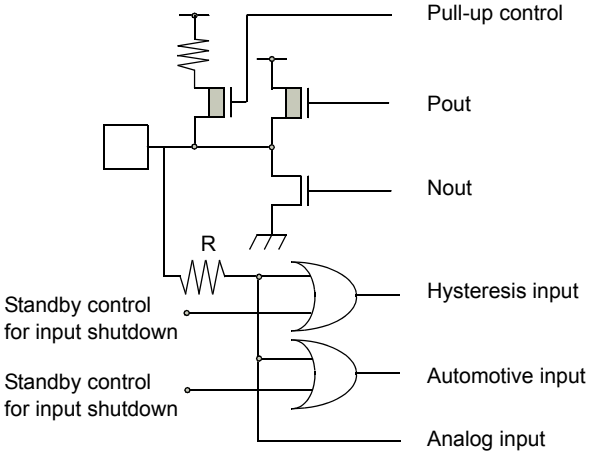
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	36
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f315asbpmc-gse2

Contents

Pin Function description (2 of 2)

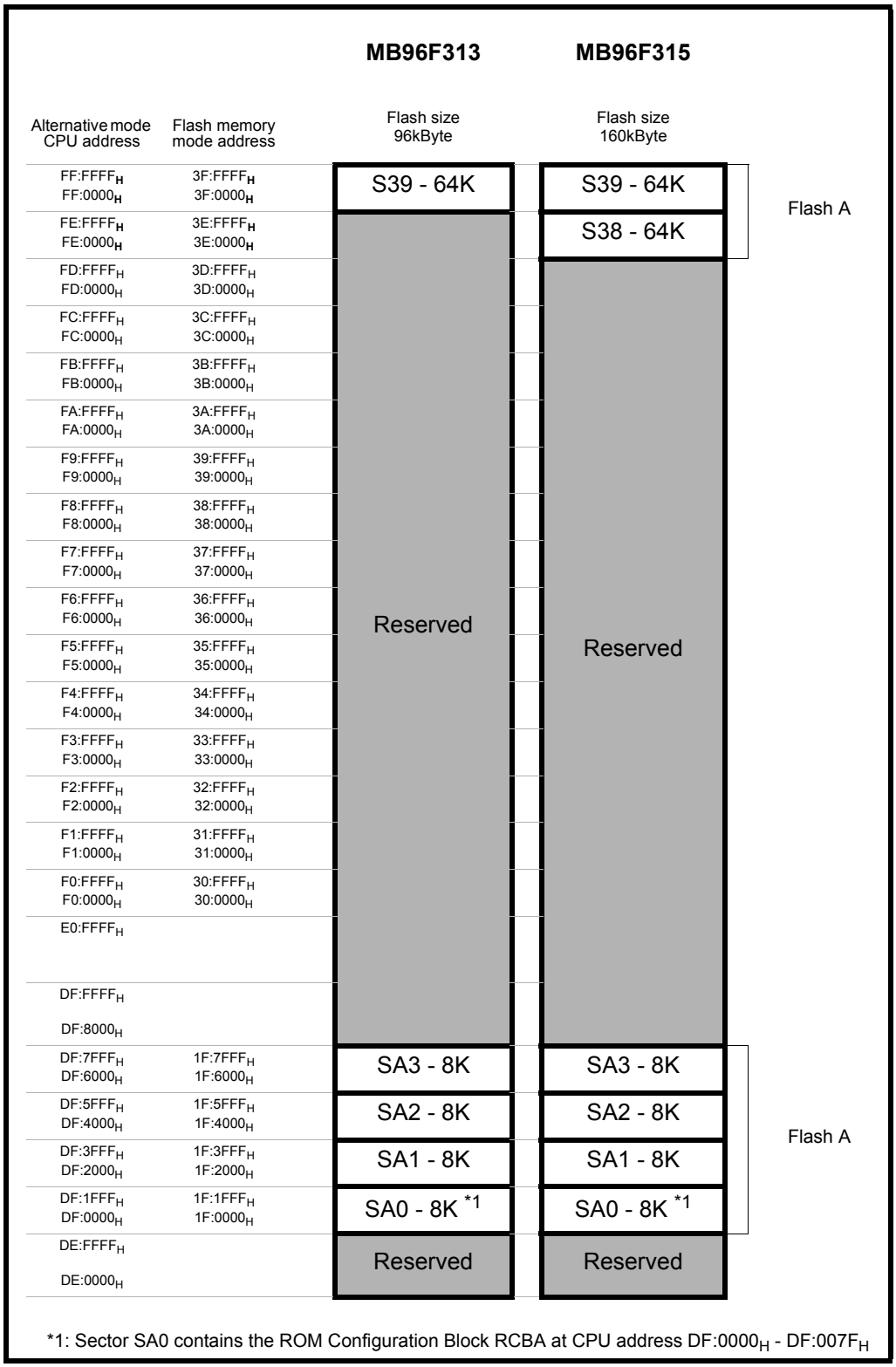
Pin name	Feature	Description
TTGn	PPG	Programmable Pulse Generator n trigger input
TTGn_R	PPG	Relocated Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
V_{CC}	Supply	Power supply
V_{SS}	Supply	Power supply
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix “W”)
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix “W”)

Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pin AVRH
H		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • CMOS hysteresis input with input shutdown function • Automotive input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.
I		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • CMOS hysteresis input with input shutdown function • Automotive input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. • Analog input

8. RAMSTART Addresses

Devices	RAM size	RAMSTART0
MB96F313/F315	8KByte	$00:6240_H$

9. User ROM Memory Map for Flash Devices



*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD[2:0] = 010)

MB96F31x		
Pin number	**USART Number**	**Normal function**
LQFP-48		
7	USART2	SIN2
8		SOT2
9		SCK2
20	USART7	SIN7_R
19		SOT7_R
18		SCK7_R
22	USART8	SIN8_R
21		SOT8_R
23		SCK8_R

Note: If a Flash programmer and its software needs to use a handshaking pin, Cypress suggests to the tool vendor to support at least port P00_1 on pin 19.
If handshaking is used by the tool but P00_1 is not available in customer's application, Cypress suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

I/O map MB96(F)315x (Sheet 3 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00005F_H$	EXTINT1 - External Interrupt Level Select High	ELVRH1		R/W
000060_H	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	R/W
000061_H	RLT0 - Timer Control Status Register High	TMCSRH0		R/W
000062_H	RLT0 - Reload Register - for writing		TMRLR0	W
000062_H	RLT0 - Reload Register - for reading		TMR0	R
000063_H	RLT0 - Reload Register - for writing			W
000063_H	RLT0 - Reload Register - for reading			R
000064_H	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	R/W
000065_H	RLT1 - Timer Control Status Register High	TMCSRH1		R/W
000066_H	RLT1 - Reload Register - for writing		TMRLR1	W
000066_H	RLT1 - Reload Register - for reading		TMR1	R
000067_H	RLT1 - Reload Register - for writing			W
000067_H	RLT1 - Reload Register - for reading			R
000068_H	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2	R/W
000069_H	RLT2 - Timer Control Status Register High	TMCSRH2		R/W
$00006A_H$	RLT2 - Reload Register - for writing		TMRLR2	W
$00006A_H$	RLT2 - Reload Register - for reading		TMR2	R
$00006B_H$	RLT2 - Reload Register - for writing			W
$00006B_H$	RLT2 - Reload Register - for reading			R
$00006C_H$	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3	R/W
$00006D_H$	RLT3 - Timer Control Status Register High	TMCSRH3		R/W
$00006E_H$	RLT3 - Reload Register - for writing		TMRLR3	W
$00006E_H$	RLT3 - Reload Register - for reading		TMR3	R
$00006F_H$	RLT3 - Reload Register - for writing			W
$00006F_H$	RLT3 - Reload Register - for reading			R
000070_H	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071_H	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		R/W
000072_H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072_H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R

I/O map MB96(F)315x (Sheet 13 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0004C4_H$-$0004CF_H$	Reserved			-
$0004D0_H$	ADC analog input enable register 0	ADER0		R/W
$0004D1_H$	ADC analog input enable register 1	ADER1		R/W
$0004D2_H$	ADC analog input enable register 2	ADER2		R/W
$0004D3_H$	ADC analog input enable register 3	ADER3		R/W
$0004D4_H$	ADC analog input enable register 4	ADER4		R/W
$0004D5_H$	Reserved			-
$0004D6_H$	Peripheral Resource Relocation Register 0	PRRR0		R/W
$0004D7_H$	Peripheral Resource Relocation Register 1	PRRR1		R/W
$0004D8_H$	Peripheral Resource Relocation Register 2	PRRR2		R/W
$0004D9_H$	Peripheral Resource Relocation Register 3	PRRR3		R/W
$0004DA_H$	Peripheral Resource Relocation Register 4	PRRR4		R/W
$0004DB_H$	Peripheral Resource Relocation Register 5	PRRR5		R/W
$0004DC_H$	Peripheral Resource Relocation Register 6	PRRR6		R/W
$0004DD_H$	Peripheral Resource Relocation Register 7	PRRR7		R/W
$0004DE_H$	Peripheral Resource Relocation Register 8	PRRR8		R/W
$0004DF_H$	Peripheral Resource Relocation Register 9	PRRR9		R/W
$0004E0_H$	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
$0004E1_H$	RTC - Sub Second Register M	WTBRH0		R/W
$0004E2_H$	RTC - Sub-Second Register H	WTBR1		R/W
$0004E3_H$	RTC - Second Register	WTSR		R/W
$0004E4_H$	RTC - Minutes	WTMR		R/W
$0004E5_H$	RTC - Hour	WTHR		R/W
$0004E6_H$	RTC - Timer Control Extended Register	WTCER		R/W
$0004E7_H$	RTC - Clock select register	WTCKSR		R/W
$0004E8_H$	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
$0004E9_H$	RTC - Timer Control Register High	WTCRH		R/W
$0004EA_H$	CAL - Calibration unit Control register	CUCR		R/W
$0004EB_H$	Reserved			-
$0004EC_H$	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W

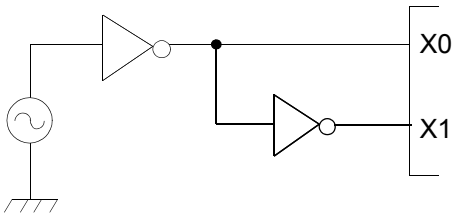
I/O map MB96(F)315x (Sheet 18 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0005C2_H$	PPG16 - Period setting register		PCSR16	W
$0005C3_H$	PPG16 - Period setting register			W
$0005C4_H$	PPG16 - Duty cycle register		PDUT16	W
$0005C5_H$	PPG16 - Duty cycle register			W
$0005C6_H$	PPG16 - Control status register Low	PCNL16	PCN16	R/W
$0005C7_H$	PPG16 - Control status register High	PCNH16		R/W
$0005C8_H$	PPG17 - Timer register		PTMR17	R
$0005C9_H$	PPG17 - Timer register			R
$0005CA_H$	PPG17 - Period setting register		PCSR17	W
$0005CB_H$	PPG17 - Period setting register			W
$0005CC_H$	PPG17 - Duty cycle register		PDUT17	W
$0005CD_H$	PPG17 - Duty cycle register			W
$0005CE_H$	PPG17 - Control status register Low	PCNL17	PCN17	R/W
$0005CF_H$	PPG17 - Control status register High	PCNH17		R/W
$0005D0_H$	PPG18 - Timer register		PTMR18	R
$0005D1_H$	PPG18 - Timer register			R
$0005D2_H$	PPG18 - Period setting register		PCSR18	W
$0005D3_H$	PPG18 - Period setting register			W
$0005D4_H$	PPG18 - Duty cycle register		PDUT18	W
$0005D5_H$	PPG18 - Duty cycle register			W
$0005D6_H$	PPG18 - Control status register Low	PCNL18	PCN18	R/W
$0005D7_H$	PPG18 - Control status register High	PCNH18		R/W
$0005D8_H$	PPG19 - Timer register		PTMR19	R
$0005D9_H$	PPG19 - Timer register			R
$0005DA_H$	PPG19 - Period setting register		PCSR19	W
$0005DB_H$	PPG19 - Period setting register			W
$0005DC_H$	PPG19 - Duty cycle register		PDUT19	W
$0005DD_H$	PPG19 - Duty cycle register			W
$0005DE_H$	PPG19 - Control status register Low	PCNL19	PCN19	R/W
$0005DF_H$	PPG19 - Control status register High	PCNH19		R/W

I/O map MB96(F)315x (Sheet 19 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0005E0_H$-$00065F_H$	Reserved			-
000660_H	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661_H	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662_H	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663_H	Peripheral Resource Relocation Register 13	PRRR13		W
000664_H-$0008FF_H$	Reserved			-
000900_H	CAN2 - Control register Low	CTRLRL2	CTRLR2	R/W
000901_H	CAN2 - Control register High (reserved)	CTRLRH2		R
000902_H	CAN2 - Status register Low	STATRL2	STATR2	R/W
000903_H	CAN2 - Status register High (reserved)	STATRH2		R
000904_H	CAN2 - Error Counter Low (Transmit)	ERRCNTL2	ERRCNT2	R
000905_H	CAN2 - Error Counter High (Receive)	ERRCNTH2		R
000906_H	CAN2 - Bit Timing Register Low	BTRL2	BTR2	R/W
000907_H	CAN2 - Bit Timing Register High	BTRH2		R/W
000908_H	CAN2 - Interrupt Register Low	INTRL2	INTR2	R
000909_H	CAN2 - Interrupt Register High	INTRH2		R
$00090A_H$	CAN2 - Test Register Low	TESTRL2	TESTR2	R/W
$00090B_H$	CAN2 - Test Register High (reserved)	TESTRH2		R
$00090C_H$	CAN2 - BRP Extension register Low	BRPERL2	BRPER2	R/W
$00090D_H$	CAN2 - BRP Extension register High (reserved)	BRPERH2		R
$00090E_H$-$00090F_H$	Reserved			-
000910_H	CAN2 - IF1 Command request register Low	IF1CREQL2	IF1CREQ2	R/W
000911_H	CAN2 - IF1 Command request register High	IF1CREQH2		R/W
000912_H	CAN2 - IF1 Command Mask register Low	IF1CMSKL2	IF1CMSK2	R/W
000913_H	CAN2 - IF1 Command Mask register High (reserved)	IF1CMSKH2		R
000914_H	CAN2 - IF1 Mask 1 Register Low	IF1MSK1L2	IF1MSK12	R/W
000915_H	CAN2 - IF1 Mask 1 Register High	IF1MSK1H2		R/W
000916_H	CAN2 - IF1 Mask 2 Register Low	IF1MSK2L2	IF1MSK22	R/W
000917_H	CAN2 - IF1 Mask 2 Register High	IF1MSK2H2		R/W

2. Opposite phase external clock
   - When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



13.4 Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

13.5 Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.6 Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

13.7 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

13.8 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.9 Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as AV_{CC} = V_{CC}, AV_{SS} = AVRH = AVRL = V_{SS}.

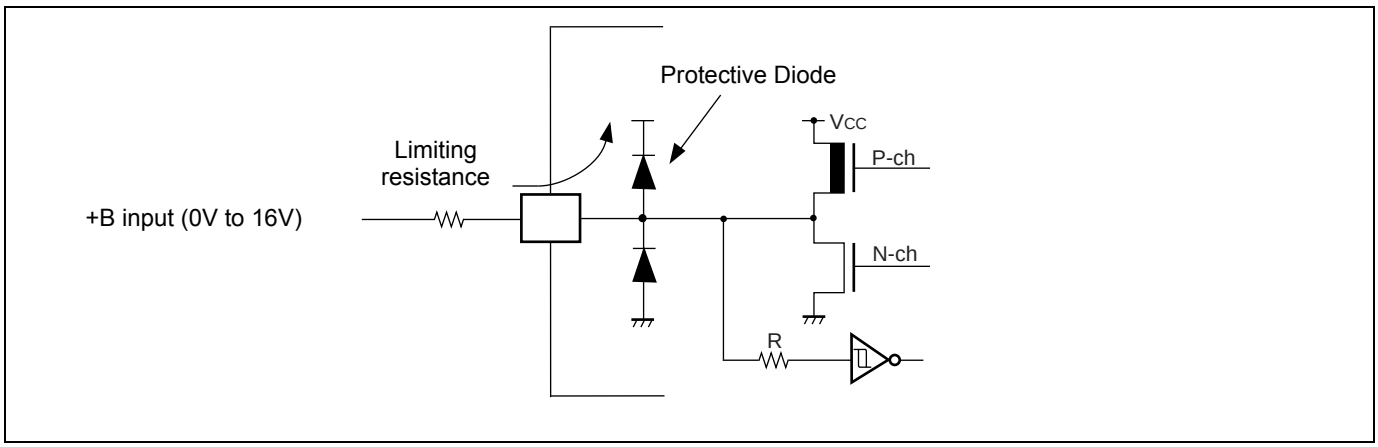
13.10 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50μs from 0.2 V to 2.7 V.

*1: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

*2: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

*3:
- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).
- Sample recommended circuits:



*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “3. DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.
I_A is the analog current consumption into AV_{CC}.

*5: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*6: Please contact Cypress for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.3 DC characteristics

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} \geq 4.5V$
				0.74 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} < 4.5V$
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
	V_{IHX0F}	X0	External clock in “Fast Clock Input mode”	0.8 V_{CC}	-	V_{CC} + 0.3	V	
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5V$
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5V$
	V_{ILX0F}	X0	External clock in “Fast Clock Input mode”	V_{SS} - 0.3	-	0.2 V_{CC}	V	
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	
Output H voltage	V_{OH2}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$, I_{OH} = -2mA / $3.0V \leq V_{CC} < 4.5V$, I_{OH} = -1.6mA	V_{CC} - 0.5	-	-	V	Driving strength set to 2mA (PODR:OD=1)
	V_{OH5}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$, I_{OH} = -5mA / $3.0V \leq V_{CC} < 4.5V$, I_{OH} = -3mA	V_{CC} - 0.5	-	-	V	Driving strength set to 5mA (PODR:OD=0)

14.4 AC Characteristics

Source Clock timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using a crystal oscillator, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” , PLL off
			3.5	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” , PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	-	256 RC clock cycles				Applied after any reset and when activating the RC oscillator.
PLL Clock frequency	f_{CLKVCO}	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T_{PSKEW}	-	-	-	± 5	ns	For CLKMC (PLL input clock) □ 4MHz, jitter coming from external oscillator, crystal or resonator is not covered
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	µs	

Internal Clock timing

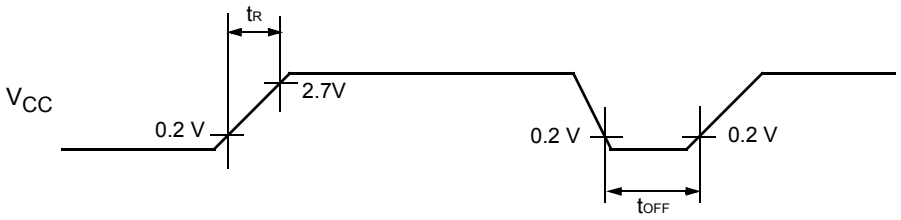
(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	

Power On Reset timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

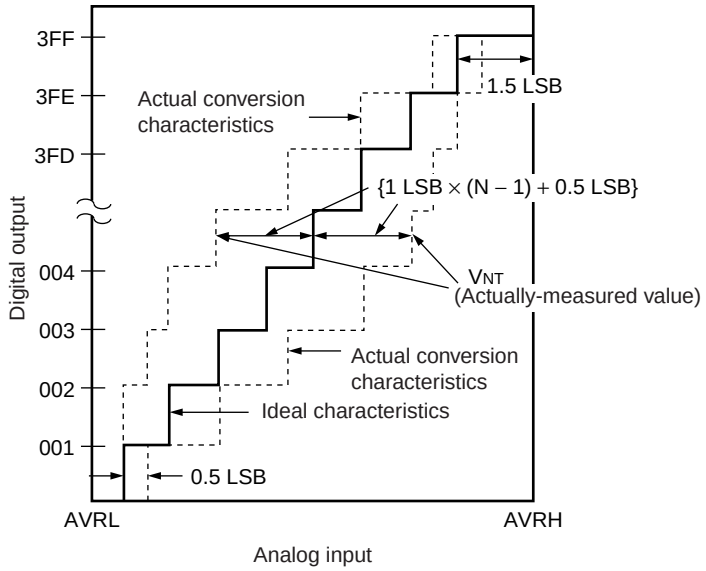
Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

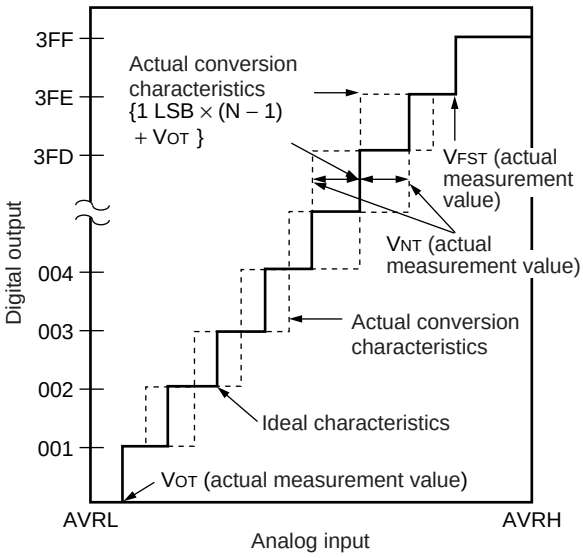
N: A/D converter digital output value

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

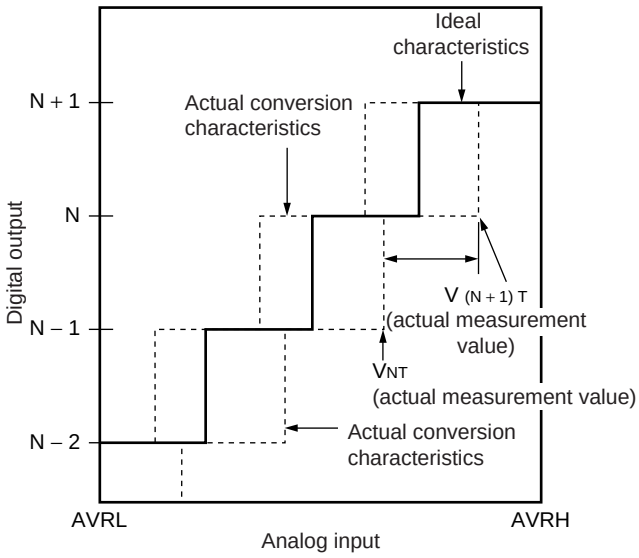
V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

Nonlinearity error



Differential nonlinearity error



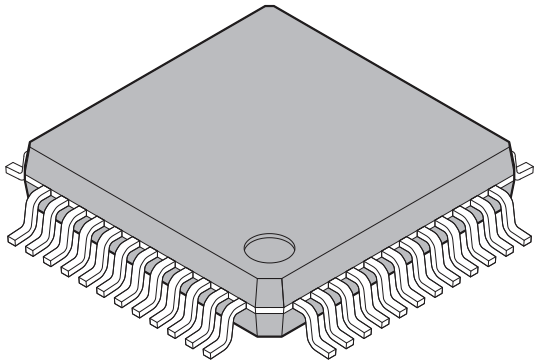
$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

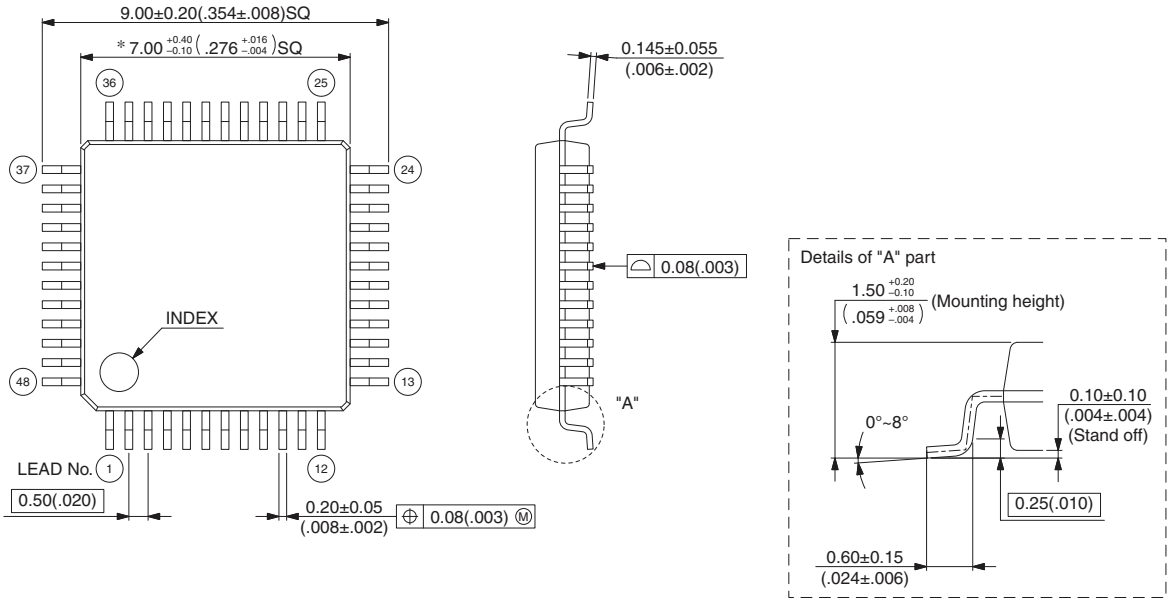
N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H."
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$."

16. Package Dimension MB96(F)31x LQFP48

48-pin plastic LQFP		
 (FPT-48P-M26)	Lead pitch	0.50 mm
	Package width × package length	7 mm × 7 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g
	Code (Reference)	P-LFQFP48-7×7-0.50

48-pin plastic LQFP
(FPT-48P-M26)

Note 1) * : These dimensions include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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