Infineon Technologies - MB96F315RSBPMC-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	36
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f315rsbpmc-gse1

1. Product Lineup

Features		MB96V300C	MB96(F)31x
Product type		Evaluation sample	Flash product: MB96F31x Mask ROM product: MB9631x
Product options			
YS		NA	Low voltage reset persistently on / Single clock devices
RS			Low voltage reset can be disabled / Single clock devices
YW			Low voltage reset persistently on / Dual clock devices
RW			Low voltage reset can be disabled / Dual clock devices
AS			No CAN / Low voltage reset can be disabled / Single clock devices
AW			No CAN / Low voltage reset can be disabled / Dual clock devices
Flash/ROM	RAM		
96KB	8KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM	MB96F313Y, MB96F313R, MB96F313A
160KB	8KB		MB96F315Y, MB96F315R, MB96F315A
Package		BGA416	FPT-48P-M26
DMA		16 channels	4 channels
USART		10 channels	3 channels
A/D Converter		40 channels	12 channels
A/D Converter Reference Voltage switch		yes	No
16-bit Reload Timer		6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer		4 channels	4 channels (without external clock input pin)
16-bit Output Compare		12 channels	2 channels
16-bit Input Capture		12 channels	4 channels (plus 3 channels for LIN USART)
16-bit Programmable Pulse Generator		20 channels	14 channels
CAN Interface		5 channels	1 channel
External Interrupts		16 channels	11 channels
Non-Maskable Interrupt		1 channel	
Real Time Clock		1	
I/O Ports		136	34 for part number with suffix “W”, 36 for part number with suffix “S”
Clock output function		2 channels	
Low voltage reset		Yes	
On-chip RC-oscillator		Yes	

4. Pin Function Description

Pin Function description (1 of 2)

Pin name	Feature	Description
ADTG_R	ADC	Relocated A/D converter trigger input
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TINn_R	Reload Timer	Relocated Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TOTn_R	Reload Timer	Relocated Reload Timer n output

5. Pin Circuit Type

Pin circuit types

FPT-48P-M26	
Pin no.	**Circuit type** [*1]
1	Supply
2	G
3 to 12	I
13, 14	B [*2]
13, 14	H [*3]
15 to 17	C
18 to 32	H
33	E
34, 35	A
36, 37	Supply
38	F
39 to 45	H
46, 47	I
48	Supply

*1: Please refer to “6.“I/O Circuit Type”” for details on the I/O circuit types

*2: Devices with suffix “W”

*3: Devices without suffix “W”

8. RAMSTART Addresses

Devices	RAM size	RAMSTART0
MB96F313/F315	8KByte	$00:6240_H$

I/O map MB96(F)315x (Sheet 6 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000104_H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105_H	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106_H	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107_H	DMA0 - Data counter high byte	DCTH0		R/W
000108_H	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109_H	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
$00010A_H$	DMA1 - Buffer address pointer high byte	BAPH1		R/W
$00010B_H$	DMA1 - DMA control register	DMACS1		R/W
$00010C_H$	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W
$00010D_H$	DMA1 - I/O register address pointer high byte	IOAH1		R/W
$00010E_H$	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
$00010F_H$	DMA1 - Data counter high byte	DCTH1		R/W
000110_H	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111_H	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112_H	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113_H	DMA2 - DMA control register	DMACS2		R/W
000114_H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115_H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116_H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117_H	DMA2 - Data counter high byte	DCTH2		R/W
000118_H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119_H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
$00011A_H$	DMA3 - Buffer address pointer high byte	BAPH3		R/W
$00011B_H$	DMA3 - DMA control register	DMACS3		R/W
$00011C_H$	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
$00011D_H$	DMA3 - I/O register address pointer high byte	IOAH3		R/W
$00011E_H$	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
$00011F_H$	DMA3 - Data counter high byte	DCTH3		R/W
000120_H-$00017F_H$	Reserved			-

I/O map MB96(F)315x (Sheet 11 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000435_H	I/O Port P05 - Data Direction Register	DDR05		R/W
000436_H	I/O Port P06 - Data Direction Register	DDR06		R/W
000437_H	I/O Port P07 - Data Direction Register	DDR07		R/W
000438_H-000443_H	Reserved			-
000444_H	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445_H	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446_H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447_H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448_H	Reserved			-
000449_H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
$00044A_H$	I/O Port P06 - Port Input Enable Register	PIER06		R/W
$00044B_H$	I/O Port P07 - Port Input Enable Register	PIER07		R/W
$00044C_H$-000457_H	Reserved			-
000458_H	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459_H	I/O Port P01 - Port Input Level Register	PILR01		R/W
$00045A_H$	I/O Port P02 - Port Input Level Register	PILR02		R/W
$00045B_H$	I/O Port P03 - Port Input Level Register	PILR03		R/W
$00045C_H$	Reserved			-
$00045D_H$	I/O Port P05 - Port Input Level Register	PILR05		R/W
$00045E_H$	I/O Port P06 - Port Input Level Register	PILR06		R/W
$00045F_H$	I/O Port P07 - Port Input Level Register	PILR07		R/W
000460_H-$00046B_H$	Reserved			-
$00046C_H$	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
$00046D_H$	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
$00046E_H$	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
$00046F_H$	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470_H	Reserved			-
000471_H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472_H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W

I/O map MB96(F)315x (Sheet 18 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0005C2_H$	PPG16 - Period setting register		PCSR16	W
$0005C3_H$	PPG16 - Period setting register			W
$0005C4_H$	PPG16 - Duty cycle register		PDUT16	W
$0005C5_H$	PPG16 - Duty cycle register			W
$0005C6_H$	PPG16 - Control status register Low	PCNL16	PCN16	R/W
$0005C7_H$	PPG16 - Control status register High	PCNH16		R/W
$0005C8_H$	PPG17 - Timer register		PTMR17	R
$0005C9_H$	PPG17 - Timer register			R
$0005CA_H$	PPG17 - Period setting register		PCSR17	W
$0005CB_H$	PPG17 - Period setting register			W
$0005CC_H$	PPG17 - Duty cycle register		PDUT17	W
$0005CD_H$	PPG17 - Duty cycle register			W
$0005CE_H$	PPG17 - Control status register Low	PCNL17	PCN17	R/W
$0005CF_H$	PPG17 - Control status register High	PCNH17		R/W
$0005D0_H$	PPG18 - Timer register		PTMR18	R
$0005D1_H$	PPG18 - Timer register			R
$0005D2_H$	PPG18 - Period setting register		PCSR18	W
$0005D3_H$	PPG18 - Period setting register			W
$0005D4_H$	PPG18 - Duty cycle register		PDUT18	W
$0005D5_H$	PPG18 - Duty cycle register			W
$0005D6_H$	PPG18 - Control status register Low	PCNL18	PCN18	R/W
$0005D7_H$	PPG18 - Control status register High	PCNH18		R/W
$0005D8_H$	PPG19 - Timer register		PTMR19	R
$0005D9_H$	PPG19 - Timer register			R
$0005DA_H$	PPG19 - Period setting register		PCSR19	W
$0005DB_H$	PPG19 - Period setting register			W
$0005DC_H$	PPG19 - Duty cycle register		PDUT19	W
$0005DD_H$	PPG19 - Duty cycle register			W
$0005DE_H$	PPG19 - Control status register Low	PCNL19	PCN19	R/W
$0005DF_H$	PPG19 - Control status register High	PCNH19		R/W

I/O map MB96(F)315x (Sheet 19 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0005E0_H$-$00065F_H$	Reserved			-
000660_H	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661_H	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662_H	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663_H	Peripheral Resource Relocation Register 13	PRRR13		W
000664_H-$0008FF_H$	Reserved			-
000900_H	CAN2 - Control register Low	CTRLRL2	CTRLR2	R/W
000901_H	CAN2 - Control register High (reserved)	CTRLRH2		R
000902_H	CAN2 - Status register Low	STATRL2	STATR2	R/W
000903_H	CAN2 - Status register High (reserved)	STATRH2		R
000904_H	CAN2 - Error Counter Low (Transmit)	ERRCNTL2	ERRCNT2	R
000905_H	CAN2 - Error Counter High (Receive)	ERRCNTH2		R
000906_H	CAN2 - Bit Timing Register Low	BTRL2	BTR2	R/W
000907_H	CAN2 - Bit Timing Register High	BTRH2		R/W
000908_H	CAN2 - Interrupt Register Low	INTRL2	INTR2	R
000909_H	CAN2 - Interrupt Register High	INTRH2		R
$00090A_H$	CAN2 - Test Register Low	TESTRL2	TESTR2	R/W
$00090B_H$	CAN2 - Test Register High (reserved)	TESTRH2		R
$00090C_H$	CAN2 - BRP Extension register Low	BRPERL2	BRPER2	R/W
$00090D_H$	CAN2 - BRP Extension register High (reserved)	BRPERH2		R
$00090E_H$-$00090F_H$	Reserved			-
000910_H	CAN2 - IF1 Command request register Low	IF1CREQL2	IF1CREQ2	R/W
000911_H	CAN2 - IF1 Command request register High	IF1CREQH2		R/W
000912_H	CAN2 - IF1 Command Mask register Low	IF1CMSKL2	IF1CMSK2	R/W
000913_H	CAN2 - IF1 Command Mask register High (reserved)	IF1CMSKH2		R
000914_H	CAN2 - IF1 Mask 1 Register Low	IF1MSK1L2	IF1MSK12	R/W
000915_H	CAN2 - IF1 Mask 1 Register High	IF1MSK1H2		R/W
000916_H	CAN2 - IF1 Mask 2 Register Low	IF1MSK2L2	IF1MSK22	R/W
000917_H	CAN2 - IF1 Mask 2 Register High	IF1MSK2H2		R/W

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
36	$36C_H$				Reserved
37	368_H	PPG3	Yes	37	Programmable Pulse Generator 3
38	364_H	PPG4	Yes	38	Programmable Pulse Generator 4
39	360				Reserved
40	$35C_H$	PPG6	Yes	40	Programmable Pulse Generator 6
41	358_H	PPG7	Yes	41	Programmable Pulse Generator 7
42	354_H	PPG8	Yes	42	Programmable Pulse Generator 8
43	350_H	PPG9	Yes	43	Programmable Pulse Generator 9
44	$34C_H$				Reserved
45	348_H				Reserved
46	344_H	PPG12	Yes	46	Programmable Pulse Generator 12
47	340_H				Reserved
48	$33C_H$	PPG14	Yes	48	Programmable Pulse Generator 14
49	338_H				Reserved
50	334_H	PPG16	Yes	50	Programmable Pulse Generator 16
51	330_H	PPG17	Yes	51	Programmable Pulse Generator 17
52	$32C_H$	PPG18	Yes	52	Programmable Pulse Generator 18
53	328_H	PPG19	Yes	53	Programmable Pulse Generator 19
54	324_H	RLT0	Yes	54	Reload Timer 0
55	320_H	RLT1	Yes	55	Reload Timer 1
56	$31C_H$	RLT2	Yes	56	Reload Timer 2
57	318_H	RLT3	Yes	57	Reload Timer 3
58	314_H	PPGRLT	Yes	58	Reload Timer 6 - dedicated for PPG
59	310_H	ICU0	Yes	59	Input Capture Unit 0
60	$30C_H$	ICU1	Yes	60	Input Capture Unit 1
61	308_H				Reserved
62	304_H				Reserved
63	300_H	ICU4	Yes	63	Input Capture Unit 4
64	$2FC_H$	ICU5	Yes	64	Input Capture Unit 5
65	$2F8_H$	ICU6	Yes	65	Input Capture Unit 6
66	$2F4_H$				Reserved
67	$2F0_H$				Reserved
68	$2EC_H$	ICU9	Yes	68	Input Capture Unit 9
69	$2E8_H$	ICU10	Yes	69	Input Capture Unit 10
70	$2E4_H$				Reserved
71	$2E0_H$				Reserved
72	$2DC_H$				Reserved

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

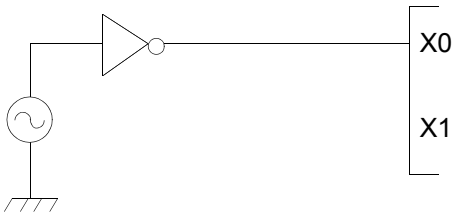
Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

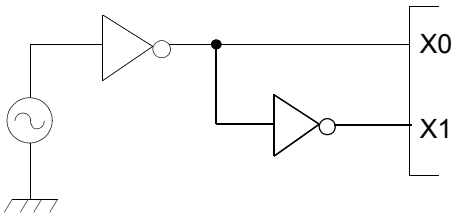
13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

1. Single phase external clock
   - When using a single phase external clock, X0 (X0A) pin must be driven and X1 (X1A) pin left open.



2. Opposite phase external clock
   - When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



13.4 Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

13.5 Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.6 Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

13.7 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

13.8 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.9 Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as AV_{CC} = V_{CC}, AV_{SS} = AVRH = AVRL = V_{SS}.

13.10 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50μs from 0.2 V to 2.7 V.

13.11 Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/μs or less in instantaneous fluctuation for power supply switching.

13.12 Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value		Unit	Remarks
				Typ	Max		
Power supply current in Sleep modes*	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = CLKP1 = 16MHz, CLKP2 = 8MHz (CLKRC and CLKSC stopped)	+25°C	4	6	mA	
			+125°C	4.7	9		
		PLL Sleep mode with CLKS1/2 = CLKP1 = 32MHz, CLKP2 = 16MHz (CLKRC and CLKSC stopped)	+25°C	7	9.5	mA	
			+125°C	8	12.5		
		PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz (CLKRC and CLKSC stopped)	+25°C	7	9	mA	
			+125°C	8	12		
		PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	11	14.5	mA	
			+125°C	12	17.5		
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	12	15	mA	
			+125°C	13	18		
	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25°C	1	1.3	mA	
			+125°C	1.6	4.1		
	I_{CCSRCH}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped)	+25°C	0.55	1.1	mA	
			+125°C	1.15	3.9		
Power supply current in Sleep modes*	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.08	0.2	mA	
			+125°C	0.59	2.95		
		RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.05	0.15	mA	
			+125°C	0.56	2.9		
	I_{CCSSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.04	0.12	mA	
			+125°C	0.54	2.9		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value		Unit	Remarks
				Typ	Max		
Power supply current in Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110_B (Core voltage at 1.8V)	+25°C	0.02	0.08	mA	
			+125°C	0.52	2.8		
		VRCR:LPMB[2:0] = 000_B (Core voltage at 1.2V)	+25°C	0.015	0.06	mA	
			+125°C	0.4	2.3		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	+25°C	5	10	µA	Must be added to all current above
			+125°C	7	20		
Power supply current for active Clock modulator	$I_{CCCLOMO}$	Clock modulator enabled (CMCR:PDX = 1)	-	3	4.5	mA	Must be added to all current above
Flash Write/Erase current	$I_{CCFLASH}$	Current for one Flash module	-	15	40	mA	Must be added to all current above
Input capacitance	C_{IN}	-	-	5	15	pF	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}

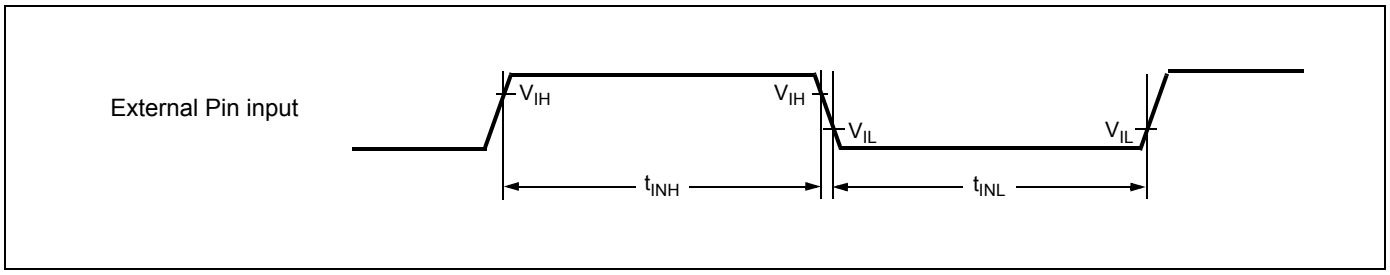
* : The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control.

External Input timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn(_R)	—	200	—	ns	External Interrupt
		NMI					NMI
		Pnn_m		$2*t_{CLKP1}$ + 200 ($t_{CLKP1}=1/f_{CLKP1}$)	—	ns	General Purpose IO
		TINn					Reload Timer
		TTGn(_R)					PPG Trigger input
		ADTG_R					AD Converter Trigger
		INn					Input Capture

Note : Relocated Resource Inputs have same characteristics



USART timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

(T_A = -40°C to 125°C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	—	4 t_{CLKP1}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		$N*t_{CLKP1}$ - 20 *1	—	$N*t_{CLKP1}$ - 30 *1	—	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	—	t_{CLKP1} + 55	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	0	—	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		—	2 t_{CLKP1} + 45	—	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	—	t_{CLKP1}/2 + 10	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK fall time	t_{FE}	SCKn		—	20	—	20	ns
SCK rise time	t_{RE}	SCKn		—	20	—	20	ns

Notes:
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96300 Super series Hardware Manual”.
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

*1: Parameter N depends on t_{SCYCI} and can be calculated as follows:
- if t_{SCYCI} = 2*k*t_{CLKP1}, then N = k, where k is an integer > 2
- if t_{SCYCI} = (2*k+1)*t_{CLKP1}, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
4*t_{CLKP1}	2
5*t_{CLKP1}, 6*t_{CLKP1}	3
7*t_{CLKP1}, 8*t_{CLKP1}	4
...	...

14.7 FLASH memory program/erase characteristics

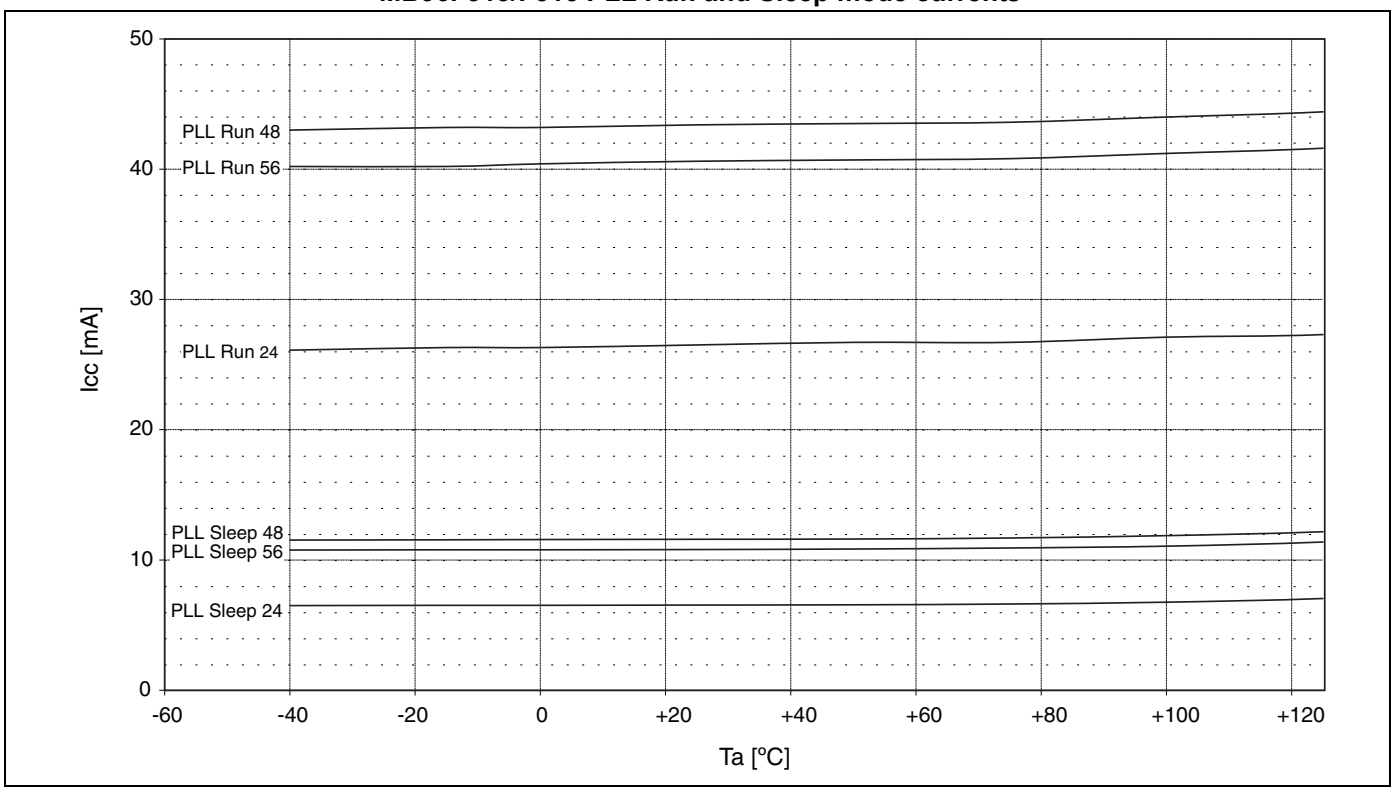
(T_A = -40°C to 105°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Without erasure pre-programming time
Chip erase time	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Word (16-bit width) programming time	-	23	370	us	Without overhead time for submitting write command
Program/Erase cycle	10000	-	-	cycle	
Flash data retention time	20	-	-	year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

Mode name	Details
RC Sleep 100k	RC Sleep mode current I_{CCSRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 100kHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
Sub Sleep	Sub Sleep mode current I_{CCSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Main oscillator stopped
PLL Timer 48	PLL Timer mode current I_{CCTPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 48MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • RC oscillator and Sub oscillator stopped
Main Timer	Main Timer mode current $I_{CCTMAIN}$ with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 4MHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Sub oscillator stopped
RC Timer 2M	RC Timer mode current I_{CCTRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2}$ = 2MHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
RC Timer 100k	RC Timer mode current I_{CCTRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2}$ = 100kHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
Sub Timer	Sub Timer mode current I_{CCTSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Main oscillator stopped
Stop 1.8V	Stop mode current I_{CCH} with the following settings: • Regulator in Low Power Mode B (by hardware) • Core voltage at 1.8V (VRCR:LPMB[2:0] = 110_B)
Stop 1.2V	Stop mode current I_{CCH} with the following settings: • Regulator in Low Power Mode B (by hardware) • Core voltage at 1.2V (VRCR:LPMB[2:0] = 000_B)

MB96F313/F315 PLL Run and Sleep mode currents



17. Ordering Information

MCU with CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F313YSB PMC-GSE2	Flash A (96KB)	No	Yes	48 pins Plastic LQFP (FPT-48P-M26)
MB96F313RSB PMC-GSE1			No	
MB96F313RSB PMC-GSE2			No	
MB96F313YWB PMC-GSE2		Yes	Yes	
MB96F313RWB PMC-GSE2			No	
MB96F315YSB PMC-GSE2	Flash A (160KB)	No	Yes	
MB96F315RSB PMC-GSE1			No	
MB96F315RSB PMC-GSE2			No	
MB96F315YWB PMC-GSE2		Yes	Yes	
MB96F315RWB PMC-GSE2			No	
MB96V300CRB-ES (for evaluation)	Emulated by ext. RAM	Yes	No	416 pin Plastic BGA (BGA-416P-M02)

MCU without CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F313ASB PMC-GSE2	Flash A (96KB)	No	No	48 pins Plastic LQFP (FPT-48P-M26)
MB96F313AWB PMC-GSE2		Yes		
MB96F315ASB PMC-GSE2	Flash A (160KB)	No		
MB96F315AWB PMC-GSE2		Yes		