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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

2 014110	
Product Status	Obsolete
Core Processor	F <sup>2</sup> MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	34
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	•
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f315rwbpmc-gse2

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



### **Flash Memory**

- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the algorithm
- Number of erase cycles: 10,000 times
- Data retention time: 20 years
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase



### 10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD[2:0] = 010)

MB96F31x										
Pin number		Normal function								
LQFP-48	USART Number									
7		SIN2								
8	USART2	SOT2								
9		SCK2								
20		SIN7_R								
19	USART7	SOT7_R								
18		SCK7_R								
22		SIN8_R								
21	USART8	SOT8_R								
23		SCK8_R								

Note: If a Flash programmer and its software needs to use a handshaking pin, Cypress suggests to the tool vendor to support at least port P00\_1 on pin 19.

If handshaking is used by the tool but P00\_1 is not available in customer's application, Cypress suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.



## I/O map MB96(F)315x (Sheet 6 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access			
000104 <sub>H</sub>	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W			
000105 <sub>H</sub>	DMA0 - I/O register address pointer high byte	IOAH0		R/W			
000106 <sub>H</sub>	DMA0 - Data counter low byte						
000107 <sub>H</sub>	DMA0 - Data counter high byte	DCTH0		R/W			
000108 <sub>H</sub>	DMA1 - Buffer address pointer low byte	BAPL1		R/W			
000109 <sub>H</sub>	DMA1 - Buffer address pointer middle byte	BAPM1		R/W			
00010A <sub>H</sub>	DMA1 - Buffer address pointer high byte	BAPH1		R/W			
00010B <sub>H</sub>	DMA1 - DMA control register	DMACS1		R/W			
00010C <sub>H</sub>	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W			
00010D <sub>H</sub>	DMA1 - I/O register address pointer high byte	IOAH1		R/W			
00010E <sub>H</sub>	DMA1 - Data counter low byte	DCTL1	DCT1	R/W			
00010F <sub>H</sub>	DMA1 - Data counter high byte	DCTH1		R/W			
000110 <sub>H</sub>	DMA2 - Buffer address pointer low byte	BAPL2		R/W			
000111 <sub>H</sub>	DMA2 - Buffer address pointer middle byte	BAPM2		R/W			
000112 <sub>H</sub>	DMA2 - Buffer address pointer high byte	BAPH2		R/W			
000113 <sub>H</sub>	DMA2 - DMA control register	DMACS2		R/W			
000114 <sub>H</sub>	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W			
000115 <sub>H</sub>	DMA2 - I/O register address pointer high byte	IOAH2		R/W			
000116 <sub>H</sub>	DMA2 - Data counter low byte	DCTL2	DCT2	R/W			
000117 <sub>H</sub>	DMA2 - Data counter high byte	DCTH2		R/W			
000118 <sub>H</sub>	DMA3 - Buffer address pointer low byte	BAPL3		R/W			
000119 <sub>H</sub>	DMA3 - Buffer address pointer middle byte	BAPM3		R/W			
00011A <sub>H</sub>	DMA3 - Buffer address pointer high byte	BAPH3		R/W			
00011B <sub>H</sub>	DMA3 - DMA control register	DMACS3		R/W			
00011C <sub>H</sub>	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W			
00011D <sub>H</sub>	DMA3 - I/O register address pointer high byte	IOAH3		R/W			
00011E <sub>H</sub>	DMA3 - Data counter low byte	DCTL3	DCT3	R/W			
00011F <sub>H</sub>	DMA3 - Data counter high byte	DCTH3		R/W			
000120 <sub>H</sub> - 00017F <sub>H</sub>	Reserved			-			



### I/O map MB96(F)315x (Sheet 10 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000404 <sub>H</sub>	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405 <sub>H</sub>	Clock Frequency control register High	CKFCRH		R/W
000406 <sub>H</sub>	PLL Control register Low	PLLCRL	PLLCR	R/W
000407 <sub>H</sub>	PLL Control register High	PLLCRH		R/W
000408 <sub>H</sub>	RC clock timer control register	RCTCR		R/W
000409 <sub>H</sub>	Main clock timer control register	MCTCR		R/W
00040A <sub>H</sub>	Sub clock timer control register	SCTCR		R/W
00040B <sub>H</sub>	Reset cause and clock status register with clear function	RCCSRC		R
00040C <sub>H</sub>	Reset configuration register	RCR		R/W
00040D <sub>H</sub>	Reset cause and clock status register	RCCSR		R
00040E <sub>H</sub>	Watch dog timer configuration register	WDTC		R/W
00040F <sub>H</sub>	Watch dog timer clear pattern register	WDTCP		W
000410 <sub>H</sub> - 000414 <sub>H</sub>	Reserved			-
000415 <sub>H</sub>	Clock output activation register	COAR		R/W
000416 <sub>H</sub>	Clock output configuration register 0	COCR0		R/W
000417 <sub>H</sub>	Clock output configuration register 1	COCR1		R/W
000418 <sub>H</sub>	Clock Modulator control register	CMCR		R/W
000419 <sub>H</sub>	Reserved			-
00041A <sub>H</sub>	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
00041B <sub>H</sub>	Clock Modulator Parameter register High	CMPRH		R/W
00041C <sub>H</sub> - 00042B <sub>H</sub>	Reserved			-
00042C <sub>H</sub>	Voltage Regulator Control register	VRCR		R/W
00042D <sub>H</sub>	Clock Input and LVD Control Register	CILCR		R/W
00042E <sub>H</sub> - 00042F <sub>H</sub>	Reserved			-
000430 <sub>H</sub>	I/O Port P00 - Data Direction Register	DDR00		R/W
000431 <sub>H</sub>	I/O Port P01 - Data Direction Register	DDR01		R/W
000432 <sub>H</sub>	I/O Port P02 - Data Direction Register	DDR02		R/W
000433 <sub>H</sub>	I/O Port P03 - Data Direction Register	DDR03		R/W
000434 <sub>H</sub>	Reserved			-



### I/O map MB96(F)315x (Sheet 17 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000588 <sub>H</sub> - 000597 <sub>H</sub>	Reserved			-
000598 <sub>H</sub>	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599 <sub>H</sub>	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
00059A <sub>H</sub>	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
00059B <sub>H</sub>	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
00059C <sub>H</sub>	PPG12 - Timer register		PTMR12	R
00059D <sub>H</sub>	PPG12 - Timer register			R
00059E <sub>H</sub>	PPG12 - Period setting register		PCSR12	W
00059F <sub>H</sub>	PPG12 - Period setting register			W
0005A0 <sub>H</sub>	PPG12 - Duty cycle register		PDUT12	W
0005A1 <sub>H</sub>	PPG12 - Duty cycle register			W
0005A2 <sub>H</sub>	PPG12 - Control status register Low	PCNL12	PCN12	R/W
0005A3 <sub>H</sub>	PPG12 - Control status register High	PCNH12		R/W
0005A4 <sub>H</sub> - 0005AB <sub>H</sub>	Reserved			-
0005AC <sub>H</sub>	PPG14 - Timer register		PTMR14	R
0005AD <sub>H</sub>	PPG14 - Timer register			R
0005AE <sub>H</sub>	PPG14 - Period setting register		PCSR14	W
0005AF <sub>H</sub>	PPG14 - Period setting register			W
0005B0 <sub>H</sub>	PPG14 - Duty cycle register		PDUT14	W
0005B1 <sub>H</sub>	PPG14 - Duty cycle register			W
0005B2 <sub>H</sub>	PPG14 - Control status register Low	PCNL14	PCN14	R/W
0005B3 <sub>H</sub>	PPG14 - Control status register High	PCNH14		R/W
0005B4 <sub>H</sub> - 0005BB <sub>H</sub>	Reserved			-
0005BC <sub>H</sub>	PPG19-PPG16 - General Control register 1 Low	GCN1L4	GCN14	R/W
0005BD <sub>H</sub>	PPG19-PPG16 - General Control register 1 High	GCN1H4		R/W
0005BE <sub>H</sub>	PPG19-PPG16 - General Control register 2 Low	GCN2L4	GCN24	R/W
0005BF <sub>H</sub>	PPG19-PPG16 - General Control register 2 High	GCN2H4		R/W
0005C0 <sub>H</sub>	PPG16 - Timer register		PTMR16	R
0005C1 <sub>H</sub>	PPG16 - Timer register			R





## **12. Interrupt Vector Table**

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC <sub>H</sub>	CALLV0	No	-	
1	3F8 <sub>H</sub>	CALLV1	No	-	
2	3F4 <sub>H</sub>	CALLV2	No	-	
3	3F0 <sub>H</sub>	CALLV3	No	-	
4	3EC <sub>H</sub>	CALLV4	No	-	
5	3E8 <sub>H</sub>	CALLV5	No	-	
6	3E4 <sub>H</sub>	CALLV6	No	-	
7	3E0 <sub>H</sub>	CALLV7	No	-	
8	3DC <sub>H</sub>	RESET	No	-	
9	3D8 <sub>H</sub>	INT9	No	-	
10	3D4 <sub>H</sub>	EXCEPTION	No	-	
11	3D0 <sub>H</sub>	NMI	No	-	Non-Maskable Interrupt
12	3CC <sub>H</sub>	DLY	No	12	Delayed Interrupt
13	3C8 <sub>H</sub>	RC_TIMER	No	13	RC Timer
14	3C4 <sub>H</sub>	MC_TIMER	No	14	Main Clock Timer
15	3C0 <sub>H</sub>	SC_TIMER	No	15	Sub Clock Timer
16	3BC <sub>H</sub>	PLL_UNLOCK	No	16	Reserved
17	3B8 <sub>H</sub>	EXTINT0	Yes	17	External Interrupt 0
18	3B4 <sub>H</sub>				Reserved
19	3B0 <sub>H</sub>	EXTINT2	Yes	19	External Interrupt 2
20	3AC <sub>H</sub>	EXTINT3	Yes	20	External Interrupt 3
21	3A8 <sub>H</sub>	EXTINT4	Yes	21	External Interrupt 4
22	3A4 <sub>H</sub>				Reserved
23	3A0 <sub>H</sub>	EXTINT7	Yes	23	External Interrupt 7
24	39C <sub>H</sub>	EXTINT8	Yes	24	External Interrupt 8
25	398 <sub>H</sub>	EXTINT9	Yes	25	External Interrupt 9
26	394 <sub>H</sub>	EXTINT10	Yes	26	External Interrupt 10
27	390 <sub>H</sub>	EXTINT11	Yes	27	External Interrupt 11
28	38C <sub>H</sub>	EXTINT12	Yes	28	External Interrupt 12
29	388 <sub>H</sub>	EXTINT13	Yes	29	External Interrupt 13
30	384 <sub>H</sub>				Reserved
31	380 <sub>H</sub>				Reserved
32	37C <sub>H</sub>				Reserved
33	378 <sub>H</sub>	CAN2	No	33	CAN Controller 2
34	374 <sub>H</sub>	PPG0	Yes	34	Programmable Pulse Generator 0
35	370 <sub>H</sub>	PPG1	Yes	35	Programmable Pulse Generator 1

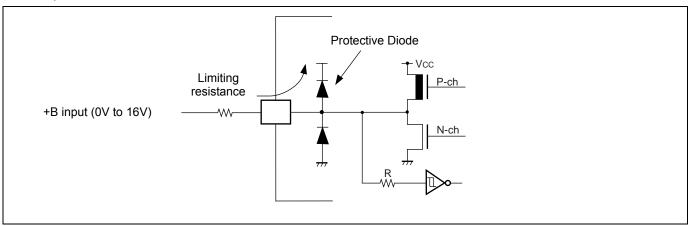




Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
36	36C <sub>H</sub>				Reserved
37	368 <sub>H</sub>	PPG3	Yes	37	Programmable Pulse Generator 3
38	364 <sub>H</sub>	PPG4	Yes	38	Programmable Pulse Generator 4
39	360				Reserved
40	35C <sub>H</sub>	PPG6	Yes	40	Programmable Pulse Generator 6
41	358 <sub>H</sub>	PPG7	Yes	41	Programmable Pulse Generator 7
42	354 <sub>H</sub>	PPG8	Yes	42	Programmable Pulse Generator 8
43	350 <sub>H</sub>	PPG9	Yes	43	Programmable Pulse Generator 9
44	34C <sub>H</sub>				Reserved
45	348 <sub>H</sub>				Reserved
46	344 <sub>H</sub>	PPG12	Yes	46	Programmable Pulse Generator 12
47	340 <sub>H</sub>				Reserved
48	33C <sub>H</sub>	PPG14	Yes	48	Programmable Pulse Generator 14
49	338 <sub>H</sub>				Reserved
50	334 <sub>H</sub>	PPG16	Yes	50	Programmable Pulse Generator 16
51	330 <sub>H</sub>	PPG17	Yes	51	Programmable Pulse Generator 17
52	32C <sub>H</sub>	PPG18	Yes	52	Programmable Pulse Generator 18
53	328 <sub>H</sub>	PPG19	Yes	53	Programmable Pulse Generator 19
54	324 <sub>H</sub>	RLT0	Yes	54	Reload Timer 0
55	320 <sub>H</sub>	RLT1	Yes	55	Reload Timer 1
56	31C <sub>H</sub>	RLT2	Yes	56	Reload Timer 2
57	318 <sub>H</sub>	RLT3	Yes	57	Reload Timer 3
58	314 <sub>H</sub>	PPGRLT	Yes	58	Reload Timer 6 - dedicated for PPG
59	310 <sub>H</sub>	ICU0	Yes	59	Input Capture Unit 0
60	30C <sub>H</sub>	ICU1	Yes	60	Input Capture Unit 1
61	308 <sub>H</sub>				Reserved
62	304 <sub>H</sub>				Reserved
63	300 <sub>H</sub>	ICU4	Yes	63	Input Capture Unit 4
64	2FC <sub>H</sub>	ICU5	Yes	64	Input Capture Unit 5
65	2F8 <sub>H</sub>	ICU6	Yes	65	Input Capture Unit 6
66	2F4 <sub>H</sub>				Reserved
67	2F0 <sub>H</sub>				Reserved
68	2EC <sub>H</sub>	ICU9	Yes	68	Input Capture Unit 9
69	2E8 <sub>H</sub>	ICU10	Yes	69	Input Capture Unit 10
70	2E4 <sub>H</sub>				Reserved
71	2E0 <sub>H</sub>				Reserved
72	2DC <sub>H</sub>				Reserved



- \*1: AV<sub>CC</sub> and V<sub>CC</sub> must be set to the same voltage. It is required that AV<sub>CC</sub> does not exceed V<sub>CC</sub> and that the voltage at the analog inputs does not exceed AV<sub>CC</sub> neither when the power is switched on.
- \*2: V<sub>I</sub> and V<sub>O</sub> should not exceed V<sub>CC</sub> + 0.3 V. V<sub>I</sub> should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I<sub>CLAMP</sub> rating supersedes the V<sub>I</sub> rating. Input/output voltages of standard ports depend on V<sub>CC</sub>.
- \*3: Applicable to all general purpose I/O pins (Pnn\_m)
  - Use within recommended operating conditions.
  - Use at DC voltage (current)
  - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
  - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
  - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
  - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
  - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage
    may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).
  - Sample recommended circuits:



\*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.

The actual power dissipation depends on the customer application and can be calculated as follows:

 $P_D = P_{IO} + P_{INT}$ 

 $P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} * I_{OH})$  (IO load power dissipation, sum is performed on all IO ports)

 $P_{INT} = V_{CC} * (I_{CC} + I_A)$  (internal power dissipation)

 $I_{CC}$  is the total core current consumption into  $V_{CC}$  as described in the "3. DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.  $I_A$  is the analog current consumption into AV<sub>CC</sub>.

- \*5: Worst case value for a package mounted on single layer PCB at specified T<sub>A</sub> without air flow.
- \*6: Please contact Cypress for reliability limitations when using under these conditions.
- WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.



### 14.2 Recommended Operating Conditions

Parameter	Symbol Value				Unit	Remarks	
Fardineter	Symbol	Min	Тур	Max	Unit	Kelliarks	
Power supply voltage	V <sub>CC</sub>	3.0	-	5.5	V		
Smoothing capacitor at C pin	C <sub>S</sub>	3.5	4.7	15	μF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



Parameter	Symbol	Condition (at T <sub>A</sub> )		Va	lue	Unit	Remarks
i arameter	Gymbol		Тур	Max	onit	Remarks	
		PLL Run mode with CLKS1/2 = CLKB =	+25°C	14.5	19.5		
		CLKP1 = 16MHz, CLKP2 = 8MHz	. 10500	4.0		mA	
		1 Flash/ROM wait state	+125°C	16	23		
		(CLKRC and CLKSC stopped)					
		PLL Run mode with CLKS1/2 = CLKB =	+25°C	23	29		
		CLKP1 = 32MHz, CLKP2 = 16MHz				mA	
		2 Flash/ROM wait states	+125°C	25	33		
	I <sub>CCPLL</sub>	(CLKRC and CLKSC stopped)					
		PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz	+25°C	26	38		
Power supply current in		0 Flash/ROM wait states	+125°C	28	42	mA	
Run modes*		(CLKRC and CLKSC stopped)	125 0	20	72		
		PLL Run mode with	+25°C	40	51		
		CLKS1/2 = CLKB = CLKP1= 56MHz,					
		CLKP2 = 28MHz				mA	
		2 Flash/ROM wait states	+125°C	42	55		
		(CLKRC and CLKSC stopped. Core voltage at 1.9V)					
		PLL Run mode with CLKS1/2 = 96MHz,	+25°C	43	56		
		CLKB = CLKP1= 48MHz, CLKP2 = 24MHz				mA	
		1 Flash/ROM wait state	+125°C	45	60		
		(CLKRC and CLKSC stopped. Core voltage at 1.9V)					

# (T<sub>A</sub> = -40°C to 125°C, V<sub>CC</sub> = AV<sub>CC</sub> = 3.0V to 5.5V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V)



Devenueter	Cumula al	Condition (at T₄)	Va	lue	Unit	Domoska			
Parameter	Symbol			Тур	Мах	Unit	Remarks		
		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz	+25°C	4	5				
	I <sub>CCMAIN</sub>	1 Flash/ROM wait state (CLKPLL, CLKSC and CLKRC stopped)	+125°C	4.7	8	mA			
		RC Run mode with CLKS1/2 = CLKB =	+25°C	2.5	3.5				
	I <sub>CCRCH</sub>	CLKP1/2 = 2MHz 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped)	+125°C	3.2	6.5	mA			
		RC Run mode with CLKS1/2 = CLKB =	+25°C	0.18	0.3				
Power supply current in Run modes*	I <sub>CCRCL</sub>	CLKP1/2 = 100kHz, SMCR:LPMS = 0 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+125°C	0.73	3.1	mA			
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz,	+25°C	0.15	0.25				
		SMCR:LPMS = 1 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/ erasing allowed)	+125°C	0.7	3.05	mA			
		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz	+25°C	0.1	0.2				
	I <sub>CCSUB</sub>	1 Flash/ROM wait state				mA			
		(CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+125°C	0.65	0.65 3				

(T<sub>A</sub> = -40°C to 125°C, V<sub>CC</sub> = AV<sub>CC</sub> = 3.0V to 5.5V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V)





#### 14.4 AC Characteristics

### Source Clock timing

(T<sub>A</sub> = -40°C to 125°C, V<sub>CC</sub> = AV<sub>CC</sub> = 3.0V to 5.5V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V)

Parameter	Symbol	Pin		Value		Unit	Remarks
Parameter	Symbol	Pin	Min	Тур	Мах	Unit	Remarks
			3	-	16	MHz	When using a crystal oscillator, PLL off
Clock frequency	f <sub>C</sub>	X0, X1	0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f <sub>FCI</sub>	X0	0	-	56	MHz	When using a single phase external clock in "Fast Clock Input mode" , PLL off
Clock nequency	'FCI	70	3.5	-	56	MHz	When using a single phase external clock in "Fast Clock Input mode" , PLL on
	f <sub>CL</sub>	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
Clock frequency			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f <sub>CR</sub>		50	100	200	kHz	When using slow frequency of RC oscillator
Clock frequency		-	1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t <sub>RCSTAB</sub>	-	256 RC clock cycles			Applied after any reset and when activating the RC oscillator.	
PLL Clock frequency	f <sub>CLKVCO</sub>	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T <sub>PSKEW</sub>	-	-	-	± 5	ns	For CLKMC (PLL input clock)   4MHz, jitter coming from external oscillator, crystal or resonator is not covered
Input clock pulse width	P <sub>WH</sub> , P <sub>WL</sub>	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	$P_{WHL}, P_{WLL}$	X0A,X1A	5	-	-	μs	

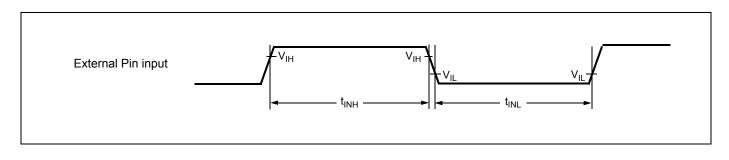


### **External Input timing**

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function		
Falametei	Symbol	FIII	Condition	Min	Мах	Unit	Osed Pin input function		
		INTn(_R)	$\begin{array}{c} 200 \\ 2^{*}t_{CLKP1} + 200 \\ (t_{CLKP1} = 1/f_{CLKP1}) \end{array}$			200			External Interrupt
		NMI		200		ns	NMI		
		Pnn_m		2*t <sub>CLKP1</sub> + 200 (t <sub>CLKP1</sub> =1/f <sub>CLKP1</sub> )	_	ns	General Purpose IO		
Input pulse width	t <sub>INH</sub> t <sub>INL</sub>	TINn					Reload Timer		
		TTGn(_R)					PPG Trigger input		
		ADTG_R					AD Converter Trigger		
	F	INn					Input Capture		

(T<sub>A</sub> = -40°C to 125°C, V<sub>CC</sub> = AV<sub>CC</sub> = 3.0V to 5.5V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V)

Note : Relocated Resource Inputs have same characteristics







### 14.5 Analog Digital Converter

	Symbol	Pin	Value				
Parameter			Min	Тур	Max	Unit	Remarks
Resolution	-	-	-	-	10	bit	
Total error	-	-	-	-	± 3	LSB	
Nonlinearity error	-	-	-	-	± 2.5	LSB	
Differential nonlinearity error	-	-	-	-	± 1.9	LSB	
Zero transition voltage	V <sub>OT</sub>	ANn	AVRL-1.5 LSB	AVRL+ 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale transition voltage	V <sub>FST</sub>	ANn	AVRH - 3.5 LSB	AVRH - 1.5 LSB	AVRH + 0.5 LSB	V	
Comparo timo	-	-	1.0	-	16,500	μS	$4.5V \leq AV_{CC} \leq 5.5V$
Compare time			2.0	-	-	μS	$3.0V \leq AV_{CC} < 4.5V$
	-	-	0.5	-	-	μS	$4.5V \leq AV_{CC} \leq 5.5V$
Sampling time			1.2	-	-	μS	$3.0V \leq AV_{CC} < 4.5V$
Analog input leakage current (during conversion)	I <sub>AIN</sub>	ANn	-1	-	+1	μA	$\begin{array}{l} T_A \leq 105 \ ^\circ C, \\ AV_{SS}, \ AVRL < V_I < AV_{CC}, \\ AVRH \end{array}$
			-1.2	-	+1.2	μA	105 °C < T <sub>A</sub> $\leq$ 125 °C, AV <sub>SS</sub> , AVRL < V <sub>I</sub> < AV <sub>CC</sub> , AVRH
Analog input voltage range	V <sub>AIN</sub>	ANn	AVRL	-	AVRH	V	
	AVRH	AVRH	0.75 AVcc	-	AVcc	V	
Reference voltage range	AVRL	AVRL	AV <sub>SS</sub>	-	$0.25  \text{AV}_{\text{CC}}$	V	
	Ι <sub>Α</sub>	AVcc	-	2.5	5	mA	A/D Converter active
Power supply current	I <sub>AH</sub>	AVcc	-	-	5	μA	A/D Converter not operated
Reference voltage current	I <sub>R</sub>	AVRH/AVR L	-	0.7	1	mA	A/D Converter active
	I <sub>RH</sub>	AVRH/AVR L	-	-	5	μA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

(T<sub>A</sub> = -40 °C to +125 °C, 3.0 V  $\leq$  AVRH - AVRL, V<sub>CC</sub> = AV<sub>CC</sub> = 3.0V to 5.5V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V)

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.





#### 14.7 FLASH memory program/erase characteristics

## (T<sub>A</sub> = -40°C to 105°C, V<sub>CC</sub> = AV<sub>CC</sub> = 3.0V to 5.5V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V)

Parameter	Value			Unit	Remarks
Falanietei	Min	Тур	Max	Onit	Remarks
Sector erase time	-	0.9	3.6	S	Without erasure pre-programming time
Chip erase time	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Word (16-bit width) programming time	-	23	370	us	Without overhead time for submitting write command
Program/Erase cycle	10000	-	-	cycle	
Flash data retention time	20	-	-	year	*1

\*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)



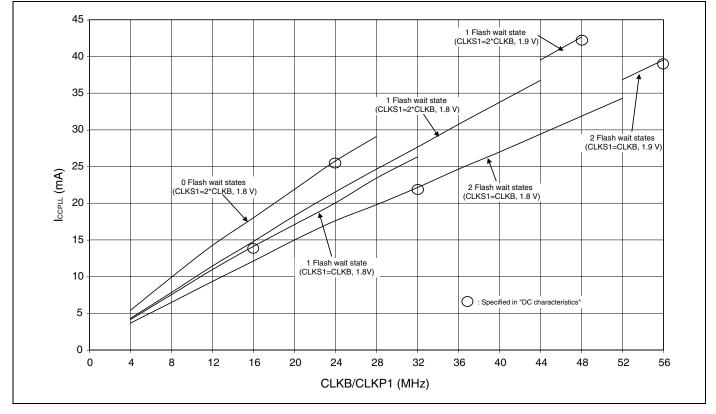
#### 15.2 Frequency dependency of power supply currents in PLL Run mode

The following diagrams show the current consumption of samples with typical wafer process parameters in PLL Run mode at different frequencies and Flash timing settings.

Measurement conditions:

- $V_{CC} = AV_{CC} = 5.0V$
- Ta = 25°C
- +  $f_{CLKS1} = f_{CLKB}$  or  $f_{CLKS1} = 2*f_{CLKB}$  as described in diagram
- $f_{CLKS2} = f_{CLKS1}$
- f<sub>CLKP1</sub> = f<sub>CLKB</sub>
- $f_{CLKP2} = f_{CLKB}/2$
- Core voltage at 1.8V (VRCR:HPM[1:0] = 10<sub>B</sub>) or 1.9V (VRCR:HPM[1:0] = 11<sub>B</sub>) as described in diagram
- Main clock = 4MHz external clock
- · Flash memory timing settings:
- MTCRA=2128<sub>H</sub>/2208<sub>H</sub> (0 Flash wait states,  $f_{CLKS1} = 2*f_{CLKB}$ )
- MTCRA=0239<sub>H</sub>/2129<sub>H</sub> (1 Flash wait state, f<sub>CLKS1</sub> = f<sub>CLKB</sub>)
- MTCRA=4C09<sub>H</sub>/6B09<sub>H</sub> (1 Flash wait state,  $f_{CLKS1} = 2*f_{CLKB}$ )
- MTCRA=233A<sub>H</sub> (2 Flash wait states, f<sub>CLKS1</sub> = f<sub>CLKB</sub>)
- Average Flash access rate (number of read accesses to the Flash per CLKB clock cycle, no buffer hit):
- 0 Flash wait states: 0.5
- 1 Flash wait states: 0.33
- 2 Flash wait states: 0.25

#### MB96F313/F315 PLL Run mode currents





# **Document History**

Document Title: MB96310 Series F <sup>2</sup> MC-16FX 16-bit Proprietary Microcontroller Document Number: 002-04592					
Revision	ECN	Orig. of Change	Submission Date	Description of Change	
**	_	AKIH		Migrated to Cypress and assigned document number 002-04592. No change to document contents or format.	
*A	5230360	AKIH	04/22/2016	Updated to Cypress template	



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