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What is "Embedded - Microcontrollers"?

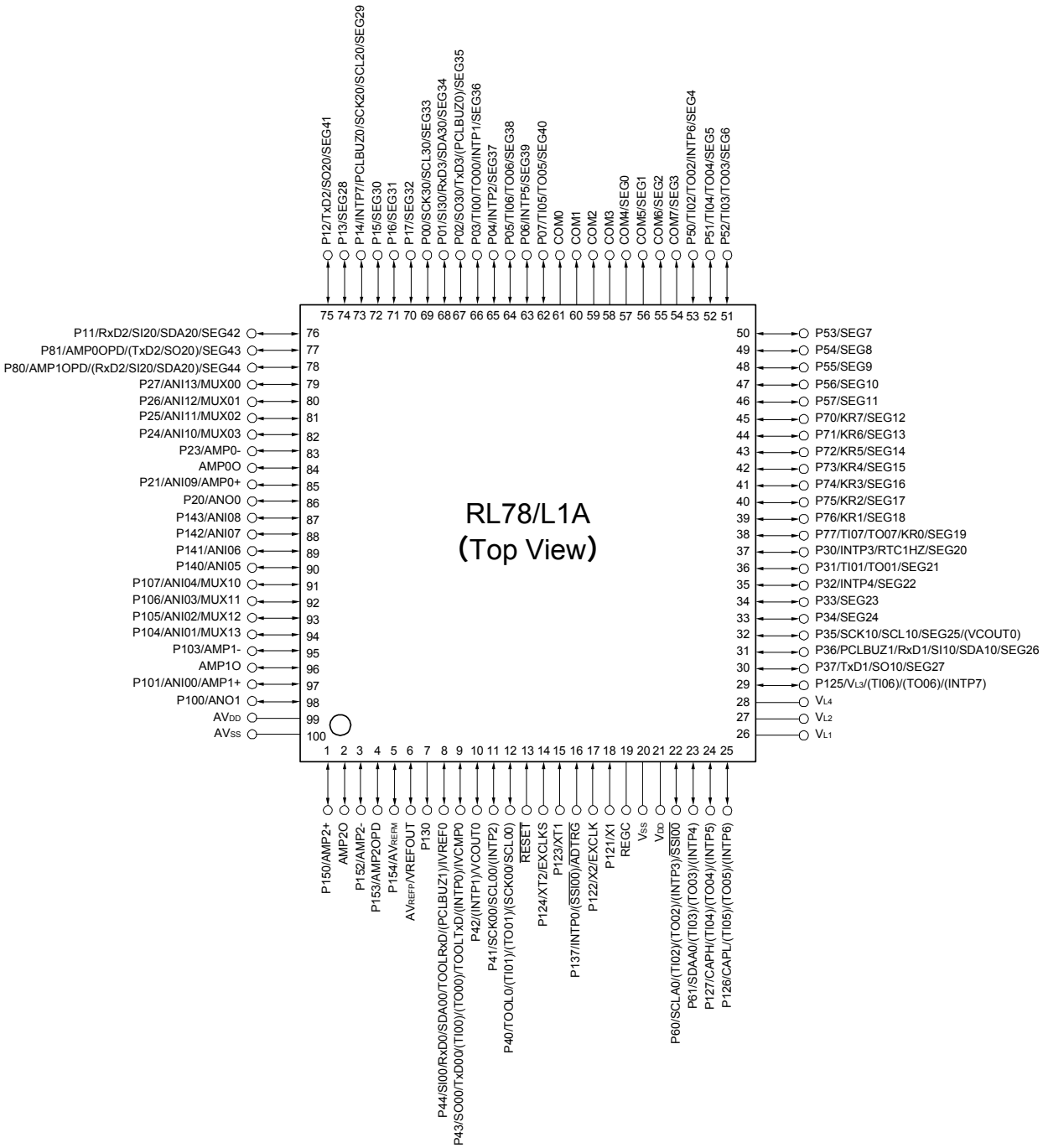
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, LINbus, SPI, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11mmfafb-30

1.3.2 100-pin products

• 100-pin plastic LFQFP (fine pitch) (14 × 14 mm, 0.5 mm pitch)



Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

(2/2)

Item			80-pin	100-pin
			R5F11MMx (x = D to F)	R5F11MPx (x = E to G)
Clock output/buzzer output			2	2
			• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
12-bit resolution A/D converter			10 channels	14 channels
12-bit resolution D/A converter			2 channels	2 channels
VREFOUT (voltage reference)			2.5 V/2.048 V/1.8 V/1.5 V	
Operational amplifier			3 channels	3 channels
	AMPnO with analog MUX switch		2 channels (2 in-out/channel)	2 channels (4 in-out/channel)
Comparator			1 channel	1 channel
Serial interface			• CSI (SPI supported): 1 channel/UART (LIN-bus supported): 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel	
	I^2C bus		1 channel	1 channel
LCD controller/driver			Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.	
	Segment signal output		32 (28) Note 1	45 (41) Note 1
	Common signal output		4 (8) Note 1	
Data transfer controller (DTC)			30 sources	30 sources
Event link controller (ELC)			Event input: 22, Event trigger output: 8	Event input: 22, Event trigger output: 8
Vectored interrupt sources		Internal	31	31
		External	9	9
Key interrupt			8	8
Reset			• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note 2 • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit			• Power-on-reset: 1.51 ±0.04 V • Power-down-reset: 1.50 ±0.04 V	
Voltage detector			• Rising edge: 1.88 V to 3.13 V (10 stages) • Falling edge: 1.84 V to 3.06 V (10 stages)	
On-chip debug function			Provided	
Power supply voltage			V_{DD} = 1.8 to 3.6 V	
Operating ambient temperature			T_A = -40 to +85 °C (A: Consumer applications)	

Note 1. The number in parentheses indicates the number of signal outputs when 8 coms are used.

Note 2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS (A: T_A = -40 to +85 °C)

This chapter describes the electrical specifications for the products A: Consumer applications (T_A = -40 to +85 °C).

Caution 1. The RL78 microcontroller has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 With functions for each product in the RL78/L1A User's Manual.

Absolute Maximum Ratings (T_A = 25°C) **(2/3)**

Parameter	Symbols	Conditions		Ratings	Unit
LCD voltage	V_{LI1}	V_{L1} input voltage Note 1		-0.3 to +2.8	V
	V_{LI2}	V_{L2} input voltage Note 1		-0.3 to +6.5	V
	V_{LI3}	V_{L3} input voltage Note 1		-0.3 to +6.5	V
	V_{LI4}	V_{L4} input voltage Note 1		-0.3 to +6.5	V
	V_{LI5}	CAPL, CAPH input voltage Note 1		-0.3 to +6.5	V
	V_{LO1}	V_{L1} output voltage		-0.3 to +2.8	V
	V_{LO2}	V_{L2} output voltage		-0.3 to +6.5	V
	V_{LO3}	V_{L3} output voltage		-0.3 to +6.5	V
	V_{LO4}	V_{L4} output voltage		-0.3 to +6.5	V
	V_{LO5}	CAPL, CAPH output voltage		-0.3 to +6.5	V
	V_{LO6}	COM0 to COM7 SEG0 to SEG44 output voltage	External resistance division method	-0.3 to V_{DD} + 0.3 Note 2	V
			Capacitor split method	-0.3 to V_{DD} + 0.3 Note 2	V
			Internal voltage boosting method	-0.3 to V_{LI4} + 0.3 Note 2	V

Note 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 ± 30%) and connect a capacitor (0.47 ± 30%) between the CAPL and CAPH pins.

Note 2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Absolute Maximum Ratings (T_A = 25°C) **(3/3)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin		-40	mA
		Total of all pins -170 mA	P40 to P44	-70	mA
			P00 to P07, P11 to P17, P30 to P37, P50 to P57, P70 to P77, P80, P81, P125 to P127, P130	-100	mA
	I_{OH2}	Per pin	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154	-0.1	mA
		Total of all pins		-1.6 Note	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins 170 mA	P40 to P44	70	mA
			P00 to P07, P11 to P17, P30 to P37, P50 to P57, P60, P61, P70 to P77, P80, P81, P125 to P127, P130	100	mA
	I_{OL2}	Per pin	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154	0.4	mA
		Total of all pins		6.4 Note	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Note Do not exceed the rated values when outputting the current simultaneously 16 pins at maximum.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85 °C, 1.8 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P07, P11 to P17, P30 to P37, P40 to P44, P50 to P57, P60, P61, P70 to P77, P80, P81, P125 to P127, P137, _RESET	V_I = V_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
	I_{LIH4}	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154	V_I = AV_{DD}				1	μA
Input leakage current, low	I_{LIL1}	P00 to P07, P11 to P17, P30 to P37, P40 to P44, P50 to P57, P60, P61, P70 to P77, P80, P81, P125 to P127, P137, _RESET	V_I = V_{SS}				-1	μA
	I_{LIL3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I = V_{SS}	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
	I_{LIL4}	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154	V_I = AV_{SS}				-1	μA
On-chip pull-up resistance	R_{U1}	P00 to P07, P11 to P17, P30 to P37, P50 to P57, P70 to P77, P80, P81, P125 to P127	V_I = V_{SS}	2.4 V ≤ V_{DD} ≤ 3.6 V	10	20	100	kΩ
				1.8 V ≤ V_{DD} < 2.4 V	10	30	100	
	R_{U2}	P40 to P44	V_I = V_{SS}		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = -40 to +85 °C, 1.8 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 3.6 V			1.7		mA
						V_{DD} = 3.0 V			1.7		
					Normal operation	V_{DD} = 3.6 V			3.6	6.1	
						V_{DD} = 3.0 V			3.6	6.1	
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 3.6 V			2.7	4.7	
						V_{DD} = 3.0 V			2.7	4.7	
			LS (low-speed main) mode Note 5	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.6 V			1.2	2.1	mA
						V_{DD} = 3.0 V			1.2	2.1	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 3.6 V	Normal operation	Square wave input			3.0	5.1	mA
						Resonator connection			3.2	5.2	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input			2.9	5.1	
						Resonator connection			3.2	5.2	
				f_{MX} = 16 MHz Note 2, V_{DD} = 3.6 V	Normal operation	Square wave input			2.5	4.4	
						Resonator connection			2.7	4.5	
				f_{MX} = 16 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input			2.5	4.4	
						Resonator connection			2.7	4.5	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.6 V	Normal operation	Square wave input			1.9	3.0	
						Resonator connection			1.9	3.0	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input			1.9	3.0	
						Resonator connection			1.9	3.0	
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.6 V	Normal operation	Square wave input			1.1	2.0	mA
						Resonator connection			1.1	2.0	
				f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input			1.1	2.0	
						Resonator connection			1.1	2.0	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input			4.0	5.4	μA
						Resonator connection			4.3	5.4	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input			4.0	5.4	
						Resonator connection			4.3	5.4	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input			4.1	7.1	
						Resonator connection			4.4	7.1	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input			4.3	8.7	
						Resonator connection			4.7	8.7	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input			4.7	12.0	
						Resonator connection			5.2	12.0	

(Notes and Remarks are listed on the next page.)

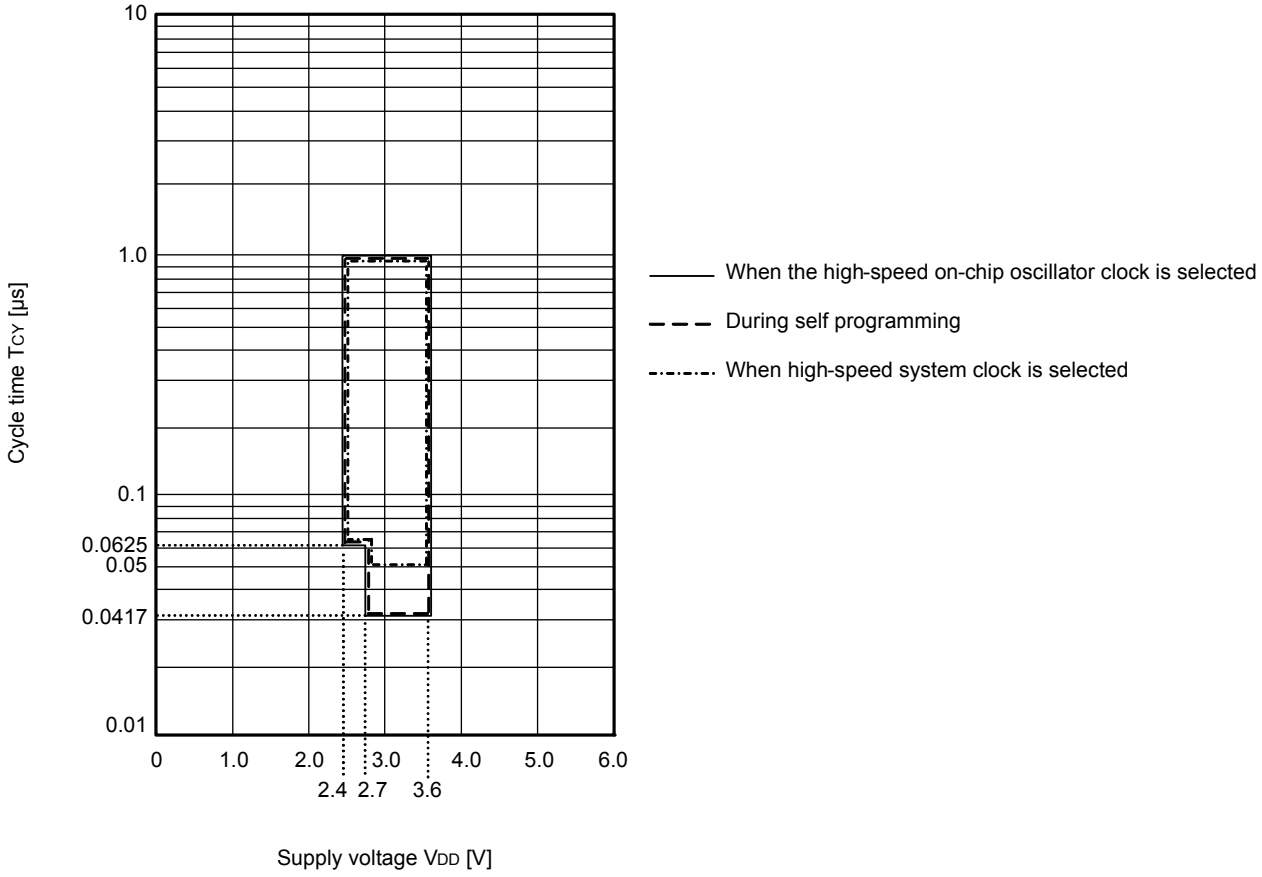
(T_A = -40 to +85 °C, 1.8 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{IH} = 24 MHz Note 4	V_{DD} = 3.6 V		0.42	1.83	mA
					V_{DD} = 3.0 V		0.42	1.83	
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.39	1.38	
					V_{DD} = 3.0 V		0.39	1.38	
			LS (low-speed main) mode Note 7	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		0.25	0.71	mA
					V_{DD} = 2.0 V		0.25	0.71	
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 3.6 V	Square wave input		0.26	1.55	mA
					Resonator connection		0.4	1.68	
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.25	1.55	
					Resonator connection		0.4	1.68	
				f_{MX} = 16 MHz Note 3, V_{DD} = 3.6 V	Square wave input		0.23	1.22	
					Resonator connection		0.36	1.39	
				f_{MX} = 16 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.22	1.22	
					Resonator connection		0.35	1.39	
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.18	0.82	
					Resonator connection		0.28	0.90	
				f_{MX} = 10 MHz Note 3, V_{DD} = 2.0 V	Square wave input		0.18	0.81	
					Resonator connection		0.28	0.89	
			LS (low-speed main) mode Note 7	f_{MX} = 8 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.09	0.51	mA
					Resonator connection		0.15	0.56	
				f_{MX} = 8 MHz Note 3, V_{DD} = 2.0 V	Square wave input		0.10	0.52	
					Resonator connection		0.15	0.57	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A = -40°C	Square wave input		0.32	0.75	μA
					Resonator connection		0.51	0.83	
				f_{SUB} = 32.768 kHz Note 5 T_A = +25°C	Square wave input		0.41	0.83	
					Resonator connection		0.62	1.00	
				f_{SUB} = 32.768 kHz Note 5 T_A = +50°C	Square wave input		0.52	1.17	
					Resonator connection		0.75	1.36	
				f_{SUB} = 32.768 kHz Note 5 T_A = +70°C	Square wave input		0.82	1.97	
					Resonator connection		1.08	2.16	
				f_{SUB} = 32.768 kHz Note 5 T_A = +85°C	Square wave input		1.38	3.37	
					Resonator connection		1.62	3.56	
	I_{DD3} Note 6	STOP mode Note 8	T_A = -40°C				0.16	0.51	μA
			T_A = +25°C				0.22	0.51	
			T_A = +50°C				0.27	1.10	
			T_A = +70°C				0.37	1.90	
			T_A = +85°C				0.6	3.30	

(Notes and Remarks are listed on the next page.)

Minimum Instruction Execution Time during Main System Clock Operation

TCY vs VDD (HS (high-speed main) mode)



(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq f_{CLK}/2$	2.7 V ≤ V_{DD} ≤ 3.6 V	167		250		ns
SCKp high-/low-level width	t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V		$t_{KCY1}/2$ - 10		$t_{KCY1}/2$ - 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V		33		110		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 20 pF Note 4			10		10	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 4)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85 °C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 3.6 V	f_{MCK} > 16 MHz	8/f_{MCK}		—		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		6/f_{MCK} and 750		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} ≤ 3.6 V		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		t_{KCY2}/2 - 18		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	2.4 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 3.6 V		2/f_{MCK} + 44		2/f_{MCK} + 110	ns
			2.4 V ≤ V_{DD} ≤ 3.6 V		2/f_{MCK} + 75		2/f_{MCK} + 110	ns
			1.8 V ≤ V_{DD} ≤ 3.6 V		—		2/f_{MCK} + 110	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

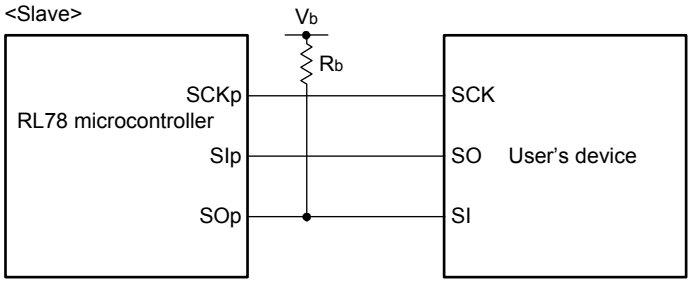
Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 4, 8)

Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode connection diagram (during communication at different potential)

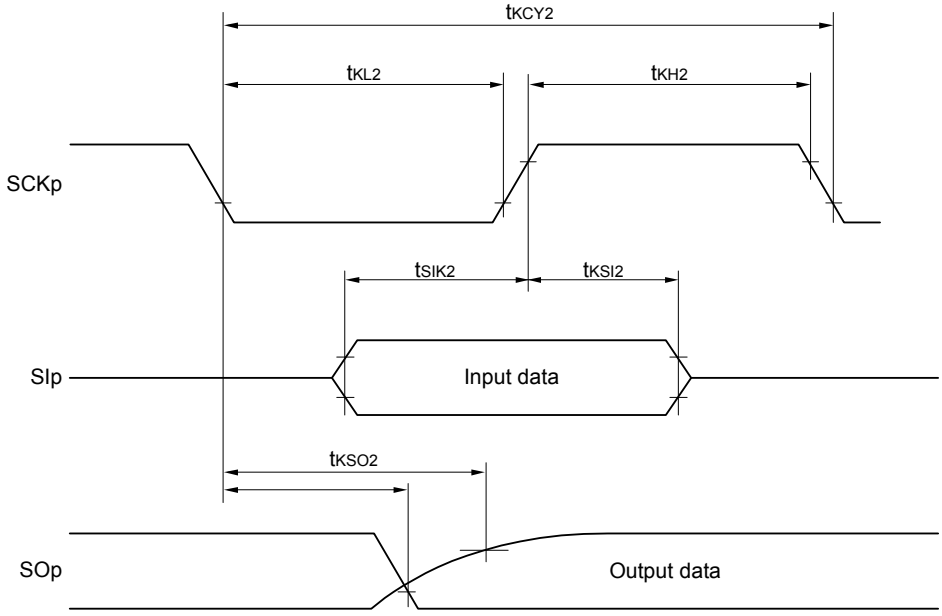


Remark 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

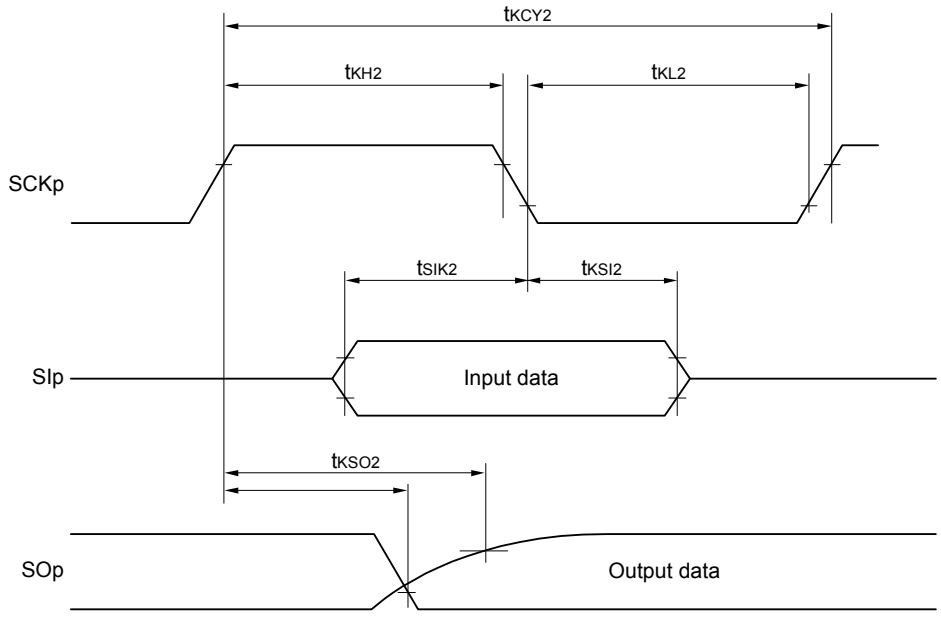
Remark 2. p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 4, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10, 12))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

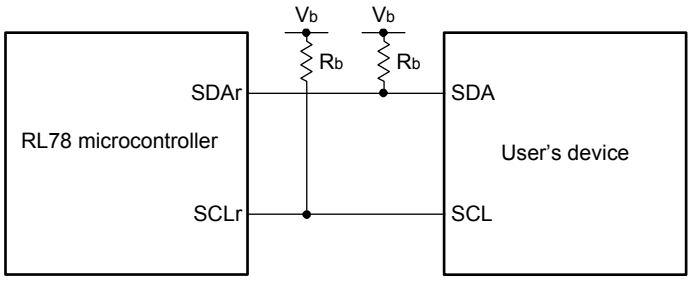


CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

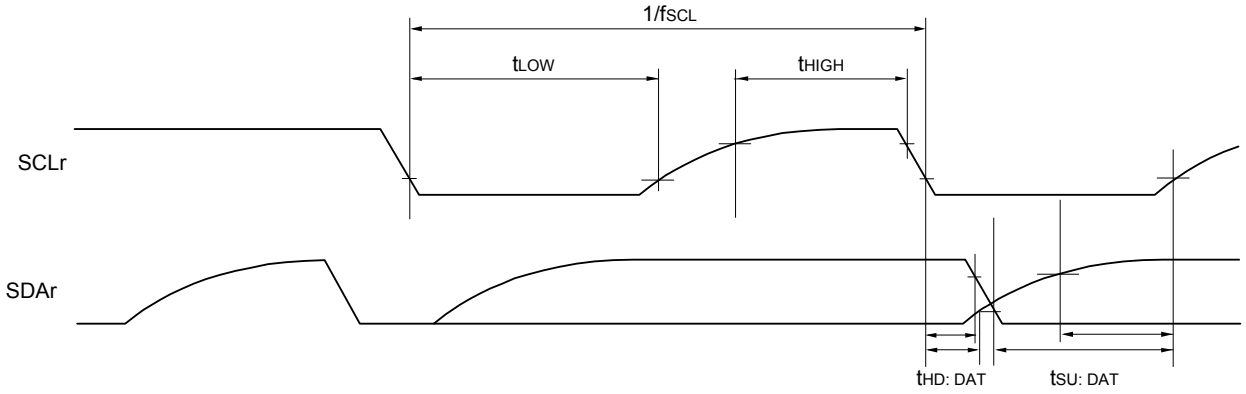


Remark p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 4, 8)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 10, 20, 30), g: PIM, POM number (g = 0, 1, 3, 4, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10, 12)

(2) I^2C fast mode

(T_A = -40 to +85 °C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ V_{DD} ≤ 3.6 V	0	400	0	400	kHz
			1.8 V ≤ V_{DD} ≤ 3.6 V	0	400	0	400	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		0.6		μs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		0.6		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		1.3		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		0.6		μs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		100		100		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0	0.9	0	0.9	μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		0	0.9	μs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		0.6		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Full-scale error	EFS	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±0.75	±4.5	LSB
			2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±0.75	±4.5	LSB
		Normal mode ADCSR.ADHSC = 1 ADSSTRn = 28H	2.7 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±0.75	±4.5	LSB
			2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±0.75	±4.5	LSB
			1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±1.5	±7.5	LSB
Differential linearity error	DLE	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±1.0	—	LSB
			2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±1.0	—	LSB
		Normal mode ADCSR.ADHSC = 1 ADSSTRn = 28H	2.7 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±1.0	—	LSB
			2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±1.0	—	LSB
			1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±1.0	—	LSB
Integral linearity error	ILE	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±1.0	±3.0	LSB
			2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±1.0	±4.5	LSB
		Normal mode ADCSR.ADHSC =1 ADSSTRn = 28H	2.7 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±1.0	±3.0	LSB
			2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±1.0	±3.0	LSB
			1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—	±1.0	±3.0	LSB

Note The characteristics above only apply when pins other than those of the A/D converter are not in use. The overall error includes the quantization error. Each of the offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error does not include the quantization error.

[Reference value for design (not guaranteed)]

We can provide the design reference values for the A/D converter. Note, however, that these values are not guaranteed and can only be used as a reference when using this function. See below for details.

T_A = 0 to +50°C, 2.0 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V, reference voltage(+) = AV_{REFP}, reference voltage(–) = AV_{REFM} = 0 V

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution	RES			—	—	—Note 3	bit
Analog capacitance	Cs			—	—	—Note 3	pF
Analog input resistance	Rs			—	—	—Note 3	kΩ
Frequency	f_{CLK}	High-speed mode	2.7 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—Note 3	—	—Note 3	MHz
			2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—Note 3	—	—Note 3	MHz
		Normal mode	2.7 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—Note 3	—	—Note 3	MHz
			2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—Note 3	—	—Note 3	MHz
			2.0 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V	—Note 3	—	—Note 3	MHz

2.6.5 Rail to rail Operational amplifier characteristics

(T_A = -40 to +85 °C, 2.2 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Circuit current	Icc1	Low-power consumption mode		—	10	16	μA
	Icc2	High-speed mode		—	210	350	μA
Common mode input range	Vicm1	Low-power consumption mode		0.1	—	AV_{DD}-0.1	V
	Vicm2	High-speed mode		0.1	—	AV_{DD}-0.1	V
Output voltage range	Vo1	Low-power consumption mode		0.1	—	AV_{DD}-0.1	V
	Vo2	High-speed mode		0.1	—	AV_{DD}-0.1	V
Input offset voltage	Fioff	Low-power consumption mode		-10	—	10	mV
		High-speed mode		-5	—	5	mV
Open gain	Av			—	120	—	dB
Gain-bandwidth (GB) product	GBW1	Low-power consumption mode		—	0.06	—	MHz
	GBW2	High-speed mode		—	1	—	MHz
Phase margin	PM	CL = 22 pF		50	—	—	deg
Gain margin	GM	CL = 20 pF		10	—	—	dB
Equivalent input noise	Vnoise1	f = 1 kHz	Low-power consumption mode	—	900	—	nV/√Hz
	Vnoise2	f = 10 kHz		—	450	—	nV/√Hz
	Vnoise3	f = 1 kHz	High-speed mode	—	80	—	nV/√Hz
	Vnoise4	f = 2 kHz		—	50	—	nV/√Hz
Power supply reduction ratio	PSRR			—	90	—	dB
Common mode signal reduction ratio	CMPR			—	90	—	dB
Operation stabilization wait time	Tturn1	CL = 20 pF	Low-power consumption mode	—	110	300	μs
	Tturn2	CL = 20 pF	High-speed mode	—	5	14	μs
Settling time	Tset1	CL = 20 pF	Low-power consumption mode	—	100	300	μs
	Tset2	CL = 20 pF	High-speed mode	—	4	14	μs
Slew rate	Tselw1	CL = 20 pF	Low-power consumption mode	0.01	0.04	—	V/μs
	Tselw2	CL = 20 pF	High-speed mode	0.3	0.7	—	V/μs
Load current	Iload1	Low-power consumption mode		-110	—	110	μA
	Iload2	High-speed mode		-110	—	110	μA
Load capacitance	CL			—	—	22	pF
Analog MUX ON resistance	Ron	One channel		—	—	1	kΩ

2.8 LCD Characteristics

2.8.1 Resistance division method

(1) Static display mode

(T_A = -40 to +85 °C, V_{L4} (MIN.) ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

(2) 1/2 bias method, 1/4 bias method

(T_A = -40 to +85 °C, V_{L4} (MIN.) ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

(T_A = -40 to +85 °C, V_{L4} (MIN.) ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}	V

(2) 1/4 bias method

(T_A = -40 to +85 °C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C5 Note 1 = 0.47 μF Note 2	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V_{L2}	C1 to C5 Note 1 = 0.47 μF		2 V_{L1} - 0.08	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L3}	C1 to C5 Note 1 = 0.47 μF		3 V_{L1} - 0.12	3 V_{L1}	3 V_{L1}	V
Quadruply output voltage	V_{L4}	C1 to C5 Note 1 = 0.47 μF		4 V_{L1} - 0.16	4 V_{L1}	4 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C5 Note 1 = 0.47μF		500			ms

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L3} and GND
C5: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = C5 = 0.47 μF±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

2.8.3 Capacitor split method

(1) 1/3 bias method

(T_A = -40 to +85 °C, 2.2 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 = 0.47 μF Note 2		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C4 = 0.47 μF Note 2	2/3 V_{L4} - 0.1	2/3 V_{L4}	2/3 V_{L4} + 0.1	V
V_{L1} voltage	V_{L1}	C1 to C4 = 0.47 μF Note 2	1/3 V_{L4} - 0.1	1/3 V_{L4}	1/3 V_{L4} + 0.1	V
Capacitor split wait time Note 1	t_{VWAIT}		100			ms

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 2. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 μF±30%