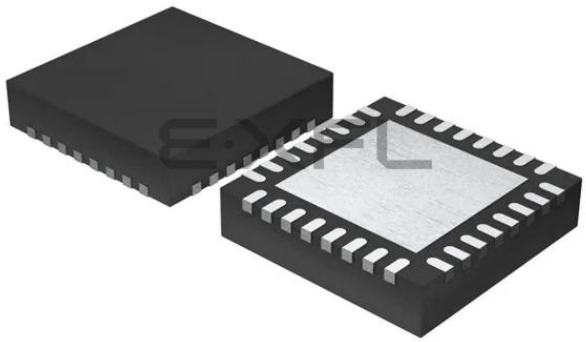

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount, Wettable Flank
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f82733mfm

- Up to 64 KB program/data flash memory
- Up to 8 KB dual port data/program RAM

1.5 Interrupt Controller

- Five interrupt priority levels
  - Three user-programmable priority levels for each interrupt source: level 0, level 1, level 2
  - Unmaskable level 3 interrupts include illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Interrupt level 3 is highest priority and non-maskable. Its sources include:
    - Illegal instructions
    - Hardware stack overflow
    - SWI instruction
    - EOnce interrupts
    - Misaligned data accesses
  - Lowest-priority software interrupt: level LP
- Support for nested interrupts, so that a higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level is managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.6 Peripheral highlights

1.6.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- 16 bits of resolution for center, edge-aligned, and asymmetrical PWMs
- PWM outputs can be configured as complementary output pairs or independent outputs
- Dedicated time-base counter with period and frequency control per submodule
- Independent top and bottom deadtime insertion for each complementary pair
- Independent control of both edges of each PWM output
- Enhanced input capture and output compare functionality on each input:
  - Channels not used for PWM generation can be used for buffered output compare functions.

    - Channels not used for PWM generation can be used for input capture functions.
    - Enhanced dual edge capture functionality
- Synchronization of submodule to external hardware (or other PWM) is supported.
- Double-buffered PWM registers
    - Integral reload rates from 1 to 16
    - Half-cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware.
- Support for double-switching PWM outputs
- Up to eight fault inputs can be assigned to control multiple PWM outputs
    - Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Individual software control of each PWM output
- All outputs can be programmed to change simultaneously via a FORCE_OUT event.
- PWMX pin can optionally output a third PWM signal from each submodule
- Option to supply the source for each complementary PWM signal pair from any of the following:
    - Crossbar module outputs
    - External ADC input, taking into account values set in ADC high and low limit registers

1.6.2 12-bit Analog-to-Digital Converter (Cyclic type)

- Two independent 12-bit analog-to-digital converters (ADCs):
    - 2 x 8-channel external inputs
    - Built-in x1, x2, x4 programmable gain pre-amplifier
    - Maximum ADC clock frequency up to 10 MHz, having period as low as 100-ns
    - Single conversion time of 10 ADC clock cycles
    - Additional conversion time of 8 ADC clock cycles
- Support of analog inputs for single-ended and differential, including unipolar differential, conversions
- Sequential, parallel, and independent scan mode
- First 8 samples have offset, limit and zero-crossing calculation supported
- ADC conversions can be synchronized by *any* module connected to the internal crossbar module, such as PWM, timer, GPIO, and comparator modules.
- Support for simultaneous triggering and software-triggering conversions
- Support for a multi-triggering mode with a programmable number of conversions on each trigger
- Each ADC has ability to scan and store up to 8 conversion results.
- Current injection protection

- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

1.6.7 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters
- Up to 100 MHz operation clock

1.6.8 Queued Serial Communications Interface (QSCI) modules

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 16-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection
- Up to 6.25 Mbit/s baud rate at 100 MHz operation clock

1.6.9 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 12.5 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers

- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.10 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter with option to clock up to 100 MHz

1.6.11 Modular/Scalable Controller Area Network (MSCAN) Module

- Clock source from PLL or oscillator.
- Implementation of the CAN protocol Version 2.0 A/B
- Standard and extended data frames
- 0-to-8 bytes data length
- Programmable bit rate up to 1 Mbit/s
- Support for remote frames
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Low power modes, with programmable wakeup on bus activity

1.6.12 Windowed Computer Operating Properly (COP) watchdog

- Programmable windowed timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
    - External crystal oscillator/external clock source

  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC
- Support for interrupt triggered when the counter reaches the timeout value

1.6.13 External Watchdog Monitor (EWM)

- Monitors external circuit as well as the software flow
- Programmable timeout period
- Interrupt capability prior to timeout
- Independent output (EWM_OUT_b) that places external circuit (but not CPU and peripheral) in a safe mode when EWM timeout occurs
- Selectable reference clock source in support of EN60730 and IEC61508
- Wait mode and Stop mode operation is not supported.
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC

1.6.14 Power supervisor

- Power-on reset (POR) to reset CPU, peripherals, and JTAG/EOnCE controllers (V_{DD} > 2.1 V)
- Brownout reset (V_{DD} < 1.9 V)
- Critical warn low-voltage interrupt (LVI2.0)
- Peripheral low-voltage interrupt (LVI2.7)

1.6.15 Phase-locked loop

- Wide programmable output frequency: 200 MHz to 400 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

2 MC56F827xx signal and pin descriptions

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, must be programmed through the GPIO module peripheral enable registers (GPIOx_PER) and the SIM module GPIO peripheral select (GPSx) registers. All GPIO ports can be individually programmed as an input or output (using bit manipulation).

- PWMA_FAULT0, PWMA_FAULT1, and similar signals are inputs used to disable selected PWMA outputs, in cases where the fault conditions originate off-chip.

For the MC56F827xx products, which use 64-pin LQFP, 48-pin LQFP and 32-pin packages:

Table 2. Signal descriptions

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
V_{DD}	29	—	—	Supply	Supply	I/O Power — Supplies 3.3 V power to the chip I/O interface.
	44	32	—			
	60	44	28			
V_{SS}	30	22	14	Supply	Supply	I/O Ground — Provide ground for the device I/O interface.
	43	31	—			
	61	45	29			
V_{DDA}	22	15	9	Supply	Supply	Analog Power — Supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	23	16	10	Supply	Supply	Analog Ground — Supplies an analog ground to the analog modules. It must be connected to a clean power supply.
V_{CAP}	26	19	—	On-chip regulator output	On-chip regulator output	Connect a 2.2 µF bypass capacitor between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation. **NOTE:** The total bypass capacitor value between all V_{CAP} pin and V_{SS} should **not** exceed 4.7 µF.
	57	43	27			
TDI	64	48	32	Input	Input, internal pullup enabled	Test Data Input — It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TDI.
(GPIOD0)				Input/Output		GPIO Port D0
TDO	62	46	30	Output	Output	Test Data Output — It is driven in the shift-IR and shift-DR controller states, and it changes on the falling edge of TCK. After reset, the default state is TDO

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
(XTAL)				Input		The external crystal oscillator output (XTAL) connects the internal crystal oscillator output to an external crystal or ceramic resonator.
GPIOC2	5	5	3	Input/Output	Input	GPIO Port C2: After reset, the default state is GPIOC2.
(TXD0)				Output		SCI0 transmit data output or transmit/ receive in single wire operation
(XB_OUT11)				Output		Crossbar module output 11
(XB_IN2)				Input		Crossbar module input 2
(CLKO0)				Output		Buffered clock output 0: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
GPIOC3	7	6	4	Input/Output	Input	GPIO Port C3: After reset, the default state is GPIOC3.
(TA0)				Input/Output		Quad timer module A channel 0 input/ output
(CMPA_O)				Output		Analog comparator A output
(RXD0)				Input		SCI0 receive data input
(CLKIN1)				Input		External clock input 1
GPIOC4	8	7	5	Input/Output	Input	GPIO Port C4: After reset, the default state is GPIOC4.
(TA1)				Input/Output		Quad timer module A channel 1 input/ output
(CMPB_O)				Output		Analog comparator B output
(XB_IN6)				Input		Crossbar module input 6
(EWM_OUT_B)				Output		External Watchdog Module output
GPIOC5	18	13	—	Input/Output	Input	GPIO Port C5: After reset, the default state is GPIOC5.
(DACA_O)				Analog Output		12-bit digital-to-analog output
(XB_IN7)				Input		Crossbar module input 7
GPIOC6	31	23	15	Input/Output	Input	GPIO Port C6: After reset, the default state is GPIOC6.
(TA2)				Input/Output		Quad timer module A channel 2 input/ output
(XB_IN3)				Input		Crossbar module input 3
(CMP_REF)				Analog Input		Positive input 3 of analog comparator A and B and C.
($\overline{SS0\_B}$)				Input/Output		In slave mode, $\overline{SS0\_B}$ indicates to the SPI module 0 that the current transfer is to be received.

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
(PWMA_1A)				Input/Output		PWM module A (NanoEdge), submodule 1, output A or input capture A
GPIOE4	51	39	25	Input/Output	Input	GPIO Port E4: After reset, the default state is GPIOE4.
(PWMA_2B)				Input/Output		PWM module A (NanoEdge), submodule 2, output B or input capture B
(XB_IN2)				Input		Crossbar module input 2
GPIOE5	52	40	26	Input/Output	Input	GPIO Port E5: After reset, the default state is GPIOE5.
(PWMA_2A)				Input/Output		PWM module A (NanoEdge), submodule 2, output A or input capture A
(XB_IN3)				Input		Crossbar module input 3
GPIOE6	53	—	—	Input/Output	Input	GPIO Port E6: After reset, the default state is GPIOE6.
(PWMA_3B)				Input/Output		PWM module A (NanoEdge), submodule 3, output B or input capture B
(XB_IN4)				Input		Crossbar module input 4
GPIOE7	54	—	—	Input/Output	Input	GPIO Port E7: After reset, the default state is GPIOE7.
(PWMA_3A)				Input/Output		PWM module A (NanoEdge), submodule 3, output A or input capture A
(XB_IN5)				Input		Crossbar module input 5
GPIOF0	36	28	—	Input/Output	Input	GPIO Port F0: After reset, the default state is GPIOF0.
(XB_IN6)				Input		Crossbar module input 6
(SCLK1)				Input/Output		SPI1 serial clock — In master mode, SCLK1 pin is an output, clocking slaved listeners. In slave mode, SCLK1 pin is the data clock input 0.
GPIOF1	50	38	—	Input/Output	Input	GPIO Port F1: After reset, the default state is GPIOF1.
(CLKO1)				Output		Buffered clock output 1: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
(XB_IN7)				Input		Crossbar module input 7
(CMPD_O)				Output		Analog comparator D output
GPIOF2	39	—	19	Input/Output	Input	GPIO Port F2: After reset, the default state is GPIOF2.
(SCL0)				Input/Open-drain Output		I^2C0 serial clock
(XB_OUT6)				Output		Crossbar module output 6
(MISO1)				Input/Output		Master in/slave out for SPI1 —In master mode, MISO1 pin is the data input. In slave mode, MISO1 pin is the data

Table continues on the next page...

3.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **nxp.com** and perform a part number search for the following device numbers: MC56F82

4 Part identification

4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

4.2 Format

Part numbers for this device have the following format: Q 56F8 2 C F P T PP N

4.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• MC = Fully qualified, general market flow • PC = Prequalification
56F8	DSC family with flash memory and DSP56800/ DSP56800E/DSP56800EX core	• 56F8
2	DSC subfamily	• 2
C	Maximum CPU frequency (MHz)	• 7 = 100 MHz
F	Primary program flash memory size	• 1 = 16 KB • 2 = 32 KB • 3 = 48 KB • 4 = 64 KB
P	Pin count	• 3 = 32 • 6 = 48 • 8 = 64
T	Temperature range (°C)	• V = –40 to 105 • M = –40 to 125
PP	Package identifier	• LC = 32LQFP • FM = 32QFN

Table continues on the next page...

6.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing is in conformity with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if after exposure to ESD pulses, the device no longer meets the device specification. Complete DC parametric and functional testing is performed as per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 4. ESD/Latch-up Protection

Characteristic[1]	Min	Max	Unit
ESD for Human Body Model (HBM)	–2000	+2000	V
ESD for Machine Model (MM)	–200	+200	V
ESD for Charge Device Model (CDM)	–500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	–100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

6.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 5 may affect device reliability or cause permanent damage to the device.

NOTE

If the voltage difference between VDD and VDDA or VSS and VSSA is too large, then the device can malfunction or be permanently damaged. The restrictions are:

- **At all times, it is recommended that the voltage difference of VDD - VSS be within +/-200 mV of the voltage difference of VDDA - VSSA**, including power ramp up and ramp down; see additional requirements in Table 6. Failure to do this recommendation may result in a

3. All 5 volt tolerant digital I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than VDIO_MIN (= V_{SS}–0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

7 General

7.1 General characteristics

The device is fabricated in high-density, low-power CMOS with 5 V–tolerant TTL-compatible digital inputs, except for the $\overline{\text{RESET}}$ pin which is 3.3V only. The term "5 V–tolerant" refers to the capability of an I/O pin, built on a 3.3 V–compatible process technology, to withstand a voltage up to 5.5 V without damaging the device.

5 V–tolerant I/O is desirable because many systems have a mixture of devices designed for 3.3 V and 5 V power supplies. In such systems, a bus may carry both 3.3 V– and 5 V–compatible I/O voltage levels (a standard 3.3 V I/O is designed to receive a maximum voltage of 3.3 V ± 10% during normal operation without causing damage). This 5 V–tolerant capability therefore offers the power savings of 3.3 V I/O levels combined with the ability to receive 5 V levels without damage.

Absolute maximum ratings in Table 5 are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply to the temperature range specified in Table 5 over the following supply ranges: V_{SS}=V_{SSA}=0V, V_{DD}=V_{DDA}=3.0V to 3.6V, CL≤50 pF, f_{OP}=50MHz.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 6. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V) (continued)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
ADC (Cyclic) Reference Voltage High	V_{REFHA} V_{REFHB}		V_{DDA}-0.6		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔVDD		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔVSS		-0.1	0	0.1	V
Input Voltage High (digital inputs)	V_{IH}	Pin Group 1	0.7 x V_{DD}		5.5	V
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	Pin Group 2	0.7 x V_{DD}	—	V_{DD}	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2			0.35 x V_{DD}	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High (at V_{OH} min.) • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	Pin Group 1 Pin Group 1	— —		-2 -9	mA
Output Source Current Low (at V_{OL} max.)[2, 3] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	Pin Groups 1, 2 Pin Groups 1, 2	— —		2 9	mA

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Total IO sink current and total IO source current are limited to 75 mA each
3. Contiguous pin DC injection current of regional limit—including sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25 mA.

7.3.2 LVD and POR operating requirements

Table 7. PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
POR Assert Voltage[1]	POR		2.0		V
POR Release Voltage[2]	POR		2.7		V
LVI_2p7 Threshold Voltage			2.73		V
LVI_2p2 Threshold Voltage			2.23		V

1. During 3.3-volt V_{DD} power supply ramp down
2. During 3.3-volt V_{DD} power supply ramp up (gated by LVI_2p7)

Table 11. Current Consumption (mA) (continued)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C		Maximum at 3.6V, 125°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
		• Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • Repeat NOP instructions • All peripheral modules, except COP and EWM, disabled and clocks gated off • Simple loop running from platform instruction buffer						
VLPWAIT	200 kHz	• 32 kHz Device Clock • Clocked by a 64 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in wait mode	0.7	—	7.5	—	10.0	—
VLPSTOP	200 kHz	• 32 kHz Device Clock • Clocked by a 64 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby. • Small regulator is disabled. • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in stop mode	0.7	—	7.5	—	10.0	—

1. No output switching, all ports configured as inputs, all inputs low, no DC loads.
2. In all chip LP modes and flash memory VLP modes, the maximum frequency for flash memory operation is 500 kHz due to the fixed frequency ratio of 1:2 between the CPU clock and the flash clock when running with 2 MHz external clock input and CPU running at 1 MHz.

7.3.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for “EMC design.”

Board type	Symbol	Description	32 QFN	32 LQFP	48 LQFP	64 LQFP	Unit	Notes
		(200 ft./min. air speed)						
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	27	49	39	39	°C/W	1,2
—	$R_{\theta JB}$	Thermal resistance, junction to board	12	31	23	28	°C/W	
—	$R_{\theta JC}$	Thermal resistance, junction to case	1.8	22	17	15	°C/W	
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	6	5	3	3	°C/W	

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions —Forced Convection (Moving Air)* with the board horizontal.

8 Peripheral operating requirements and behaviors

8.1 Core modules

8.1.1 JTAG timing

Table 16. JTAG timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation	f_{OP}	DC	SYS_CLK/ 8	MHz	Figure 6
TCK clock pulse width	t_{PW}	50	—	ns	Figure 6
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 7

Table continues on the next page...

8.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

8.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

8.4.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	1
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	70	575	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

8.4.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA

Table continues on the next page...

8.5.2 12-bit Digital-to-Analog Converter (DAC) parameters

Table 28. DAC parameters

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
DC Specifications						
Resolution			12	12	12	bits
Settling time[1]	At output load RLD = 3 kΩ CLD = 400 pF		—	1		µs
Power-up time	Time from release of PWRDWN signal until DACOUT signal is valid	t_{DAPU}	—	—	11	µs
Accuracy						
Integral non-linearity[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	INL	—	+/- 3	+/- 4	LSB[3]
Differential non-linearity[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	DNL	—	+/- 0.8	+/- 0.9	LSB[3]
Monotonicity	> 6 sigma monotonicity, < 3.4 ppm non-monotonicity		guaranteed			—
Offset error[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	V_{OFFSET}	—	+/- 25	+ /- 43	mV
Gain error[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	E_{GAIN}	—	+/- 0.5	+/- 1.5	%
DAC Output						
Output voltage range	Within 40 mV of either V_{SSA} or V_{DDA}	V_{OUT}	V_{SSA} + 0.04 V	—	V_{DDA} - 0.04 V	V
AC Specifications						
Signal-to-noise ratio		SNR	—	85	—	dB
Spurious free dynamic range		SFDR	—	-72	—	dB
Effective number of bits		ENOB	—	11	—	bits

1. Settling time is swing range from V_{SSA} to V_{DDA}
2. No guaranteed specification within 5% of V_{DDA} or V_{SSA}
3. LSB = 0.806 mV

Table 32. SPI timing (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Clock (SCK) high time Master Slave	t_{CH}		— —	ns ns	Figure 14 Figure 15 Figure 16 Figure 17
Clock (SCK) low time Master Slave	t_{CL}	28 28	— —	ns ns	Figure 17
Data set-up time required for inputs Master Slave	t_{DS}	20 1	— —	ns ns	Figure 14 Figure 15 Figure 16 Figure 17
Data hold time required for inputs Master Slave	t_{DH}	1 3	— —	ns ns	Figure 14 Figure 15 Figure 16 Figure 17
Access time (time to data active from high-impedance state) Slave	t_A	5	—	ns	Figure 17
Disable time (hold time to high-impedance state) Slave	t_D	5	—	ns	Figure 17
Data valid for outputs Master Slave (after enable edge)	t_{DV}	— —		ns ns	Figure 14 Figure 15 Figure 16 Figure 17
Data invalid Master Slave	t_{DI}	0 0	— —	ns ns	Figure 14 Figure 15 Figure 16 Figure 17
Rise time Master Slave	t_R	— —	1 1	ns ns	Figure 14 Figure 15 Figure 16 Figure 17
Fall time Master Slave	t_F	— —	1 1	ns ns	Figure 14 Figure 15 Figure 16 Figure 17

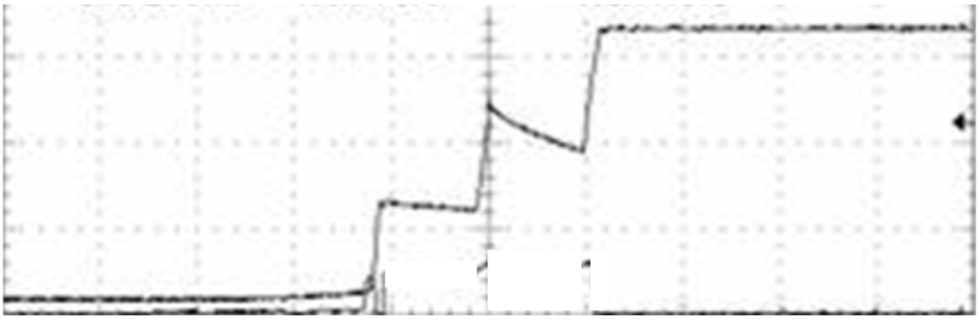

Figure 23. Supply Voltage Drop

A recommended initialization sequence during power-up is:

1. After POR is released, run a few hundred NOP instructions from the internal relaxation oscillator; this gives time for the supply voltage to stabilize.
2. Configure the peripherals (except the ADC) to the desired settings; the ADC should stay in low power mode.
3. Power up the PLL.
4. After the PLL locks, switch the clock from PLL prescale to postscale.
5. Configure the ADC.

10 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **nxp.com** and perform a keyword search for the drawing's document number:

Drawing for package	Document number to be used
32LQFP	98ASH70029A
32QFN	98ASA00473D
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W

11 Pinout

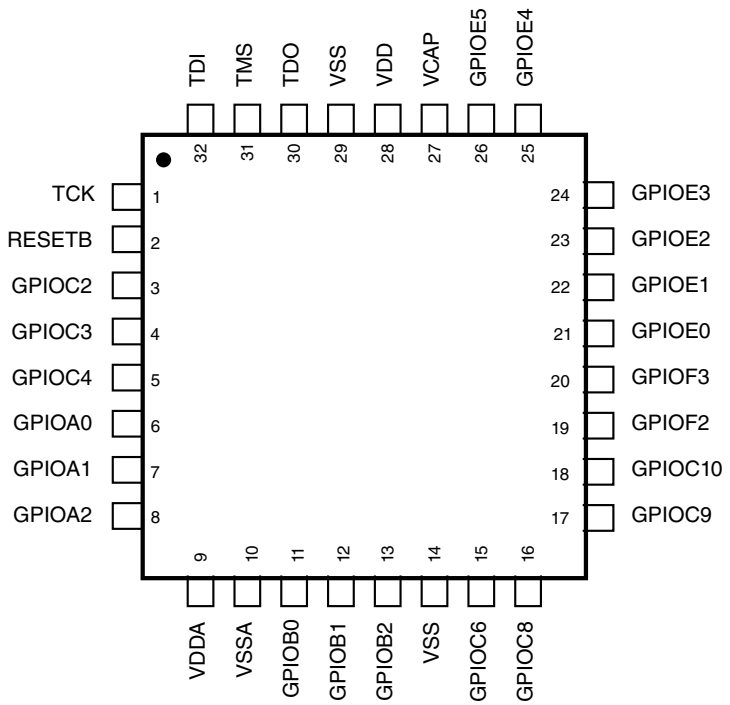

Figure 26. 32-pin LQFP and QFN

NOTE

The RESETB pin is a 3.3 V pin only.

12 Product documentation

The documents listed in Table 36 are required for a complete description and to successfully design using the device. Documentation is available from local NXP distributors, NXP sales offices, or online at **www.nxp.com**.

Table 36. Device documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F827xx Reference Manual	Detailed functional description and programming model	MC56F827XXRM
MC56F827xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F827XXDS
MC56F82xxx Errata	Details any chip issues that might be present	MC56F82xxx_Errata

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