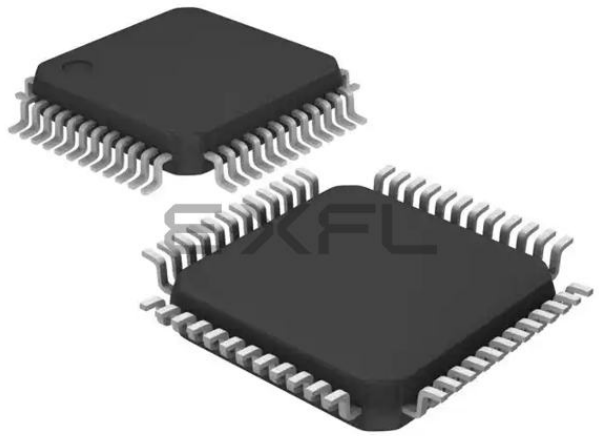

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	39
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f82746mlf

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, which effectively supports DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers correspond to nine address registers (R0, R1, R2, R3, R4, R5, N, N3, M01)
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions enable compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack, with the stack's depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation Parameters

- Up to 50 MHz operation in normal mode and 100 MHz operation in fast mode
- Operation ambient temperature:
  V Temperature option:-40 ºC to 105ºC
  M Temperature option:-40 ºC to 125ºC
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 On-Chip Memory and Memory Protection

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-port RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses by the core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory

- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.10 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter with option to clock up to 100 MHz

1.6.11 Modular/Scalable Controller Area Network (MSCAN) Module

- Clock source from PLL or oscillator.
- Implementation of the CAN protocol Version 2.0 A/B
- Standard and extended data frames
- 0-to-8 bytes data length
- Programmable bit rate up to 1 Mbit/s
- Support for remote frames
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Low power modes, with programmable wakeup on bus activity

1.6.12 Windowed Computer Operating Properly (COP) watchdog

- Programmable windowed timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
    - External crystal oscillator/external clock source

1.6.16 Clock sources

1.6.16.1 On-chip oscillators

- Tunable 8 MHz relaxation oscillator with 400 kHz at standby mode (divide-by-two output)
- 200 kHz low frequency clock as secondary clock source for COP, EWM, PIT

1.6.16.2 Crystal oscillator

- Support for both high ESR crystal oscillator (ESR greater than 100 Ω) and ceramic resonator
- Operating frequency: 4–16 MHz

1.6.17 Cyclic Redundancy Check (CRC) Generator

- Hardware CRC generator circuit with 16-bit shift register
- High-speed hardware CRC calculation
- Programmable initial seed value
- CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial
- Error detection for all single, double, odd, and most multibit errors
- Option to transpose input data or output data (CRC result) bitwise, which is required for certain CRC standards

1.6.18 General Purpose I/O (GPIO)

- 5 V tolerance (except RESETB pin)
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins (except JTAG and RESETB) default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

1.7 Block diagrams

The 56800EX core is based on a modified dual Harvard-style architecture, consisting of three execution units operating in parallel, and allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
(ANA2&VREFHA &CMPA_IN1)				Input		ANA2 is analog input to channel 2 of ADCA; VREFHA is analog reference high of ADCA; CMPA_IN1 is negative input 1 of analog comparator A. When used as an analog input, the signal goes to both ANA2, VREFHA, and CMPA_IN1.
GPIOA3	16	12	—	Input/Output	Input	GPIO Port A3: After reset, the default state is GPIOA3.
(ANA3&VREFLA& CMPA_IN2)				Input		ANA3 is analog input to channel 3 of ADCA; VREFLA is analog reference low of ADCA; CMPA_IN2 is negative input 2 of analog comparator A.
GPIOA4	12	8	—	Input/Output	Input	GPIO Port A4: After reset, the default state is GPIOA4.
(ANA4&CMPD_IN 0)				Input		ANA4 is Analog input to channel 4 of ADCA; CMPD_IN0 is input 0 to comparator D.
GPIOA5	11	—	—	Input/Output	Input	GPIO Port A5: After reset, the default state is GPIOA5.
(ANA5&CMPD_IN 1)				Input		ANA5 is analog input to channel 5 of ADCA; ANC9 is analog input to channel 9 of ADCC; CMPD_IN1 is negative input 1 of analog comparator D.
GPIOA6	10	—	—	Input/Output	Input	GPIO Port A6: After reset, the default state is GPIOA6.
(ANA6&CMPD_IN 2)				Input		ANA6 is analog input to channel 5 of ADCA; CMPD_IN2 is negative input 2 of analog comparator D.
GPIOA7	9	—	—	Input/Output	Input	GPIO Port A7: After reset, the default state is GPIOA7.
(ANA7&CMPD_IN 3)				Input		ANA7 is analog input to channel 7 of ADCA; CMPD_IN3 is negative input 3 of analog comparator D.
GPIOB0	24	17	11	Input/Output	Input	GPIO Port B0: After reset, the default state is GPIOB0.
(ANB0&CMPB_IN 3)				Input		ANB0 is analog input to channel 0 of ADCB; CMPB_IN3 is positive input 3 of analog comparator B. When used as an analog input, the signal goes to ANB0 and CMPB_IN3. The ADC control register configures this input as ANB0.
GPIOB1	25	18	12	Input/Output	Input	GPIO Port B1: After reset, the default state is GPIOB1.
(ANB1&CMPB_IN 0)				Input		ANB1 is analog input to channel 1 of ADCB; CMPB_IN0 is negative input 0 of analog comparator B. When used as an analog input, the signal goes to ANB1

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
						output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
GPIOF3	40	—	20	Input/Output	Input	GPIO Port F3: After reset, the default state is GPIOF3.
(SDA0)				Input/Open-drain Output		I^2C0 serial data line
(XB_OUT7)				Output		Crossbar module output 7
(MOSI1)				Input/Output		Master out/slave in for SPI1— In master mode, MOSI1 pin is the data output. In slave mode, MOSI1 pin is the data input.
GPIOF4	41	—	—	Input/Output	Input	GPIO Port F4: After reset, the default state is GPIOF4.
(TXD1)				Output		SCI1 transmit data output or transmit/ receive in single wire operation
(XB_OUT8)				Output		Crossbar module output 8
(PWMA_0X)				Input/Output		PWM module A (NanoEdge), submodule 0, output X or input capture X
(PWMA_FAULT6)				Input		Disable PWMA output 6
GPIOF5	42	—	—	Input/Output	Input	GPIO Port F5: After reset, the default state is GPIOF5.
(RXD1)				Input		SCI1 receive data input
(XB_OUT9)				Output		Crossbar module output 9
(PWMA_1X)				Input/Output		PWM module A (NanoEdge), submodule 1, output X or input capture X
(PWMA_FAULT7)				Input		Disable PWMA output 7
GPIOF6	58	—	—	Input/Output	Input	GPIO Port F6: After reset, the default state is GPIOF6.
(PWMA_3X)				Input/Output		PWM module A (NanoEdge), submodule 3, output X or input capture X
(XB_IN2)				Input		Crossbar module input 2
GPIOF7	59	—	—	Input/Output	Input	GPIO Port F7: After reset, the default state is GPIOF7.
(CMPC_O)				Output		Analog comparator C output
(SS1_B)				Input/Output		In slave mode, SS1_B indicates to the SPI1 module that the current transfer is to be received.
(XB_IN3)				Input		Crossbar module input 3
GPIOF8	6	—	—	Input/Output	Input	GPIO Port F8: After reset, the default state is GPIOF8.
(RXD0)				Input		SCI0 receive data input
(XB_OUT10)				Output		Crossbar module output 10
(CMPD_O)				Output		Analog comparator D output

Table continues on the next page...

Field	Description	Values
		• LF = 48LQFP • LH = 64LQFP
N	Packaging type	• R = Tape and reel • (Blank) = Trays

4.4 Example

This is an example part number: MC56F82748VLH

5 Terminology and guidelines

5.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

5.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

5.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

5.2.1 Example

This is an example of an operating behavior:

harmful leakage current through the substrate, between the VDD/VSS and VDDA/VSSA pad cells. This harmful leakage current could prevent the device from operating after power up.

- **At all times, to avoid permanent damage to the part, the voltage difference between VDD and VDDA must absolutely be limited to 0.3 V**; see Table 5.
- **At all times, to avoid permanent damage to the part, the voltage difference between VSS and VSSA must absolutely be limited to 0.3 V**; see Table 5.

Table 5. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Supply Voltage Range	V_{DD}		-0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		-0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		-0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Input Voltage Range	V_{IN_RESET}	Pin Group 2	-0.3	4.0	V
Oscillator Input Voltage Range	V_{OSC}	Pin Group 4	-0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	-0.3	4.0	V
Input clamp current, per pin (V_{IN} < V_{SS} - 0.3 V)[2, 3]	V_{IC}		—	-5.0	mA
Output clamp current, per pin[4]	V_{OC}		—	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{ICont}		-25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1, 2	-0.3	4.0	V
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Output Voltage Range	V_{OUTOD_RESET}	Pin Group 2	-0.3	4.0	V
DAC Output Voltage Range	V_{OUT_DAC}	Pin Group 5	-0.3	4.0	V
Ambient Temperature	T_A	V temperature	-40	105	°C
		M temperature	-40	125	
Junction Temperature	T_j	V temperature	-40	115	°C
		M temperature	-40	135	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		-55	150	°C

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Continuous clamp current

Table 6. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V) (continued)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
ADC (Cyclic) Reference Voltage High	V_{REFHA} V_{REFHB}		V_{DDA}-0.6		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔVDD		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔVSS		-0.1	0	0.1	V
Input Voltage High (digital inputs)	V_{IH}	Pin Group 1	0.7 x V_{DD}		5.5	V
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	Pin Group 2	0.7 x V_{DD}	—	V_{DD}	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2			0.35 x V_{DD}	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High (at V_{OH} min.) • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	Pin Group 1 Pin Group 1	— —		-2 -9	mA
Output Source Current Low (at V_{OL} max.)[2, 3] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	Pin Groups 1, 2 Pin Groups 1, 2	— —		2 9	mA

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Total IO sink current and total IO source current are limited to 75 mA each
3. Contiguous pin DC injection current of regional limit—including sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25 mA.

7.3.2 LVD and POR operating requirements

Table 7. PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
POR Assert Voltage[1]	POR		2.0		V
POR Release Voltage[2]	POR		2.7		V
LVI_2p7 Threshold Voltage			2.73		V
LVI_2p2 Threshold Voltage			2.23		V

1. During 3.3-volt V_{DD} power supply ramp down
2. During 3.3-volt V_{DD} power supply ramp up (gated by LVI_2p7)

8.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

8.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

8.4.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	1
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	70	575	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

8.4.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA

Table continues on the next page...

Table 27. 12-bit ADC Electrical Specifications (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ADC RUN Current (per ADC block)	I_{ADRUN}		1.8		mA
ADC Powerdown Current (adc_pdn enabled)	$I_{ADPWRDWN}$		0.1		µA
V_{REFH} Current (in external mode)	I_{VREFH}		190	225	µA
Accuracy (DC or Absolute)					
Integral non-Linearity[6]	INL		+/- 1.5	+/- 2.2	LSB[7]
Differential non-Linearity[6]	DNL		+/- 0.5	+/- 0.8	LSB[7]
Monotonicity			GUARANTEED		
Offset[8] Fully Differential Single Ended/Unipolar	V_{OFFSET}		+/- 8 +/- 12		mV
Gain Error	E_{GAIN}		0.996 to1.004	0.990 to 1.010	
AC Specifications[9]					
Signal to Noise Ratio	SNR		66		dB
Total Harmonic Distortion	THD		75		dB
Spurious Free Dynamic Range	SFDR		77		dB
Signal to Noise plus Distortion	SINAD		66		dB
Effective Number of Bits Gain = 1x (Fully Differential/Unipolar) Gain = 2x (Fully Differential/Unipolar) Gain = 4x (Fully Differential/Unipolar) Gain = 1x (Single Ended) Gain = 2x (Single Ended) Gain = 4x (Single Ended) Variation across channels[10]	ENOB		— 10.6 — 10.3 10.6 10.4 10.2 0.1		bits
ADC Inputs					
Input Leakage Current	I_{IN}		1		nA
Temperature sensor slope	T_{SLOPE}		1.7		mV/°C
Temperature sensor voltage at 25 °C	V_{TEMP25}		0.82		V
Disturbance					
Input Injection Current [11]	I_{INJ}			+/-3	mA
Channel to Channel Crosstalk[12]	ISOXTLK		-82		dB
Memory Crosstalk[13]	MEMXTLK		-71		dB
Input Capacitance Sampling Capacitor	C_{ADI}		4.8		pF

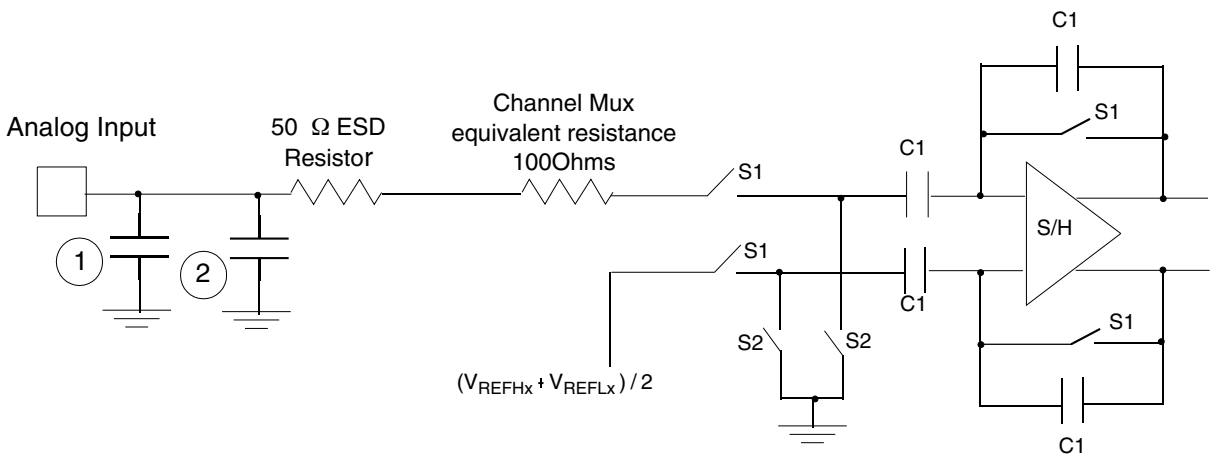
1. The ADC functions up to VDDA = 2.7 V. When VDDA is below 3.0 V, ADC specifications are not guaranteed
2. ADC clock duty cycle is 45% ~ 55%
3. Conversion range is defined for x1 gain setting. For x2 and x4 the range is 1/2 and 1/4, respectively.
4. In unipolar mode, positive input must be ensured to be always greater than negative input.
5. First conversion takes 10 clock cycles.
6. INL/DNL is measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$ using Histogram method at x1 gain setting

7. Least Significant Bit = 0.806 mV at 3.3 V V_{DDA}, x1 gain Setting
8. Offset measured at 2048 code
9. Measured converting a 1 kHz input full scale sine wave
10. When code runs from internal RAM
11. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC
12. Any off-channel with 50 kHz full-scale input to the channel being sampled with DC input (isolation crosstalk)
13. From a previously sampled channel with 50 kHz full-scale input to the channel being sampled with DC input (memory crosstalk).

8.5.1.1 Equivalent circuit for ADC inputs

The following figure shows the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases, and both S1 and S2 are dependent on the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times 4.8 \times 10^{-12}} + 100\ ohm + 50\ ohm$$



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling = 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing = 2.04pF
3. S1 and S2 switch phases are non-overlapping and depend on the ADC clock frequency

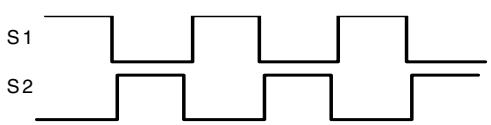


Figure 10. Equivalent circuit for A/D loading

8.5.2 12-bit Digital-to-Analog Converter (DAC) parameters

Table 28. DAC parameters

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
DC Specifications						
Resolution			12	12	12	bits
Settling time[1]	At output load RLD = 3 kΩ CLD = 400 pF		—	1		µs
Power-up time	Time from release of PWRDWN signal until DACOUT signal is valid	t_{DAPU}	—	—	11	µs
Accuracy						
Integral non-linearity[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	INL	—	+/- 3	+/- 4	LSB[3]
Differential non-linearity[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	DNL	—	+/- 0.8	+/- 0.9	LSB[3]
Monotonicity	> 6 sigma monotonicity, < 3.4 ppm non-monotonicity		guaranteed			—
Offset error[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	V_{OFFSET}	—	+/- 25	+ /- 43	mV
Gain error[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	E_{GAIN}	—	+/- 0.5	+/- 1.5	%
DAC Output						
Output voltage range	Within 40 mV of either V_{SSA} or V_{DDA}	V_{OUT}	V_{SSA} + 0.04 V	—	V_{DDA} - 0.04 V	V
AC Specifications						
Signal-to-noise ratio		SNR	—	85	—	dB
Spurious free dynamic range		SFDR	—	-72	—	dB
Effective number of bits		ENOB	—	11	—	bits

1. Settling time is swing range from V_{SSA} to V_{DDA}
2. No guaranteed specification within 5% of V_{DDA} or V_{SSA}
3. LSB = 0.806 mV

Table 31. Timer timing

Characteristic	Symbol	Min[1]	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	Figure 13
Timer input high/low period	P_{INHL}	1T + 3	—	ns	Figure 13
Timer output period	P_{OUT}	2T-2	—	ns	Figure 13
Timer output high/low period	P_{OUTHL}	1T-2	—	ns	Figure 13

1. T = clock cycle. For 100 MHz operation, T = 10 ns.

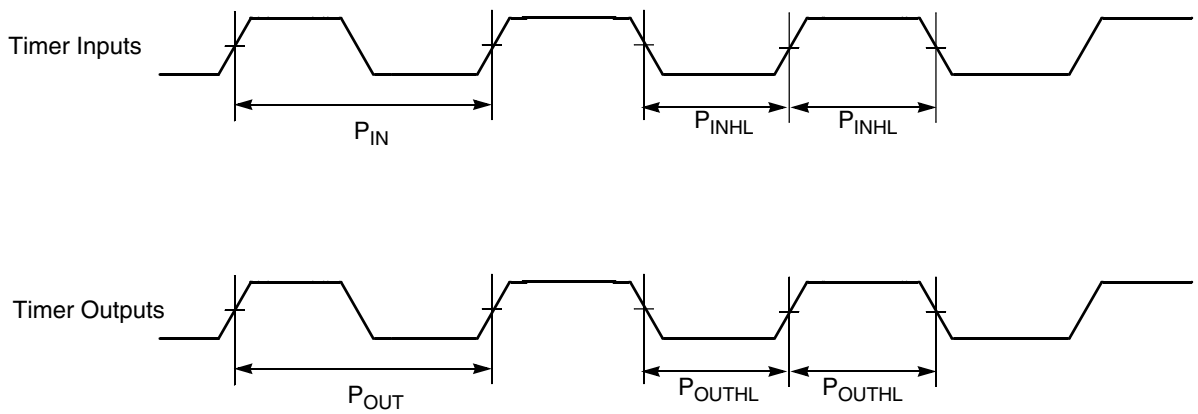


Figure 13. Timer timing

8.7 Communication interfaces

8.7.1 Queued Serial Peripheral Interface (SPI) timing

Parameters listed are guaranteed by design.

Table 32. SPI timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	60 60	— —	ns ns	Figure 14 Figure 15 Figure 16 Figure 17
Enable lead time Master Slave	t_{ELD}	— 20	— —	ns ns	Figure 17
Enable lag time Master Slave	t_{ELG}	— 20	— —	ns ns	Figure 17

Table continues on the next page...

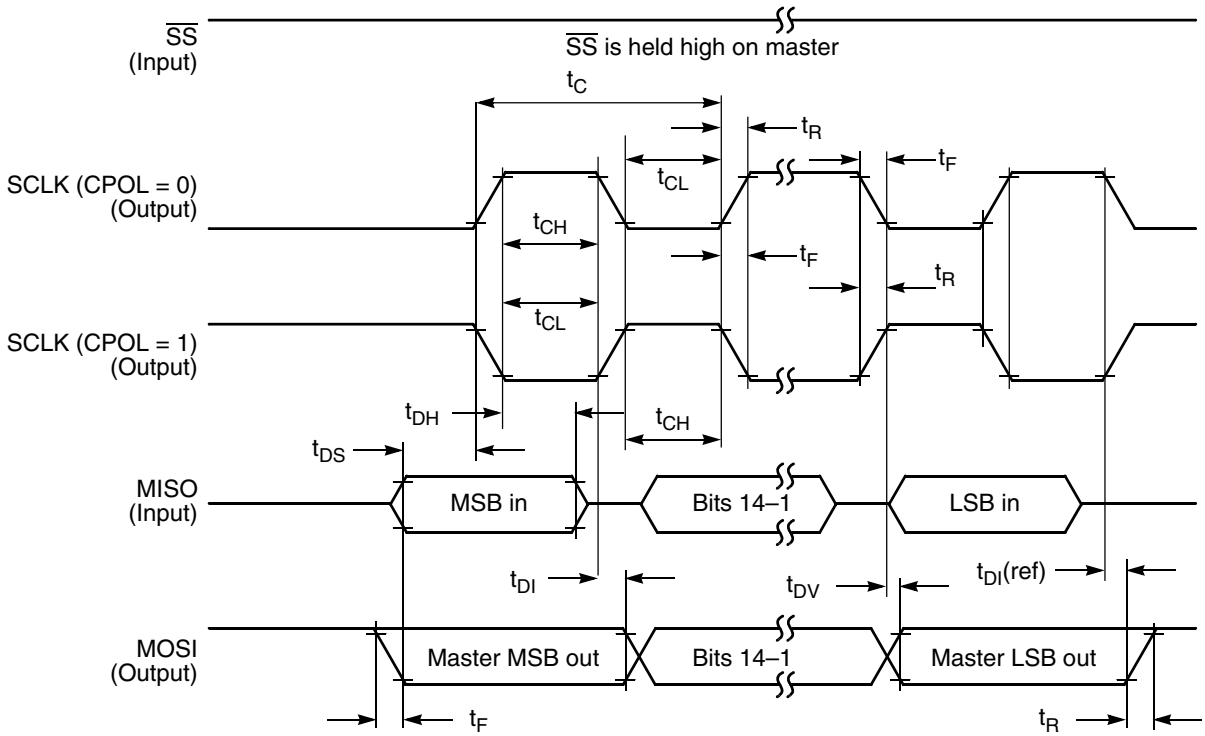


Figure 14. SPI master timing (CPHA = 0)

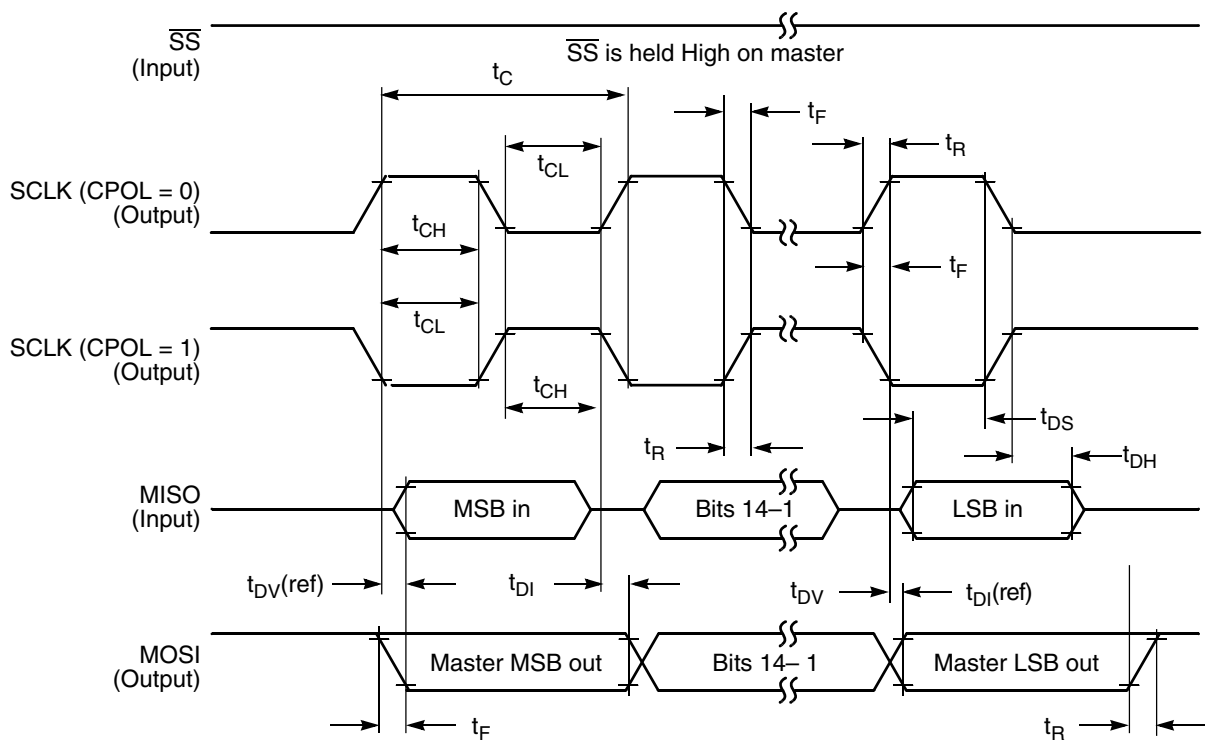


Figure 15. SPI master timing (CPHA = 1)

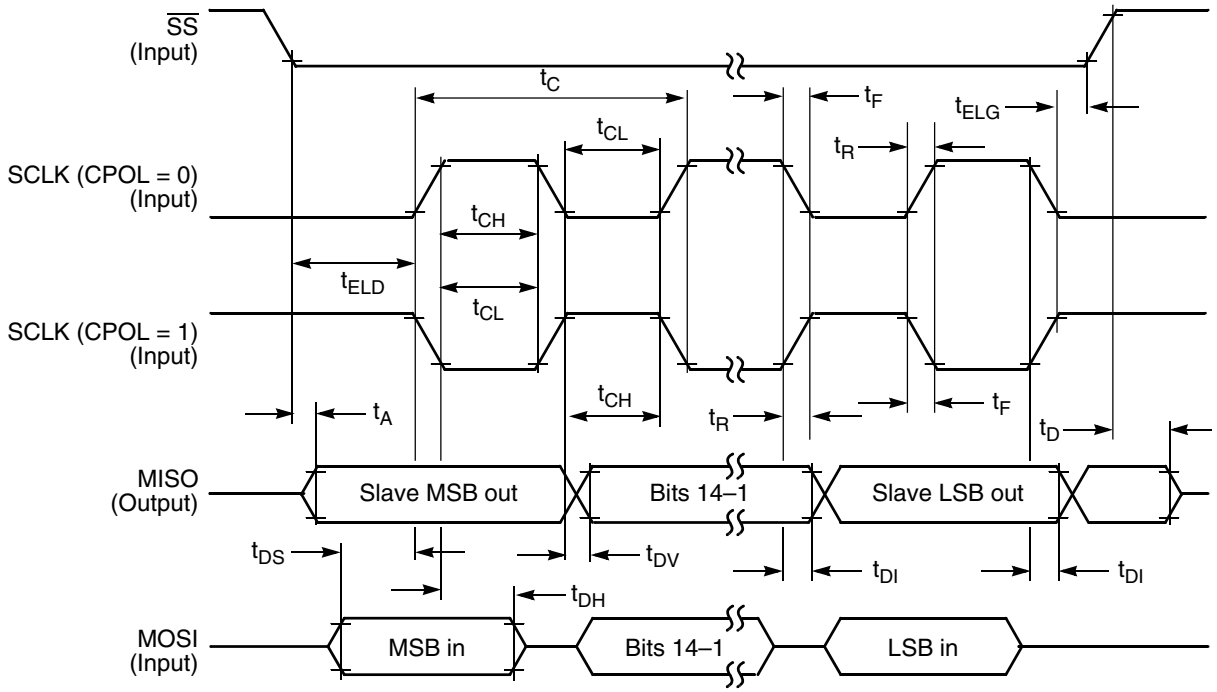


Figure 16. SPI slave timing (CPHA = 0)

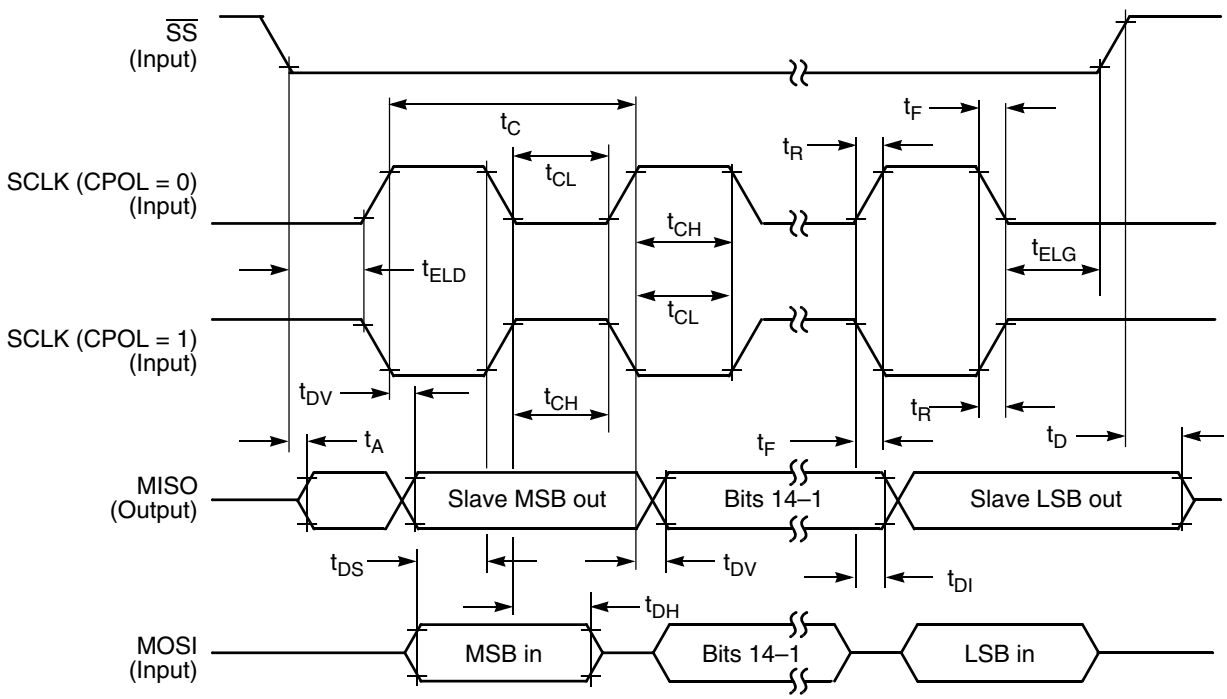


Figure 17. SPI slave timing (CPHA = 1)

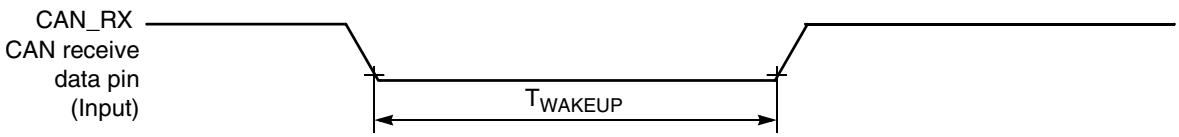


Figure 20. Bus Wake-up Detection

NOTE

CAN wakeup is not supported when ROSC_8M is in standby mode.

8.7.4 Inter-Integrated Circuit Interface (I^2C) timing

Table 35. I^2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF.
4. Set-up time in slave-transmitter mode is 1 IP Bus clock period, if the TX FIFO is empty.
5. A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{SU;\,DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\,DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

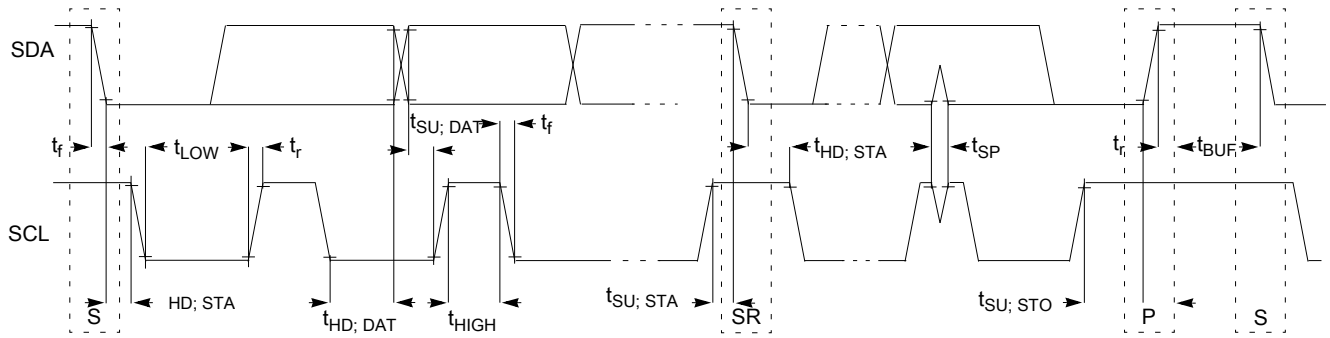


Figure 21. Timing definition for fast and standard mode devices on the I^2C bus

9 Design Considerations

9.1 Thermal design considerations

An estimate of the chip junction temperature (TJ) can be obtained from the equation:

$$T_J = T_A + (R_{\Theta JA} \times P_D)$$

Where,

T_A = Ambient temperature for the package (°C)

$R_{\Theta JA}$ = Junction-to-ambient thermal resistance (°C/W)

P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which TJ value is closer to the application depends on the power dissipated by other components on the board.

- The TJ value obtained on a single layer board is appropriate for a tightly packed printed circuit board.
- The TJ value obtained on a board with the internal planes is usually appropriate if the board has low-power dissipation and if the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$$

Where,

- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at tri-state.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10Ω RC filter.

9.3 Power-on Reset design considerations

9.3.1 Improper power-up sequence between VDD/VSS and VDDA/VSSA:

It is recommended that VDD be kept within 100 mV of VDDA at all times, including power ramp-up and ramp-down. Failure to keep VDDA within 100 mV of VDDA may cause a leakage current through the substrate, between the VDD and VDDA pad cells. This leakage current could prevent operation of the device after it powers up. The voltage difference between VDD and VDDA must be limited to below 0.3 V at all times, to avoid permanent damage to the part (See Table 5). Also see Table 6.

9.3.2 Unnecessary protection circuit:

In many circuit designs, it is a general practice to add external clamping diodes on each analog input pin; see diode D1 and D2 in Figure 22, to prevent the surge voltage from damaging the analog input.

11.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The SIM's GPS registers are responsible for selecting which ALT functionality is available on most pins.

NOTE

- The RESETB pin is a 3.3 V pin only.
- If the GPIOC1 pin is used as GPIO, the XOSC should be powered down.
- Not all CMPD pins are available on 48 LQFP, 32 LQFP, and 32 QFN packages.
- QSPI signals—including MISO1, MOSI1, SCLK1, and SS0_B—are not available on the 48 LQFP, 32 LQFP, and 32 QFN packages.

64 LQFP	48 LQFP	32 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
1	1	1	TCK	TCK	GPIOD2			
2	2	2	RESETB	RESETB	GPIOD4			
3	3	—	GPIOC0	GPIOC0	EXTAL	CLKIN0		
4	4	—	GPIOC1	GPIOC1	XTAL			
5	5	3	GPIOC2	GPIOC2	TXD0	XB_OUT11	XB_IN2	CLKO0
6	—	—	GPIOF8	GPIOF8	RXD0	XB_OUT10	CMPD_O	PWM_2X
7	6	4	GPIOC3	GPIOC3	TA0	CMPA_O	RXD0	CLKIN1
8	7	5	GPIOC4	GPIOC4	TA1	CMPB_O	XB_IN6	EWM_OUT_B
9	—	—	GPIOA7	GPIOA7	ANA7&CMPD_IN3			
10	—	—	GPIOA6	GPIOA6	ANA6&CMPD_IN2			
11	—	—	GPIOA5	GPIOA5	ANA5&CMPD_IN1			
12	8	—	GPIOA4	GPIOA4	ANA4&CMPD_IN0			
13	9	6	GPIOA0	GPIOA0	ANA0&CMPA_IN3	CMPC_O		
14	10	7	GPIOA1	GPIOA1	ANA1&CMPA_IN0			
15	11	8	GPIOA2	GPIOA2	ANA2&VREFHA&CMPA_IN1			
16	12	—	GPIOA3	GPIOA3	ANA3&VREFLA&CMPA_IN2			
17	—	—	GPIOB7	GPIOB7	ANB7&CMPB_IN2			
18	13	—	GPIOC5	GPIOC5	DACA_O	XB_IN7		
19	—	—	GPIOB6	GPIOB6	ANB6&CMPB_IN1			
20	—	—	GPIOB5	GPIOB5	ANB5&CMPC_IN2			
21	14	—	GPIOB4	GPIOB4	ANB4&CMPC_IN1			
22	15	9	VDDA	VDDA				
23	16	10	VSSA	VSSA				
24	17	11	GPIOB0	GPIOB0	ANB0&CMPB_IN3			

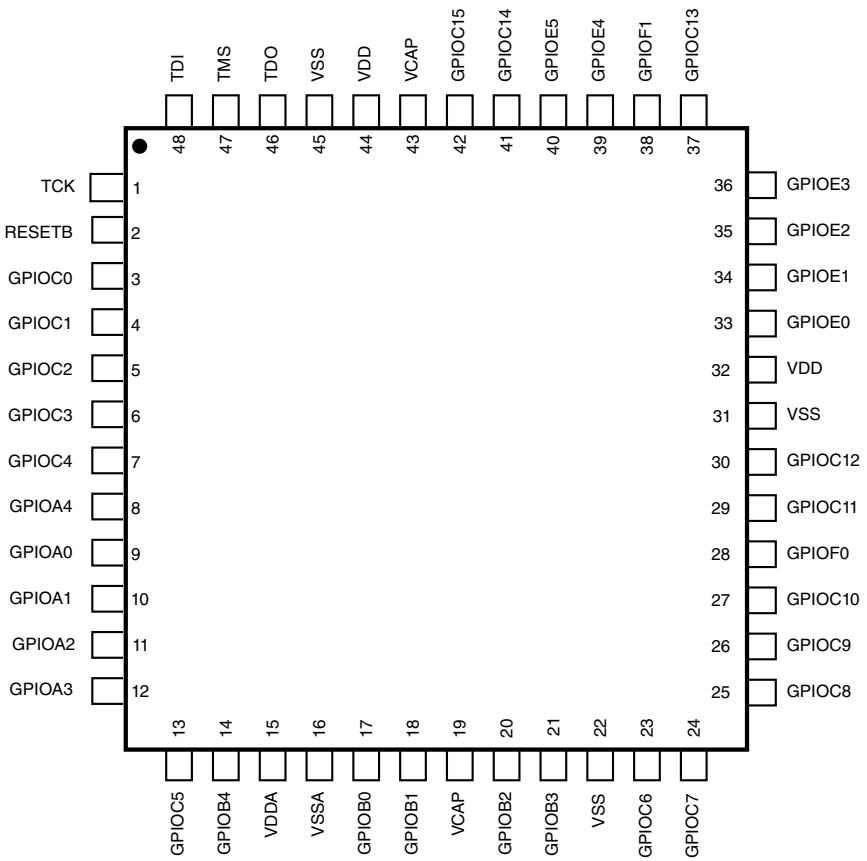


Figure 25. 48-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.