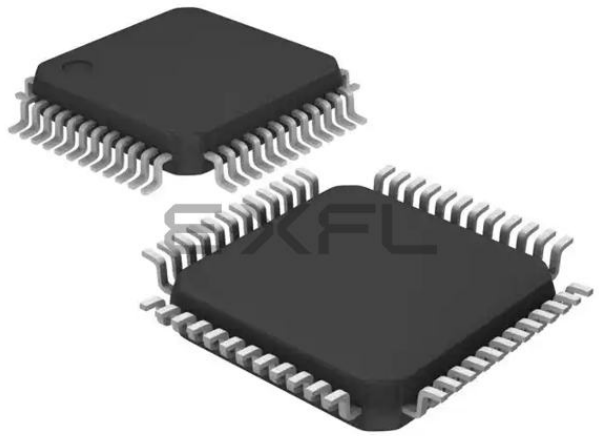

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	39
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f82746vlfr

1 Overview

1.1 MC56F827xx Product Family

The following table is the comparsion of features among members of the family.

Table 1. MC56F827xx Family

Feature	MC56F82											
Part Number[1]	748V LH	746V LF 746M LF	743V LC	743V FM	738V LH	736V LF	733V LC	733V FM 733M FM	728V LH	726V LF	723V LC	723V FM
Core frequency (MHz)	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50
Flash memory (KB)	64	64	64	64	48	48	48	48	32	32	32	32
RAM (KB)	8	8	8	8	8	8	8	8	6	6	6	6
Interrupt Controller	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Windowed Computer Operating Properly (WCOP)	1	1	1	1	1	1	1	1	1	1	1	1
External Watchdog Monitor (EWM)	1	1	1	1	1	1	1	1	1	1	1	1
Periodic Interrupt Timer (PIT)	2	2	2	2	2	2	2	2	2	2	2	2
Cyclic Redundancy Check (CRC)	1	1	1	1	1	1	1	1	1	1	1	1
Quad Timer (TMR)	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4
12-bit Cyclic ADC channels	2x8	2x5	2x3	2x3	2x8	2x5	2x3	2x3	2x8	2x5	2x3	2x3
PWM Module:												
Input capture channels[2]	12	6	6	6	12	6	6	6	12	6	6	6
High-resolution channels	8	6	6	6	8	6	6	6	8	6	6	6
Standard channels	4	0	0	0	4	0	0	0	4	0	0	0
12-bit DAC	2	2	2	2	2	2	2	2	2	2	2	2
DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table continues on the next page...

Table 1. MC56F827xx Family (continued)

Feature	MC56F82											
Part Number[1]	748V LH	746V LF 746M LF	743V LC	743V FM	738V LH	736V LF	733V LC	733V FM 733M FM	728V LH	726V LF	723V LC	723V FM
Analog Comparators (CMP)	4	4	3	3	4	4	3	3	4	4	3	3
QSCI	2	2	1	1	2	2	1	1	2	2	1	1
QSPI	2	1	1	1	2	1	1	1	2	1	1	1
I2C/SMBus	1	1	1	1	1	1	1	1	1	1	1	1
MSCAN	1	1	0	0	1	1	0	0	1	1	0	0
GPIO	54	39	26	26	54	39	26	26	54	39	26	26
Package pin count	64 LQFP	48 LQFP	32 LQFP	32 QFN	64 LQFP	48 LQFP	32 LQFP	32 QFN	64 LQFP	48 LQFP	32 LQFP	32 QFN
AEC-Q100[3]	Yes	Yes	No	No	Yes	Yes	No	No	Yes	Yes	No	No

1. Temperature options
   V: -40°C to 105°C
   M: -40°C to 125°C
2. Input capture shares the pin with cooresponding PWM channels.
3. Qualification aligned to AEC-Q100

1.2 56800EX 32-bit Digital Signal Controller (DSC) core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture:
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Supports concurrent instruction fetches in the same cycle, and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 100 million instructions per second (MIPS) at 100 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses support 8-bit, 16-bit, and 32-bit data movement, plus addition, subtraction, and logical operations
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, which effectively supports DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers correspond to nine address registers (R0, R1, R2, R3, R4, R5, N, N3, M01)
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions enable compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack, with the stack's depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation Parameters

- Up to 50 MHz operation in normal mode and 100 MHz operation in fast mode
- Operation ambient temperature:
  V Temperature option:-40 ºC to 105ºC
  M Temperature option:-40 ºC to 125ºC
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 On-Chip Memory and Memory Protection

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-port RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses by the core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory

- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

1.6.7 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters
- Up to 100 MHz operation clock

1.6.8 Queued Serial Communications Interface (QSCI) modules

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 16-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection
- Up to 6.25 Mbit/s baud rate at 100 MHz operation clock

1.6.9 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 12.5 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers

- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.10 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter with option to clock up to 100 MHz

1.6.11 Modular/Scalable Controller Area Network (MSCAN) Module

- Clock source from PLL or oscillator.
- Implementation of the CAN protocol Version 2.0 A/B
- Standard and extended data frames
- 0-to-8 bytes data length
- Programmable bit rate up to 1 Mbit/s
- Support for remote frames
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Low power modes, with programmable wakeup on bus activity

1.6.12 Windowed Computer Operating Properly (COP) watchdog

- Programmable windowed timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
    - External crystal oscillator/external clock source

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
(SCL0)				Input/Open-drain Output		I²C0 serial clock
(TXD1)				Output		SCI1 transmit data output or transmit/ receive in single wire operation
GPIOC12	38	30	—	Input/Output	Input	GPIO Port C12: After reset, the default state is GPIOC12.
(CANRX)				Input		CAN receive data input
(SDA0)				Input/Open-drain Output		I²C0 serial data line
(RXD1)				Input		SCI1 receive data input
GPIOC13	49	37	—	Input/Output	Input	GPIO Port C13: After reset, the default state is GPIOC13.
(TA3)				Input/Output		Quad timer module A channel 3 input/ output
(XB_IN6)				Input		Crossbar module input 6
(EWM_OUT_B)				Output		External Watchdog Module output
GPIOC14	55	41	—	Input/Output	Input	GPIO Port C14: After reset, the default state is GPIOC14.
(SDA0)				Input/ Opendrain Output		I²C0 serial data line
(XB_OUT4)				Output		Crossbar module output 4
(PWM_FAULT4)				Input		Disable PWMA output 4
GPIOC15	56	42	—	Input/Output	Input	GPIO Port C15: After reset, the default state is GPIOC15.
(SCL0)				Input/Open-drain Output		I²C0 serial clock
(XB_OUT5)				Output		Crossbar module output 5
(PWM_FAULT5)				Input		Disable PWMA output 5
GPIOE0	45	33	21	Input/Output	Input	GPIO Port E0: After reset, the default state is GPIOE0.
(PWM_0B)				Input/Output		PWM module A (NanoEdge), submodule 0, output B or input capture B
GPIOE1	46	34	22	Input/Output	Input	GPIO Port E1: After reset, the default state is GPIOE1.
(PWM_0A)				Input/Output		PWM module A (NanoEdge), submodule 0, output A or input capture A
GPIOE2	47	35	23	Input/Output	Input	GPIO Port E2: After reset, the default state is GPIOE2.
(PWMA_1B)				Input/Output		PWM module A (NanoEdge), submodule 1, output B or input capture B
GPIOE3	48	36	24	Input/Output	Input	GPIO Port E3: After reset, the default state is GPIOE3.

Table continues on the next page...

Field	Description	Values
		• LF = 48LQFP • LH = 64LQFP
N	Packaging type	• R = Tape and reel • (Blank) = Trays

4.4 Example

This is an example part number: MC56F82748VLH

5 Terminology and guidelines

5.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

5.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

5.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

5.2.1 Example

This is an example of an operating behavior:

Table 6. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V) (continued)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
ADC (Cyclic) Reference Voltage High	V_{REFHA} V_{REFHB}		V_{DDA}-0.6		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔVDD		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔVSS		-0.1	0	0.1	V
Input Voltage High (digital inputs)	V_{IH}	Pin Group 1	0.7 x V_{DD}		5.5	V
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	Pin Group 2	0.7 x V_{DD}	—	V_{DD}	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2			0.35 x V_{DD}	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High (at V_{OH} min.) • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	Pin Group 1 Pin Group 1	— —		-2 -9	mA
Output Source Current Low (at V_{OL} max.)[2, 3] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	Pin Groups 1, 2 Pin Groups 1, 2	— —		2 9	mA

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Total IO sink current and total IO source current are limited to 75 mA each
3. Contiguous pin DC injection current of regional limit—including sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25 mA.

7.3.2 LVD and POR operating requirements

Table 7. PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
POR Assert Voltage[1]	POR		2.0		V
POR Release Voltage[2]	POR		2.7		V
LVI_2p7 Threshold Voltage			2.73		V
LVI_2p2 Threshold Voltage			2.23		V

1. During 3.3-volt V_{DD} power supply ramp down
2. During 3.3-volt V_{DD} power supply ramp up (gated by LVI_2p7)

Table 10. Power mode transition behavior

Symbol	Description	Min	Max	Unit	Notes[1]
T_{POR}	After a POR event, the amount of delay from when V_{DD} reaches 2.7 V to when the first instruction executes (over the operating temperature range).	199	225	µs	
	STOP mode to RUN mode	6.79	7.27.31	µs	2
	LPS mode to LPRUN mode	240.9	551	µs	3
	VLPS mode to VLPRUN mode	1424	1459	µs	4
	WAIT mode to RUN mode	0.570	0.620	µs	5
	LPWAIT mode to LPRUN mode	237.2	554	µs	3
	VLPWAIT mode to VLPRUN mode	1413	1500	µs	4

1. Wakeup times are measured from GPIO toggle for wakeup till GPIO toggle at the wakeup interrupt subroutine from respective stop/wait mode.
2. Clock configuration: CPU clock=4 MHz. System clock source is 8 MHz IRC in normal mode.
3. CPU clock = 200 KHz and 8 MHz IRC on standby. Exit by an interrupt on PORTC GPIO.
4. Using 64 KHz external clock; CPU Clock = 32KHz. Exit by an interrupt on PortC GPIO.
5. Clock configuration: CPU and system clocks= 100 MHz. Bus Clock = 50 MHz. .Exit by interrupt on PORTC GPIO

7.3.5 Power consumption operating behaviors

Table 11. Current Consumption (mA)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C		Maximum at 3.6V, 125°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
RUN1	100 MHz	• 100 MHz Core • 50 MHz Peripheral clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Continuous MAC instructions with fetches from Program Flash • All peripheral modules enabled. TMRs and SCIs using 1X peripheral clock • NanoEdge within eFlexPWM using 2X peripheral clock • ADC/DAC (only one 12-bit DAC and all 6-bit DACs) powered on and clocked • Comparator powered on	38.1	9.9	53.5	13.2	53.5	13.2
RUN2	50 MHz	• 50 MHz Core and Peripheral clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Continuous MAC instructions with fetches from Program Flash • All peripheral modules enabled. TMRs and SCIs using 1X peripheral clock • NanoEdge within eFlexPWM using 2X peripheral clock	27.6	9.9	43.5	13.2	43.5	14.0

Table continues on the next page...

Table 11. Current Consumption (mA) (continued)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C		Maximum at 3.6V, 125°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
		• ADC/DAC (only one 12-bit DAC and all 6-bit DACs) powered on and clocked • Comparator powered on						
WAIT	50 MHz	• 50 MHz Core and Peripheral clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Processor Core in WAIT state • All Peripheral modules enabled. • TMRs and SCIs using 1X Clock • NanoEdge within PWMA using 2X clock • ADC/DAC (single 12-bit DAC, all 6-bit DACs), Comparator powered off	24.0	—	41.3	—	41.3	—
STOP	4 MHz	• 4 MHz Device Clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered off • Processor Core in STOP state • All peripheral module and core clocks are off • ADC/DAC/Comparator powered off	6.3	—	19.4	—	19.4	—
LPRUN (LsRUN)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator's (ROSC) low speed clock • ROSC in standby mode • Regulators are in standby • PLL disabled • Repeat NOP instructions • All peripheral modules enabled, except NanoEdge and cyclic ADCs. One 12-bit DAC and all 6-bit DACs enabled. • Simple loop with running from platform instruction buffer	2.8	3.1	11.1	4.0	13.0	4.0
LPWAIT (LsWAIT)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator's (ROSC) low speed clock • ROSC in standby mode • Regulators are in standby • PLL disabled • All peripheral modules enabled, except NanoEdge and cyclic ADCs. One 12-bit DAC and all 6-bit DACs enabled.[2] • Processor core in wait mode	2.7	3.1	11.1	4.0	13.0	4.0
LPSTOP (LsSTOP)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator's (ROSC) low speed clock • ROSC in standby mode • Regulators are in standby • PLL disabled • Only PITs and COP enabled; other peripheral modules disabled and clocks gated off[2] • Processor core in stop mode	1.2	—	9.1	—	12.0	—
VLPRUN	200 kHz	• 32 kHz Device Clock • Clocked by a 64 kHz external clock source	0.7	—	7.5	—	10.0	—

Table continues on the next page...

7.3.7 Capacitance attributes

Table 12. Capacitance attributes

Description	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	—	10	—	pF
Output capacitance	C_{OUT}	—	10	—	pF

7.4 Switching specifications

7.4.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYSCLK}	Device (system and core) clock frequency • using relaxation oscillator • using external clock source	 0.001 0	 100 100	MHz	
f_{BUS}	Bus clock	—	50	MHz	

7.4.2 General switching timing

Table 14. Switching timing

Symbol	Description	Min	Max	Unit	Notes
	GPIO pin interrupt pulse width[1] Synchronous path	1.5		IP Bus Clock Cycles	
	Port rise and fall time (high drive strength), Slew disabled 2.7 ≤ V_{DD} ≤ 3.6V.	5.5	15.1	ns	
	Port rise and fall time (high drive strength), Slew enabled 2.7 ≤ V_{DD} ≤ 3.6V.	1.5	6.8	ns	2
	Port rise and fall time (low drive strength). Slew disabled . 2.7 ≤ V_{DD} ≤ 3.6V	8.2	17.8	ns	
	Port rise and fall time (low drive strength). Slew enabled . 2.7 ≤ V_{DD} ≤ 3.6V	3.2	9.2	ns	3

1. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIOn_IPOLR and GPIOn_IENR.
2. 75 pF load
3. 15 pF load

7.5 Thermal specifications

7.5.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description		Min	Max	Unit
T_J	Die junction temperature	V	–40	115	°C
		M	–40	135	°C
T_A	Ambient temperature	V	–40	105	°C
		M	–40	125	°C

7.5.2 Thermal attributes

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To account for $P_{I/O}$ in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

See Thermal design considerations for more detail on thermal design considerations.

Board type	Symbol	Description	32 QFN	32 LQFP	48 LQFP	64 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	96	83	70	64	°C/W	,
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	33	55	46	46	°C/W	1,
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient	80	70	57	52	°C/W	1,2

Table continues on the next page...

Table 25. Flash high voltage current behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

8.4.1.4 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

8.5 Analog

8.5.1 12-bit Cyclic Analog-to-Digital Converter (ADC) Parameters

Table 27. 12-bit ADC Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Conditions					
Supply Voltage[1]	VDDA	3	3.3	3.6	V
VREFH (in external reference mode)	Vrefhx	VDDA-0.6		VDDA	V
ADC Conversion Clock[2]	f_{ADCCLK}	0.1		10	MHz
Conversion Range[3] Fully Differential Single Ended/Unipolar	R_{AD}	 $-(V_{REFH} - V_{REFL})$ V_{REFL}		 $V_{REFH} - V_{REFL}$ V_{REFH}	V
Input Voltage Range (per input)[4] External Reference Internal Reference	V_{ADIN}	 V_{REFL} 0		 V_{REFH} V_{DDA}	V
Timing and Power					
Conversion Time[5]	t_{ADC}		8		ADC Clock Cycles
ADC Power-Up Time (from adc_pdn)	t_{ADPU}		13		ADC Clock Cycles

Table continues on the next page...

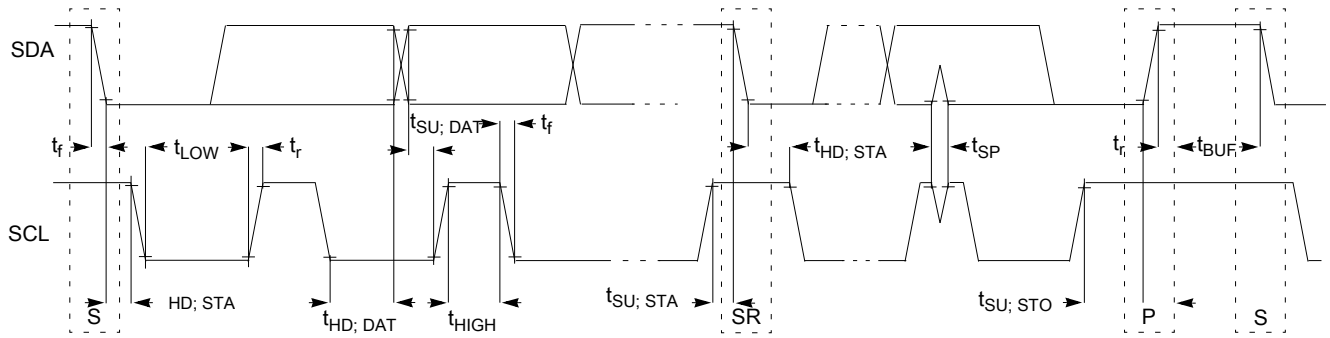

Figure 21. Timing definition for fast and standard mode devices on the I^2C bus

9 Design Considerations

9.1 Thermal design considerations

An estimate of the chip junction temperature (TJ) can be obtained from the equation:

$$T_J = T_A + (R_{\Theta JA} \times P_D)$$

Where,

T_A = Ambient temperature for the package (°C)

$R_{\Theta JA}$ = Junction-to-ambient thermal resistance (°C/W)

P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which TJ value is closer to the application depends on the power dissipated by other components on the board.

- The TJ value obtained on a single layer board is appropriate for a tightly packed printed circuit board.
- The TJ value obtained on a board with the internal planes is usually appropriate if the board has low-power dissipation and if the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$$

Where,

$R_{\Theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\Theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (YJT) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

Where,

T_T = Thermocouple temperature on top of package (°C/W)

Ψ_{JT} = hermal characterization parameter (°C/W)

P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

To determine the junction temperature of the device in the application when heat sinks are used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at tri-state.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10Ω RC filter.

9.3 Power-on Reset design considerations

9.3.1 Improper power-up sequence between VDD/VSS and VDDA/VSSA:

It is recommended that VDD be kept within 100 mV of VDDA at all times, including power ramp-up and ramp-down. Failure to keep VDDA within 100 mV of VDDA may cause a leakage current through the substrate, between the VDD and VDDA pad cells. This leakage current could prevent operation of the device after it powers up. The voltage difference between VDD and VDDA must be limited to below 0.3 V at all times, to avoid permanent damage to the part (See Table 5). Also see Table 6.

9.3.2 Unnecessary protection circuit:

In many circuit designs, it is a general practice to add external clamping diodes on each analog input pin; see diode D1 and D2 in Figure 22, to prevent the surge voltage from damaging the analog input.

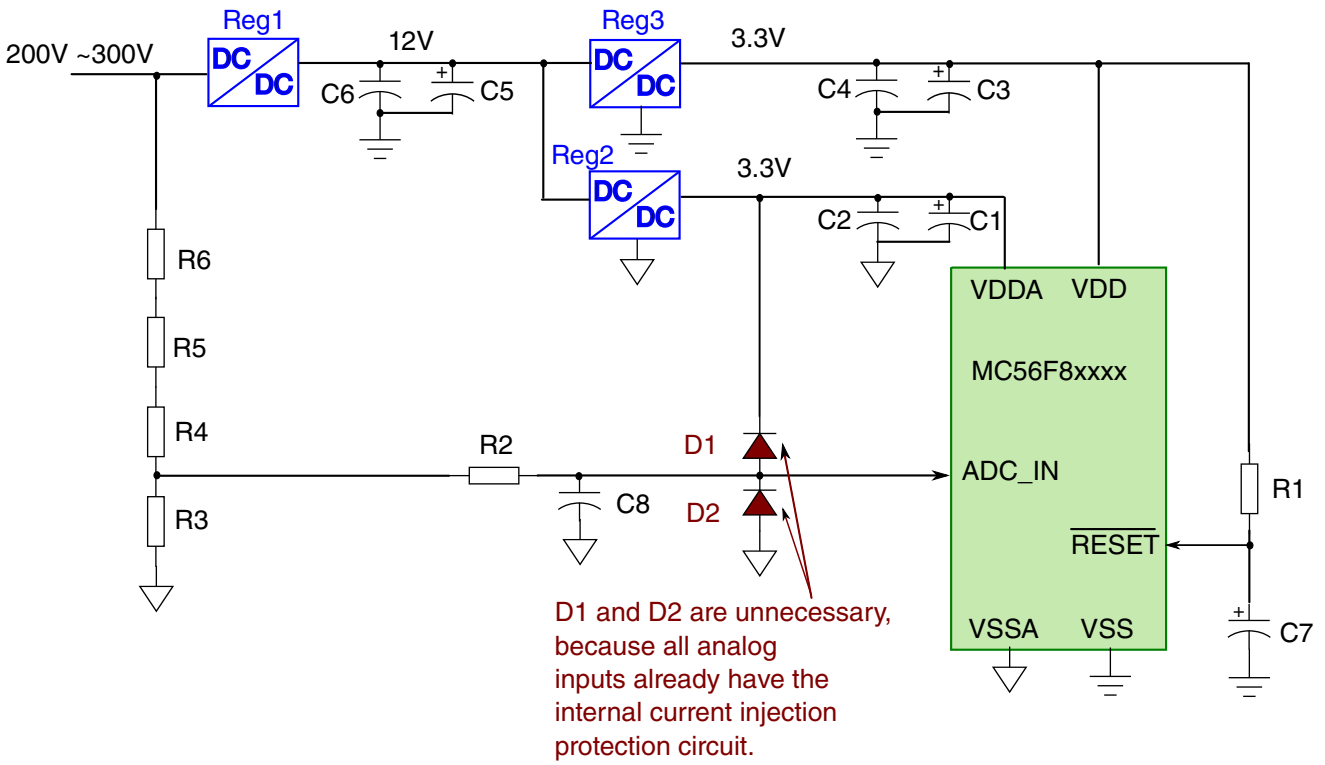

Figure 22. Protection Circuit Example

MC56F8xxxx DSC uses the 5V tolerance I/O. When the pin is configured to digital input, it can accept 5V input. See Table 5. When the pin is configured to analog input, the internal integrated current injection protection circuit is enabled. The current injection protection circuit performs the same functions as external clamp diode D1 and D2 in Figure 22. As long as the source or sink current for each analog pin is less than 3 mA, then there is no damage to the device. See Table 27. Therefore, D1 and D2 clamping diodes are **not** recommended to be used.

9.3.3 Heavy capacitive load on power supply output:

In some applications, the low cost DC/DC converter may not regulate the output voltage well before it reaches the regulation point, which is roughly around 2.5V to 2.7V. However, the MC56F8xxxx DSC will exit power-on reset at around 2.3V. If the initialization code enables the PLL to run the DSC at full speed right after reset, then the high current will be pulled by DSC from the supply, which can cause the supply voltage to drop below the operation voltage; see the captured graph (Figure 23). This can cause the DSC fail to start up.

64 LQFP	48 LQFP	32 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
25	18	12	GPIOB1	GPIOB1	ANB1&CMPB_IN0	DACB_O		
26	19	—	VCAP	VCAP				
27	20	13	GPIOB2	GPIOB2	ANB2&VERFHB&CMPC_IN3			
28	21	—	GPIOB3	GPIOB3	ANB3&VREFLB&CMPC_IN0			
29	—	—	VDD	VDD				
30	22	14	VSS	VSS				
31	23	15	GPIOC6	GPIOC6	TA2	XB_IN3	CMP_REF	SS0_B
32	24	—	GPIOC7	GPIOC7	SS0_B	TXD0	XB_IN8	
33	25	16	GPIOC8	GPIOC8	MISO0	RXD0	XB_IN9	XB_OUT6
34	26	17	GPIOC9	GPIOC9	SCLK0	XB_IN4	TXD0	XB_OUT8
35	27	18	GPIOC10	GPIOC10	MOSI0	XB_IN5	MISO0	XB_OUT9
36	28	—	GPIOF0	GPIOF0	XB_IN6		SCLK1	
37	29	—	GPIOC11	GPIOC11	CANTX	SCL0	TXD1	
38	30	—	GPIOC12	GPIOC12	CANRX	SDA0	RXD1	
39	—	19	GPIOF2	GPIOF2	SCL0	XB_OUT6	MISO1	
40	—	20	GPIOF3	GPIOF3	SDA0	XB_OUT7	MOSI1	
41	—	—	GPIOF4	GPIOF4	TXD1	XB_OUT8	PWM_0X	PWM_FAULT6
42	—	—	GPIOF5	GPIOF5	RXD1	XB_OUT9	PWM_1X	PWM_FAULT7
43	31	—	VSS	VSS				
44	32	—	VDD	VDD				
45	33	21	GPIOE0	GPIOE0	PWM_0B			
46	34	22	GPIOE1	GPIOE1	PWM_0A			
47	35	23	GPIOE2	GPIOE2	PWM_1B			
48	36	24	GPIOE3	GPIOE3	PWM_1A			
49	37	—	GPIOC13	GPIOC13	TA3	XB_IN6	EWM_OUT_B	
50	38	—	GPIOF1	GPIOF1	CLKO1	XB_IN7	CMPD_O	
51	39	25	GPIOE4	GPIOE4	PWM_2B	XB_IN2		
52	40	26	GPIOE5	GPIOE5	PWM_2A	XB_IN3		
53	—	—	GPIOE6	GPIOE6	PWM_3B	XB_IN4		
54	—	—	GPIOE7	GPIOE7	PWM_3A	XB_IN5		
55	41	—	GPIOC14	GPIOC14	SDA0	XB_OUT4	PWM_FAULT4	
56	42	—	GPIOC15	GPIOC15	SCL0	XB_OUT5	PWM_FAULT5	
57	43	27	VCAP	VCAP				
58	—	—	GPIOF6	GPIOF6		PWM_3X		XB_IN2
59	—	—	GPIOF7	GPIOF7		CMPC_O	SS1_B	XB_IN3
60	44	28	VDD	VDD				
61	45	29	VSS	VSS				
62	46	30	TDO	TDO	GPIOD1			
63	47	31	TMS	TMS	GPIOD3			
64	48	32	TDI	TDI	GPIOD0			

11.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

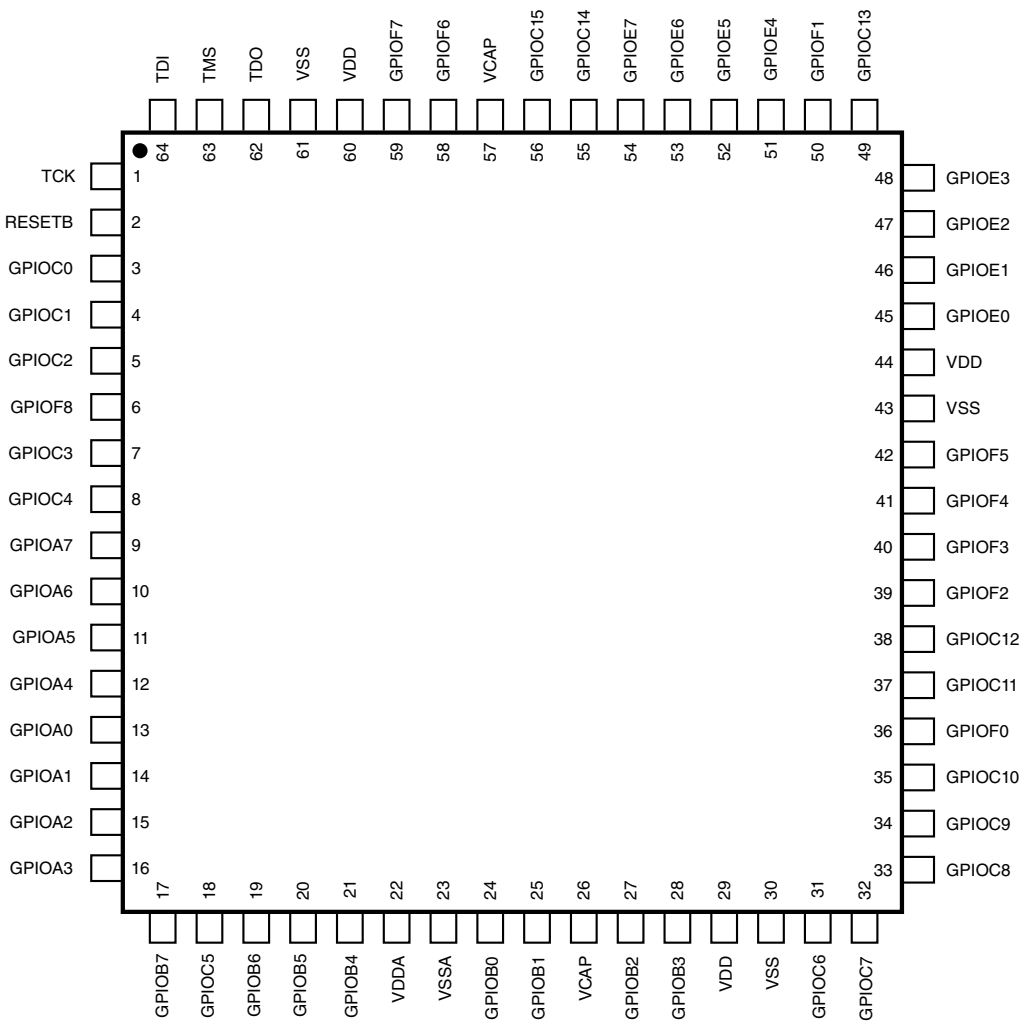

Figure 24. 64-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.

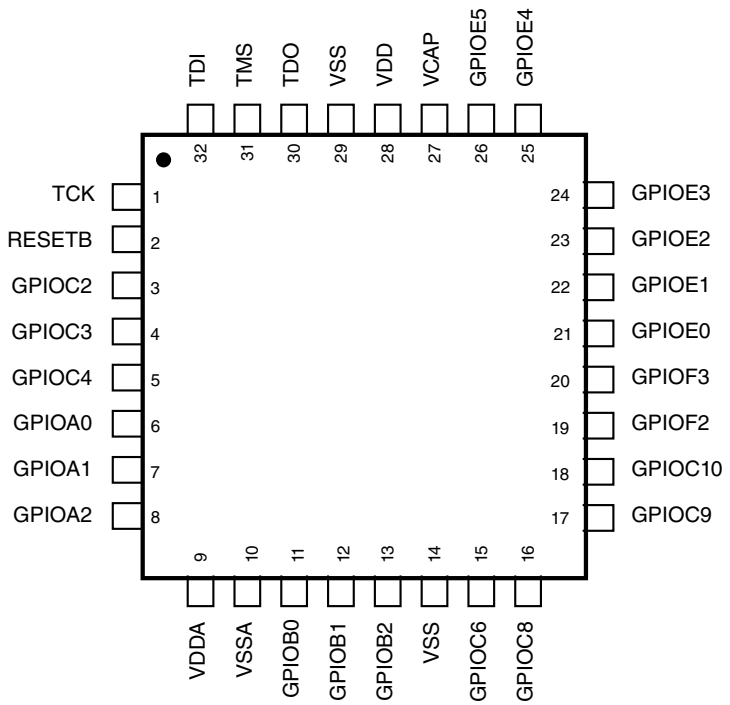

Figure 26. 32-pin LQFP and QFN

NOTE

The RESETB pin is a 3.3 V pin only.

12 Product documentation

The documents listed in Table 36 are required for a complete description and to successfully design using the device. Documentation is available from local NXP distributors, NXP sales offices, or online at **www.nxp.com**.

Table 36. Device documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F827xx Reference Manual	Detailed functional description and programming model	MC56F827XXRM
MC56F827xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F827XXDS
MC56F82xxx Errata	Details any chip issues that might be present	MC56F82xxx_Errata