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Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I ² C), LINbus, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 25x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f544-iq

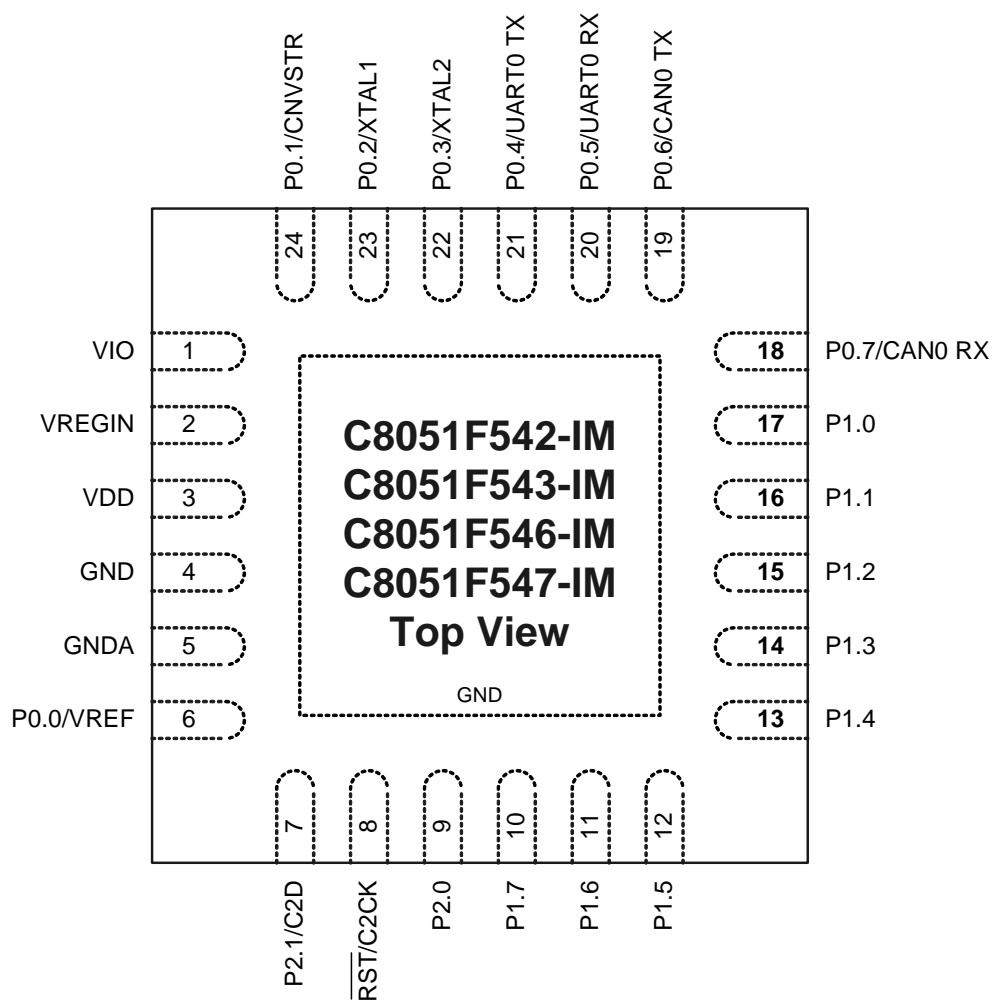


Figure 3.3. QFN-24 Pinout Diagram (Top View)

5.3.2. Setting the Gain Value

The three programmable gain registers are accessed indirectly using the ADC0H and ADC0L registers when the GAINEN bit (ADC0CF.0) bit is set. ADC0H acts as the address register, and ADC0L is the data register. The programmable gain registers can only be written to and cannot be read. See Gain Register Definition 5.1, Gain Register Definition 5.2, and Gain Register Definition 5.3 for more information.

The gain is programmed using the following steps:

1. Set the GAINEN bit (ADC0CF.0)
2. Load the ADC0H with the ADC0GNH, ADC0GNL, or ADC0GNA address.
3. Load ADC0L with the desired value for the selected gain register.
4. Reset the GAINEN bit (ADC0CF.0)

Notes:

1. An ADC conversion should not be performed while the GAINEN bit is set.
2. Even with gain enabled, the maximum input voltage must be less than V_{REGIN} and the maximum voltage of the signal after gain must be less than or equal to V_{REF} .

In code, changing the value to 0.44 gain from the previous example looks like:

```
// in 'C':
ADC0CF |= 0x01;           // GAINEN = 1
ADC0H = 0x04;             // Load the ADC0GNH address
ADC0L = 0x6C;             // Load the upper byte of 0x6CA to ADC0GNH
ADC0H = 0x07;             // Load the ADC0GNL address
ADC0L = 0xA0;             // Load the lower nibble of 0x6CA to ADC0GNL
ADC0H = 0x08;             // Load the ADC0GNA address
ADC0L = 0x01;             // Set the GAINADD bit
ADC0CF &= ~0x01;         // GAINEN = 0

; in assembly
ORL ADC0CF,#01H           ; GAINEN = 1
MOV ADC0H,#04H            ; Load the ADC0GNH address
MOV ADC0L,#06CH           ; Load the upper byte of 0x6CA to ADC0GNH
MOV ADC0H,#07H            ; Load the ADC0GNL address
MOV ADC0L,#0A0H           ; Load the lower nibble of 0x6CA to ADC0GNL
MOV ADC0H,#08H            ; Load the ADC0GNA address
MOV ADC0L,#01H            ; Set the GAINADD bit
ANL ADC0CF,#0FEH          ; GAINEN = 0
```

SFR Definition 5.4. ADC0CF: ADC0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	AD0SC[4:0]					AD0RPT[1:0]		GAINEN
Type	R/W					R/W	R/W	R/W
Reset	1	1	1	1	1	0	0	0

SFR Address = 0xBC; SFR Page = 0x00

Bit	Name	Function
7:3	AD0SC[4:0]	ADC0 SAR Conversion Clock Period Bits. SAR Conversion clock is derived from system clock by the following equation, where AD0SC refers to the 5-bit value held in bits AD0SC4–0. SAR Conversion clock requirements are given in the ADC specification table BURSTEN = 0: FCLK is the current system clock BURSTEN = 1: FCLK is a maximum of 30 MHz, independent of the current system clock.. $AD0SC = \frac{FCLK}{CLK_{SAR}} - 1$ Note: Round up the result of the calculation for AD0SC
2:1	A0RPT[1:0]	ADC0 Repeat Count Controls the number of conversions taken and accumulated between ADC0 End of Conversion (ADCINT) and ADC0 Window Comparator (ADCWINT) interrupts. A convert start is required for each conversion unless Burst Mode is enabled. In Burst Mode, a single convert start can initiate multiple self-timed conversions. Results in both modes are accumulated in the ADC0H:ADC0L register. When AD0RPT1–0 are set to a value other than '00', the AD0LJST bit in the ADC0CN register must be set to '0' (right justified). 00: 1 conversion is performed. 01: 4 conversions are performed and accumulated. 10: 8 conversions are performed and accumulated. 11: 16 conversions are performed and accumulated.
0	GAINEN	Gain Enable Bit. Controls the gain programming. Refer to Section “5.3. Selectable Gain” on page 35 for information about using this bit.

Table 6.6. Internal High-Frequency Oscillator Electrical Characteristics

V_{DD} = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	IFCN = 111b; VDD ≥ VREGMIN ¹	24 – 0.5%	24 ²	24 + 0.5%	MHz
	IFCN = 111b; VDD < VREGMIN ¹	24 – 1.0%	24 ²	24 + 1.0%	
Oscillator Supply Current (from V _{DD})	Internal Oscillator On OSCICN[7:6] = 11b	—	880	1300	μA
Internal Oscillator Suspend OSCICN[7:6] = 00b ZTCEN = 1	Temp = 25 °C	—	67	—	
	Temp = 85 °C		90		
	Temp = 125 °C		130		
Wake-up Time From Suspend	OSCICN[7:6] = 00b	—	1	—	μs
Power Supply Sensitivity	Constant Temperature	—	0.11	—	%/V
Temperature Sensitivity ³	Constant Supply				ppm/°C ppm/°C ²
	TC ₁	—	5.0	—	
	TC ₂	—	–0.65	—	
<div>1. VREGMIN is the minimum output of the voltage regulator for its low setting (REG0CN: REG0MD = 0b). See Table 6.8, “Voltage Regulator Electrical Characteristics,” on page 54.</div> <div>2. This is the average frequency across the operating temperature range</div> <div>3. Use temperature coefficients TC₁ and TC₂ to calculate the new internal oscillator frequency using the following equation:</div> <div>$f(T) = f_0 \times (1 + TC_1 \times (T - T_0) + TC_2 \times (T - T_0)^2)$</div> <div>where f₀ is the internal oscillator frequency at 25 °C and T₀ is 25 °C.</div>					

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Comparator outputs can be polled in software, used as an interrupt source, and/or routed to a Port pin. When routed to a Port pin, Comparator outputs are available asynchronous or synchronous to the system clock; the asynchronous output is available even in STOP mode (with no system clock active). When disabled, the Comparator output (if assigned to a Port I/O pin via the Crossbar) defaults to the logic low state, and the power supply to the comparator is turned off. See Section “18.3. Priority Crossbar Decoder” on page 150 for details on configuring Comparator outputs via the digital Crossbar. Comparator inputs can be externally driven from -0.25 V to $(V_{DD}) + 0.25\text{ V}$ without damage or upset. The complete Comparator electrical specifications are given in Table 6.12.

The Comparator response time may be configured in software via the CPTnMD registers (see SFR Definition 8.2). Selecting a longer response time reduces the Comparator supply current. See Table 6.12 for complete timing and supply current requirements.

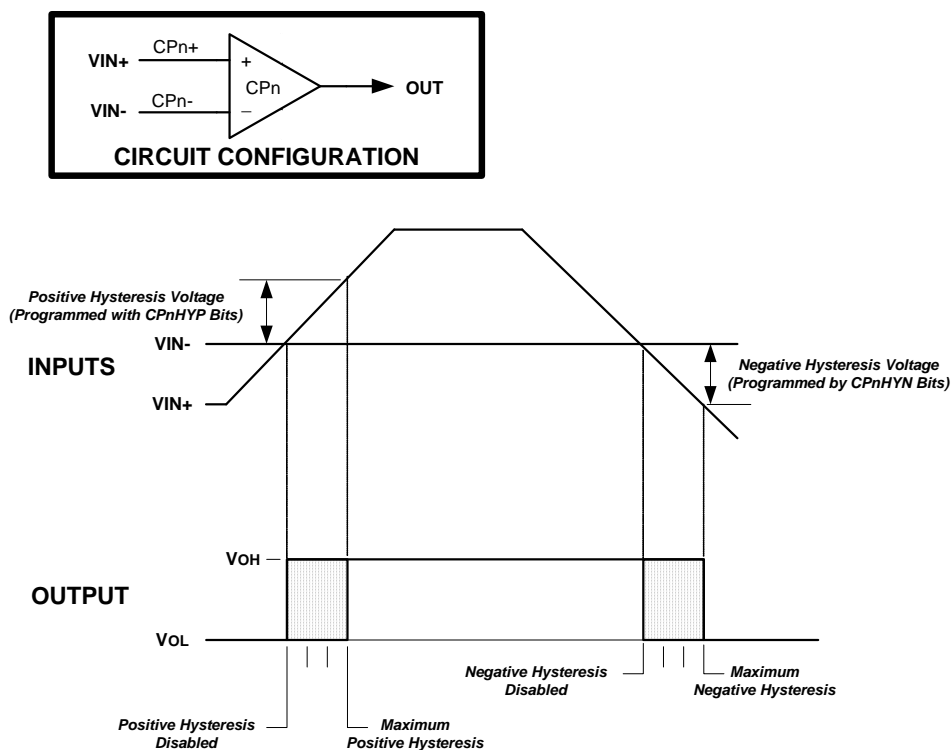


Figure 8.2. Comparator Hysteresis Plot

Comparator hysteresis is software-programmable via its Comparator Control register CPTnCN.

The amount of negative hysteresis voltage is determined by the settings of the CPnHYN bits. As shown in Figure 8.2, various levels of negative hysteresis can be programmed, or negative hysteresis can be disabled. In a similar way, the amount of positive hysteresis is determined by the setting the CPnHYP bits.

Comparator interrupts can be generated on both rising-edge and falling-edge output transitions. (For Interrupt enable and priority control, see “13. Interrupts”.) The CPnFIF flag is set to 1 upon a Comparator falling-edge, and the CPnRIF flag is set to 1 upon the Comparator rising-edge. Once set, these bits remain set until cleared by software. The output state of the Comparator can be obtained at any time by reading the CPnOUT bit. The Comparator is enabled by setting the CPnEN bit to 1, and is disabled by clearing this bit to 0.

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SFR Definition 8.4. CPT1MD: Comparator1 Mode Selection

Bit	7	6	5	4	3	2	1	0
Name			CP1RIE	CP1FIE			CP1MD[1:0]	
Type	R	R	R/W	R/W	R	R	R/W	
Reset	0	0	0	0	0	0	1	0

SFR Address = 0x9E; SFR Page = 0x00

Bit	Name	Function
7:6	Unused	Read = 00b, Write = Don't Care.
5	CP1RIE	Comparator1 Rising-Edge Interrupt Enable. 0: Comparator1 Rising-edge interrupt disabled. 1: Comparator1 Rising-edge interrupt enabled.
4	CP1FIE	Comparator1 Falling-Edge Interrupt Enable. 0: Comparator1 Falling-edge interrupt disabled. 1: Comparator1 Falling-edge interrupt enabled.
3:2	Unused	Read = 00b, Write = don't care.
1:0	CP1MD[1:0]	Comparator1 Mode Select. These bits affect the response time and power consumption for Comparator1. 00: Mode 0 (Fastest Response Time, Highest Power Consumption) 01: Mode 1 10: Mode 2 11: Mode 3 (Slowest Response Time, Lowest Power Consumption)

Table 10.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
XRL A, #data	Exclusive-OR immediate to A	2	2
XRL direct, A	Exclusive-OR A to direct byte	2	2
XRL direct, #data	Exclusive-OR immediate to direct byte	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through Carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through Carry	1	1
SWAP A	Swap nibbles of A	1	1
Data Transfer			
MOV A, Rn	Move Register to A	1	1
MOV A, direct	Move direct byte to A	2	2
MOV A, @Ri	Move indirect RAM to A	1	2
MOV A, #data	Move immediate to A	2	2
MOV Rn, A	Move A to Register	1	1
MOV Rn, direct	Move direct byte to Register	2	2
MOV Rn, #data	Move immediate to Register	2	2
MOV direct, A	Move A to direct byte	2	2
MOV direct, Rn	Move Register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	2	2
MOV direct, #data	Move immediate to direct byte	3	3
MOV @Ri, A	Move A to indirect RAM	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	2	2
MOV @Ri, #data	Move immediate to indirect RAM	2	2
MOV DPTR, #data16	Load DPTR with 16-bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A, @A+PC	Move code byte relative PC to A	1	3
MOVX A, @Ri	Move external data (8-bit address) to A	1	3
MOVX @Ri, A	Move A to external data (8-bit address)	1	3
MOVX A, @DPTR	Move external data (16-bit address) to A	1	3
MOVX @DPTR, A	Move A to external data (16-bit address)	1	3
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange Register with A	1	1
XCH A, direct	Exchange direct byte with A	2	2
XCH A, @Ri	Exchange indirect RAM with A	1	2
XCHD A, @Ri	Exchange low nibble of indirect RAM with A	1	2
Boolean Manipulation			
CLR C	Clear Carry	1	1
CLR bit	Clear direct bit	2	2
Note: Certain instructions take a variable number of clock cycles to execute depending on instruction alignment and the FLRT setting (SFR Definition 14.3).			

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SFR Definition 10.6. PSW: Program Status Word

Bit	7	6	5	4	3	2	1	0
Name	CY	AC	F0	RS[1:0]		OV	F1	PARITY
Type	R/W	R/W	R/W	R/W		R/W	R/W	R
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD0; SFR Page = All Pages; Bit-Addressable

Bit	Name	Function
7	CY	Carry Flag. This bit is set when the last arithmetic operation resulted in a carry (addition) or a borrow (subtraction). It is cleared to logic 0 by all other arithmetic operations.
6	AC	Auxiliary Carry Flag. This bit is set when the last arithmetic operation resulted in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to logic 0 by all other arithmetic operations.
5	F0	User Flag 0. This is a bit-addressable, general purpose flag for use under software control.
4:3	RS[1:0]	Register Bank Select. These bits select which register bank is used during register accesses. 00: Bank 0, Addresses 0x00-0x07 01: Bank 1, Addresses 0x08-0x0F 10: Bank 2, Addresses 0x10-0x17 11: Bank 3, Addresses 0x18-0x1F
2	OV	Overflow Flag. This bit is set to 1 under the following circumstances: <ul style="list-style-type: none"> ■ An ADD, ADDC, or SUBB instruction causes a sign-change overflow. ■ A MUL instruction results in an overflow (result is greater than 255). ■ A DIV instruction causes a divide-by-zero condition. The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases.
1	F1	User Flag 1. This is a bit-addressable, general purpose flag for use under software control.
0	PARITY	Parity Flag. This bit is set to logic 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even.

SFR Definition 12.3. SFRNEXT: SFR Next

Bit	7	6	5	4	3	2	1	0
Name	SFRNEXT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x85; SFR Page = All Pages

Bit	Name	Function
7:0	SFRNEXT[7:0]	<p>SFR Page Bits.</p> <p>This is the value that will go to the SFR Page register upon a return from interrupt.</p> <p>Write: Sets the SFR Page contained in the second byte of the SFR Stack. This will cause the SFRPAGE SFR to have this SFR page value upon a return from interrupt.</p> <p>Read: Returns the value of the SFR page contained in the second byte of the SFR stack.</p> <p>SFR page context is retained upon interrupts/return from interrupts in a 3 byte SFR Page Stack: SFRPAGE is the first entry, SFRNEXT is the second, and SFRLAST is the third entry. The SFR stack bytes may be used alter the context in the SFR Page Stack, and will not cause the stack to “push” or “pop”. Only interrupts and return from interrupts cause pushes and pops of the SFR Page Stack.</p>

SFR Definition 13.1. IE: Interrupt Enable

Bit	7	6	5	4	3	2	1	0
Name	EA	ESPI0	ET2	ES0	ET1	EX1	ET0	EX0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA8; Bit-Addressable; SFR Page = All Pages

Bit	Name	Function
7	EA	Enable All Interrupts. Globally enables/disables all interrupts. It overrides individual interrupt mask settings. 0: Disable all interrupt sources. 1: Enable each interrupt according to its individual mask setting.
6	ESPI0	Enable Serial Peripheral Interface (SPI0) Interrupt. This bit sets the masking of the SPI0 interrupts. 0: Disable all SPI0 interrupts. 1: Enable interrupt requests generated by SPI0.
5	ET2	Enable Timer 2 Interrupt. This bit sets the masking of the Timer 2 interrupt. 0: Disable Timer 2 interrupt. 1: Enable interrupt requests generated by the TF2L or TF2H flags.
4	ES0	Enable UART0 Interrupt. This bit sets the masking of the UART0 interrupt. 0: Disable UART0 interrupt. 1: Enable UART0 interrupt.
3	ET1	Enable Timer 1 Interrupt. This bit sets the masking of the Timer 1 interrupt. 0: Disable all Timer 1 interrupt. 1: Enable interrupt requests generated by the TF1 flag.
2	EX1	Enable External Interrupt 1. This bit sets the masking of External Interrupt 1. 0: Disable external interrupt 1. 1: Enable interrupt requests generated by the $\overline{\text{INT1}}$ input.
1	ET0	Enable Timer 0 Interrupt. This bit sets the masking of the Timer 0 interrupt. 0: Disable all Timer 0 interrupt. 1: Enable interrupt requests generated by the TF0 flag.
0	EX0	Enable External Interrupt 0. This bit sets the masking of External Interrupt 0. 0: Disable external interrupt 0. 1: Enable interrupt requests generated by the $\overline{\text{INT0}}$ input.

14.1.3. Flash Write Procedure

Flash bytes are programmed by software with the following sequence:

1. Disable interrupts (recommended).
2. Erase the 512-byte Flash page containing the target location, as described in Section 14.1.2.
3. Set the PSWE bit (register PSCTL).
4. Clear the PSEE bit (register PSCTL).
5. Write the first key code to FLKEY: 0xA5.
6. Write the second key code to FLKEY: 0xF1.
7. Using the MOVX instruction, write a single data byte to the desired location within the 512-byte sector.
8. Clear the PSWE bit.

Steps 5–7 must be repeated for each byte to be written. After Flash writes are complete, PSWE should be cleared so that MOVX instructions do not target program memory.

14.1.4. Flash Write Optimization

The Flash write procedure includes a block write option to optimize the time to perform consecutive byte writes. When block write is enabled by setting the CHBLKW bit (CCH0CN.0), writes to two consecutive bytes in Flash require the same amount of time as a single byte write. This is performed by caching the first byte that is written to Flash and then committing both bytes to Flash when the second byte is written. When block writes are enabled, if the second write does not occur, the first data byte written is not actually written to Flash. Flash bytes with block write enabled are programmed by software with the following sequence:

1. Disable interrupts (recommended).
2. Erase the 512-byte Flash page containing the target location, as described in Section 14.1.2.
3. Set the CHBLKW bit (register CCH0CN).
4. Set the PSWE bit (register PSCTL).
5. Clear the PSEE bit (register PSCTL).
6. Write the first key code to FLKEY: 0xA5.
7. Write the second key code to FLKEY: 0xF1.
8. Using the MOVX instruction, write the first data byte to the desired location within the 512-byte sector.
9. Write the first key code to FLKEY: 0xA5.
10. Write the second key code to FLKEY: 0xF1.
11. Using the MOVX instruction, write the second data byte to the desired location within the 512-byte sector. The location of the second byte must be the next higher address from the first data byte.
12. Clear the PSWE bit.
13. Clear the CHBLKW bit.

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SFR Definition 16.2. RSTSRC: Reset Source

Bit	7	6	5	4	3	2	1	0
Name		FERROR	CORSEF	SWRSF	WDTRSF	MCDRSF	PORSF	PINRSF
Type	R	R	R/W	R/W	R	R/W	R/W	R
Reset	0	Varies	Varies	Varies	Varies	Varies	Varies	Varies

SFR Address = 0xEF; SFR Page = 0x00

Bit	Name	Description	Write	Read
7	Unused	Unused.	Don't care.	0
6	FERROR	Flash Error Reset Flag.	N/A	Set to 1 if Flash read/write/erase error caused the last reset.
5	CORSEF	Comparator0 Reset Enable and Flag.	Writing a 1 enables Comparator0 as a reset source (active-low).	Set to 1 if Comparator0 caused the last reset.
4	SWRSF	Software Reset Force and Flag.	Writing a 1 forces a system reset.	Set to 1 if last reset was caused by a write to SWRSF.
3	WDTRSF	Watchdog Timer Reset Flag.	N/A	Set to 1 if Watchdog Timer overflow caused the last reset.
2	MCDRSF	Missing Clock Detector Enable and Flag.	Writing a 1 enables the Missing Clock Detector. The MCD triggers a reset if a missing clock condition is detected.	Set to 1 if Missing Clock Detector timeout caused the last reset.
1	PORSF	Power-On/V_{DD} Monitor Reset Flag, and V_{DD} monitor Reset Enable.	Writing a 1 enables the V _{DD} monitor as a reset source. Writing 1 to this bit before the V_{DD} monitor is enabled and stabilized may cause a system reset.	Set to 1 anytime a power-on or V _{DD} monitor reset occurs. When set to 1 all other RSTSRC flags are indeterminate.
0	PINRSF	HW Pin Reset Flag.	N/A	Set to 1 if RST pin caused the last reset.

Note: Do not use read-modify-write operations on this register

Table 18.2. Port I/O Assignment for Digital Functions

Digital Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
Any pin used for GPIO	P0.0–P3.0*	P0SKIP, P1SKIP, P2SKIP, P3SKIP
*Note: P2.2–P2.7, P3.0 are only available on the 32-pin packages.		

18.2.3. Assigning Port I/O Pins to External Digital Event Capture Functions

External digital event capture functions can be used to trigger an interrupt or wake the device from a low power mode when a transition occurs on a digital I/O pin. The digital event capture functions do not require dedicated pins and will function on both GPIO pins (PnSKIP = 1) and pins in use by the Crossbar (PnSKIP = 0). External digital event capture functions cannot be used on pins configured for analog I/O. Table 18.3 shows all available external digital event capture functions.

Table 18.3. Port I/O Assignment for External Digital Event Capture Functions

Digital Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
External Interrupt 0	P1.0–P1.7	IT01CF
External Interrupt 1	P1.0–P1.7	IT01CF
Port Match	P0.0–P3.0*	P0MASK, P0MAT P1MASK, P1MAT P2MASK, P2MAT P3MASK, P3MAT
*Note: P2.2–P2.7, P3.0 are only available on the 32-pin packages.		

18.3. Priority Crossbar Decoder

The Priority Crossbar Decoder (Figure 18.3) assigns a priority to each I/O function, starting at the top with UART0. When a digital resource is selected, the least-significant unassigned Port pin is assigned to that resource excluding UART0, which is always assigned to pins P0.4 and P0. If a Port pin is assigned, the Crossbar skips that pin when assigning the next selected resource. Additionally, the Crossbar will skip Port pins whose associated bits in the PnSKIP registers are set. The PnSKIP registers allow software to skip Port pins that are to be used for analog input, dedicated functions, or GPIO.

Because of the nature of Priority Crossbar Decoder, not all peripherals can be located on all port pins. Figure 18.3 maps peripherals to the potential port pins on which the peripheral I/O can appear.

Important Note on Crossbar Configuration: If a Port pin is claimed by a peripheral without use of the Crossbar, its corresponding PnSKIP bit should be set. This applies to P0.0 if VREF is used, P0.1 if the ADC is configured to use the external conversion start signal (CNVSTR), P0.3 and/or P0.2 if the external oscillator circuit is enabled, and any selected ADC or Comparator inputs. The Crossbar skips selected pins as if they were already assigned, and moves to the next unassigned pin.

LIN Register Definition 19.4. LIN0DTn: LIN0 Data Byte n

Bit	7	6	5	4	3	2	1	0
Name	DATAn[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Indirect Address: LIN0DT1 = 0x00, LIN0DT2 = 0x01, LIN0DT3 = 0x02, LIN0DT4 = 0x03, LIN0DT5 = 0x04, LIN0DT6 = 0x05, LIN0DT7 = 0x06, LIN0DT8 = 0x07

Bit	Name	Function
7:0	DATAn[7:0]	LIN Data Byte n. Serial Data Byte that is received or transmitted across the LIN interface.

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LIN Register Definition 19.5. LIN0CTRL: LIN0 Control Register

Bit	7	6	5	4	3	2	1	0
Name	STOP	SLEEP	TXRX	DTACK	RSTINT	RSTERR	WUPREQ	STREQ
Type	W	R/W	R/W	R/W	W	W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Indirect Address = 0x08

Bit	Name	Function
7	STOP	Stop Communication Processing Bit. (slave mode only) This bit always reads as 0. 0: No effect. 1: Block the processing of LIN communications until the next SYNC BREAK signal.
6	SLEEP	Sleep Mode Bit. (slave mode only) 0: Wake the device after receiving a Wakeup interrupt. 1: Put the device into sleep mode after receiving a Sleep Mode frame or a bus idle timeout.
5	TXRX	Transmit / Receive Selection Bit. 0: Current frame is a receive operation. 1: Current frame is a transmit operation.
4	DTACK	Data Acknowledge Bit. (slave mode only) Set to 1 after handling a data request interrupt to acknowledge the transfer. The bit will automatically be cleared to 0 by the LIN controller.
3	RSTINT	Reset Interrupt Bit. This bit always reads as 0. 0: No effect. 1: Reset the LININT bit (LIN0ST.3).
2	RSTERR	Reset Error Bit. This bit always reads as 0. 0: No effect. 1: Reset the error bits in LIN0ST and LIN0ERR.
1	WUPREQ	Wakeup Request Bit. Set to 1 to terminate sleep mode by sending a wakeup signal. The bit will automatically be cleared to 0 by the LIN controller.
0	STREQ	Start Request Bit. (master mode only) 1: Start a LIN transmission. This should be set only after loading the identifier, data length and data buffer if necessary. The bit is reset to 0 upon transmission completion or error detection.

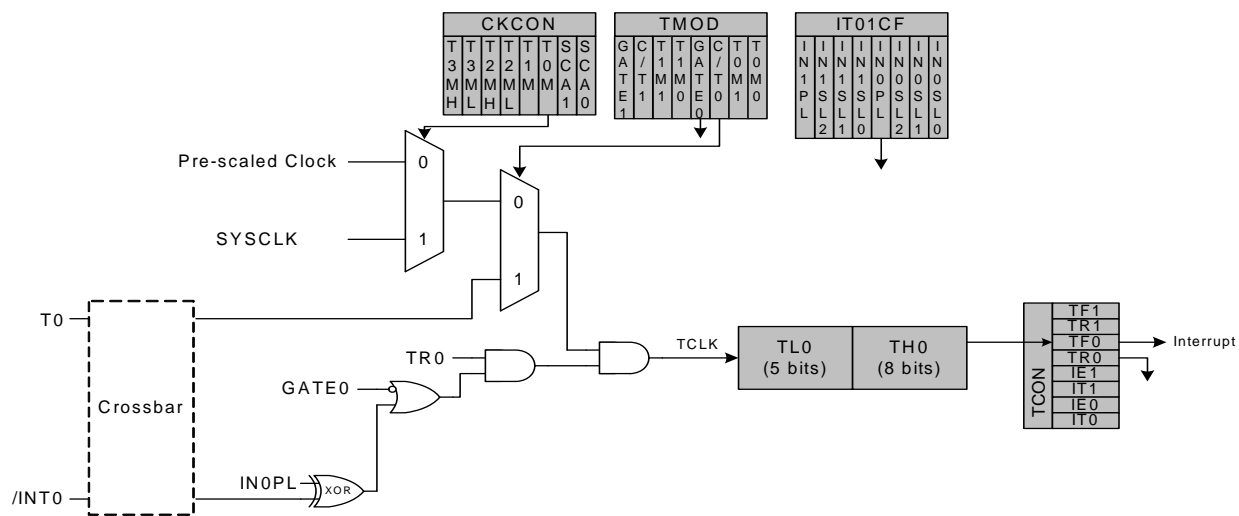


Figure 23.1. T0 Mode 0 Block Diagram

23.1.2. Mode 1: 16-bit Counter/Timer

Mode 1 operation is the same as Mode 0, except that the counter/timer registers use all 16 bits. The counter/timers are enabled and configured in Mode 1 in the same manner as for Mode 0.

23.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload

Mode 2 configures Timer 0 and Timer 1 to operate as 8-bit counter/timers with automatic reload of the start value. TL0 holds the count and TH0 holds the reload value. When the counter in TL0 overflows from all ones to 0x00, the timer overflow flag TF0 (TCON.5) is set and the counter in TL0 is reloaded from TH0. If Timer 0 interrupts are enabled, an interrupt will occur when the TF0 flag is set. The reload value in TH0 is not changed. TL0 must be initialized to the desired value before enabling the timer for the first count to be correct. When in Mode 2, Timer 1 operates identically to Timer 0.

Both counter/timers are enabled and configured in Mode 2 in the same manner as Mode 0. Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or when the input signal INT0 is active as defined by bit IN0PL in register IT01CF (see Section “13.3. External Interrupts INT0 and INT1” on page 115 for details on the external input signals INT0 and INT1).

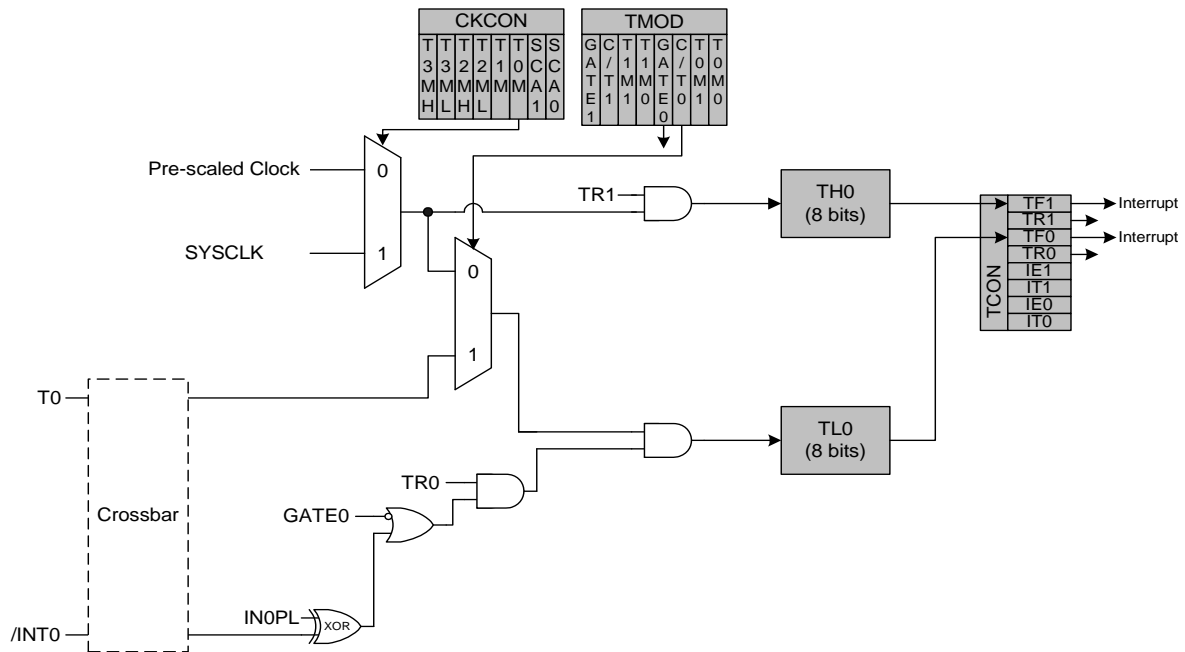


Figure 23.3. T0 Mode 3 Block Diagram

C8051F54x

SFR Definition 23.16. TMR3L: Timer 3 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x94; SFR Page = 0x00

Bit	Name	Function
7:0	TMR3L[7:0]	Timer 3 Low Byte. In 16-bit mode, the TMR3L register contains the low byte of the 16-bit Timer 3. In 8-bit mode, TMR3L contains the 8-bit low byte timer value.

SFR Definition 23.17. TMR3H Timer 3 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3H[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x95; SFR Page = 0x00

Bit	Name	Function
7:0	TMR3H[7:0]	Timer 3 High Byte. In 16-bit mode, the TMR3H register contains the high byte of the 16-bit Timer 3. In 8-bit mode, TMR3H contains the 8-bit high byte timer value.

24. Programmable Counter Array

The Programmable Counter Array (PCA0) provides enhanced timer functionality while requiring less CPU intervention than the standard 8051 counter/timers. The PCA consists of a dedicated 16-bit counter/timer and six 16-bit capture/compare modules. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the Crossbar to Port I/O when enabled. The counter/timer is driven by a programmable timebase that can select between six sources: system clock, system clock divided by four, system clock divided by twelve, the external oscillator clock source divided by 8, Timer 0 overflows, or an external clock signal on the ECI input pin. Each capture/compare module may be configured to operate independently in one of six modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, 8 to 11-Bit PWM, or 16-Bit PWM (each mode is described in Section "24.3. Capture/Compare Modules" on page 252). The external oscillator clock option is ideal for real-time clock (RTC) functionality, allowing the PCA to be clocked by a precision external oscillator while the internal oscillator drives the system clock. The PCA is configured and controlled through the system controller's Special Function Registers. The PCA block diagram is shown in Figure 24.1

Important Note: The PCA Module 5 may be used as a watchdog timer (WDT), and is enabled in this mode following a system reset. **Access to certain PCA registers is restricted while WDT mode is enabled.** See Section 24.4 for details.

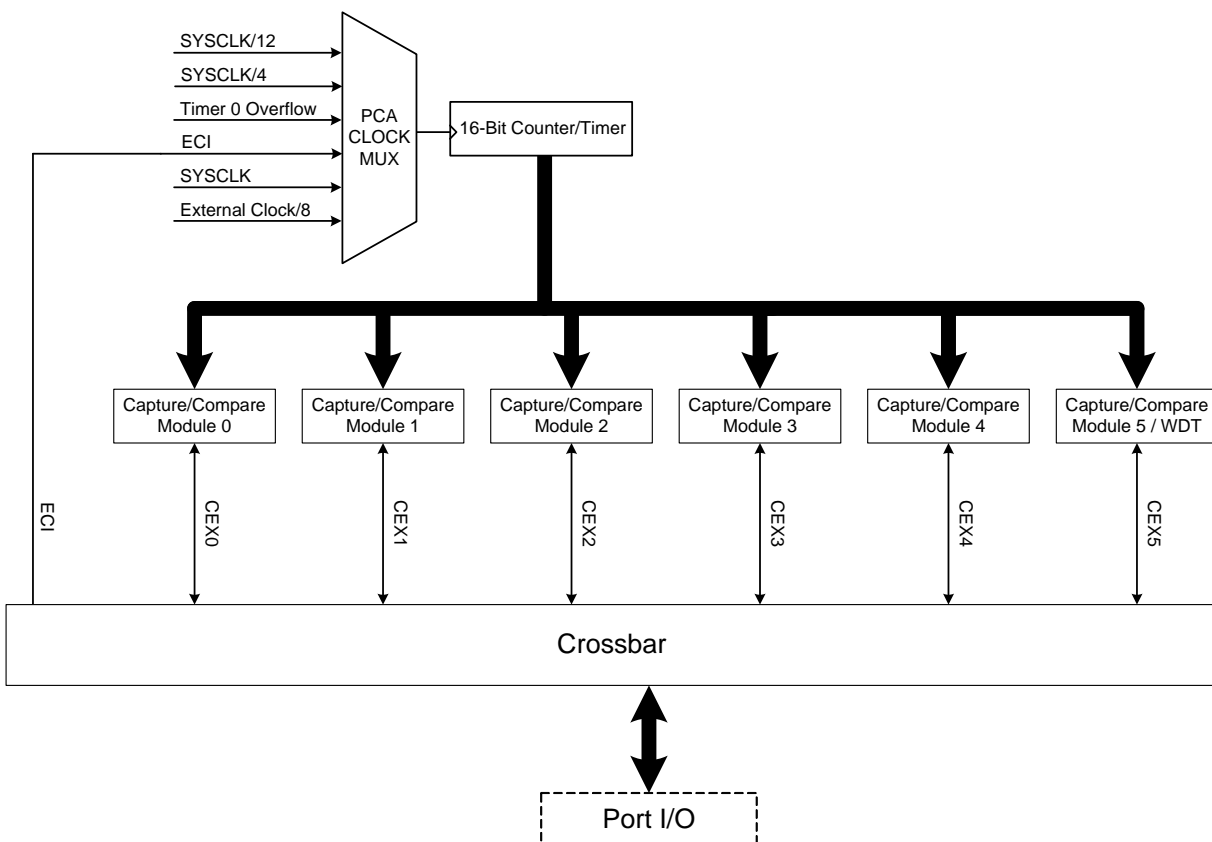


Figure 24.1. PCA Block Diagram