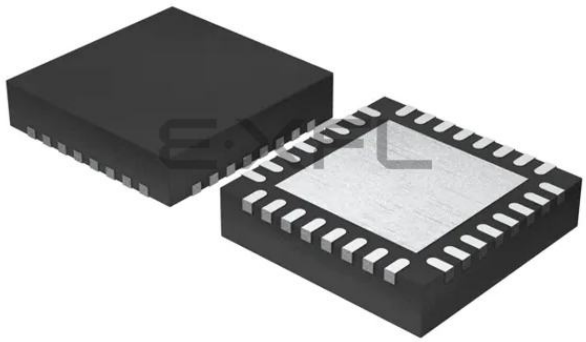

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 25x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f545-im

3. Pin Definitions

Table 3.1. Pin Definitions for the C8051F54x

Name	Pin 'F540/1/4/5 (32-pin)	Pin 'F542/3/6/7 (24-pin)	Type	Description
VDD	4	3		Digital Supply Voltage. Must be connected.
GND	6	4		Digital Ground. Must be connected.
VDDA	5	—		Analog Supply Voltage. Must be connected. Connected internally to VDD on the 24-pin packages.
GNDA	7	5		Analog Ground. Must be connected.
VREGIN	3	2		Voltage Regulator Input
VIO	2	1		Port I/O Supply Voltage. Must be connected.
$\overline{\text{RST}}$/ C2CK	10	8	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} Monitor. Clock signal for the C2 Debug Interface.
P2.1/ C2D	—	7	D I/O or A In D I/O	Port 2.1. See SFR Definition 18.20 for a description. Bi-directional data signal for the C2 Debug Interface.
P3.0/ C2D	9	—	D I/O or A In D I/O	Port 3.0. See SFR Definition 18.24 for a description. Bi-directional data signal for the C2 Debug Interface.
P0.0	8	6	D I/O or A In	Port 0.0. See SFR Definition 18.12 for a description.
P0.1	1	24	D I/O or A In	Port 0.1
P0.2	32	23	D I/O or A In	Port 0.2
P0.3	31	22	D I/O or A In	Port 0.3
P0.4	30	21	D I/O or A In	Port 0.4
P0.5	29	20	D I/O or A In	Port 0.5
P0.6	28	19	D I/O or A In	Port 0.6
P0.7	27	18	D I/O or A In	Port 0.7
P1.0	26	17	D I/O or A In	Port 1.0. See SFR Definition 18.16 for a description.
P1.1	25	16	D I/O or A In	Port 1.1.
P1.2	24	15	D I/O or A In	Port 1.2.

4.3. QFN-24 Package Specifications

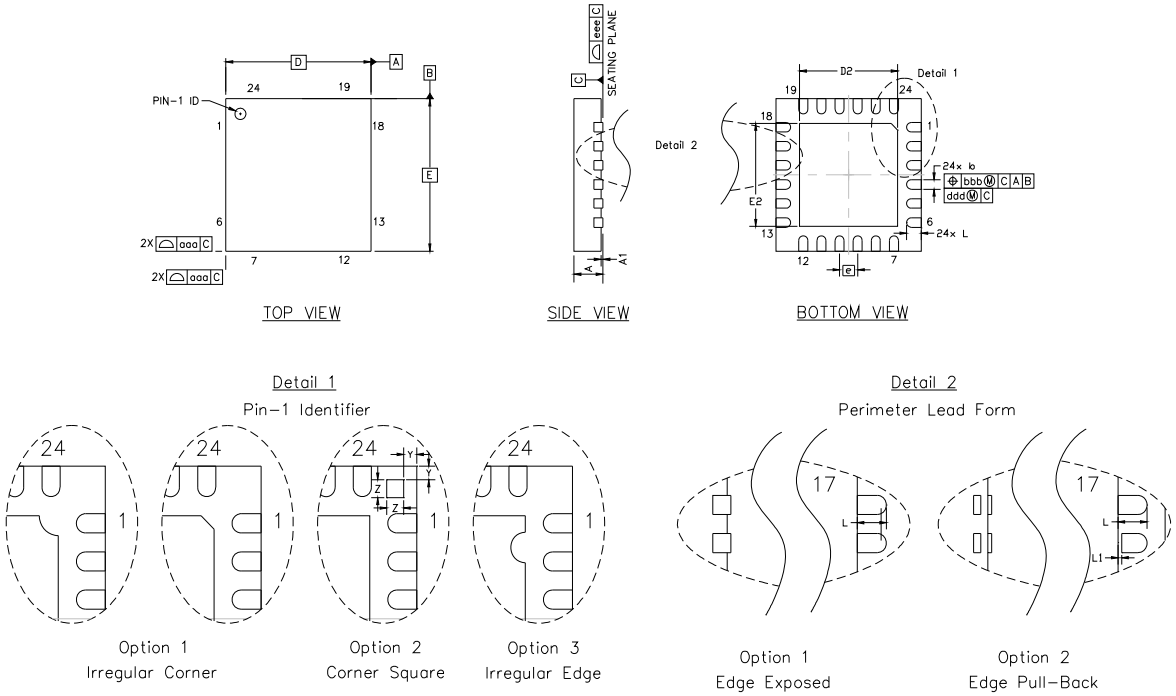


Figure 4.5. QFN-24 Package Drawing

Table 4.5. QFN-24 Package Dimensions

Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.70	0.75	0.80	L	0.30	0.40	0.50
A1	0.00	0.02	0.05	L1	0.00		0.15
b	0.18	0.25	0.30	aaa			0.15
D	4.00 BSC			bbb			0.10
D2	2.55	2.70	2.80	ddd			0.05
e	0.50 BSC			eee			0.08
E	4.00 BSC			Z		0.24	
E2	2.55	2.70	2.80	Y		0.18	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD, except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table 6.7. Clock Multiplier Electrical Specifications

V_{DD} = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Frequency (Fcm_{in})		2	—	—	MHz
Output Frequency		—	—	50	MHz
Power Supply Current		—	0.9	1.9	mA

Table 6.8. Voltage Regulator Electrical Characteristics

V_{DD} = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Range (V_{REGIN})*		1.8*	—	5.25	V
Dropout Voltage (V_{DO})	Maximum Current = 50 mA	—	10	—	mV/mA
Output Voltage (V_{DD})	2.1 V operation (REG0MD = 0) 2.6 V operation (REG0MD = 1)	2.0 2.5	2.1 2.6	2.25 2.75	V
Bias Current		—	1	9	µA
Dropout Indicator Detection Threshold	With respect to VDD	–0.21	—	–0.02	V
Output Voltage Temperature Coefficient		—	0.29	—	mV/°C
VREG Settling Time	50 mA load with V_{REGIN} = 2.4 V and V_{DD} load capacitor of 4.8 µF	—	450	—	µs
***Note:** The minimum input voltage is 1.8 V or V_{DD} + V_{DO}(max load), whichever is greater					

SFR Definition 12.4. SFRLAST: SFR Last

Bit	7	6	5	4	3	2	1	0
Name	SFRLAST[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA7; SFR Page = All Pages

Bit	Name	Function
7:0	SFRLAST[7:0]	**SFR Page Stack Bits.** This is the value that will go to the SFRNEXT register upon a return from interrupt. Write: Sets the SFR Page in the last entry of the SFR Stack. This will cause the SFRNEXT SFR to have this SFR page value upon a return from interrupt. Read: Returns the value of the SFR page contained in the last entry of the SFR stack. SFR page context is retained upon interrupts/return from interrupts in a 3 byte SFR Page Stack: SFRPAGE is the first entry, SFRNEXT is the second, and SFRLAST is the third entry. The SFR stack bytes may be used alter the context in the SFR Page Stack, and will not cause the stack to “push” or “pop”. Only interrupts and return from interrupts cause pushes and pops of the SFR Page Stack.

Table 12.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
PCA0CPH5	0xCF	PCA Capture 5 High	268
PCA0CPL0	0xFB	PCA Capture 0 Low	268
PCA0CPL1	0xE9	PCA Capture 1 Low	268
PCA0CPL2	0xEB	PCA Capture 2 Low	268
PCA0CPL3	0xED	PCA Capture 3 Low	268
PCA0CPL4	0xFD	PCA Capture 4 Low	268
PCA0CPL5	0xCE	PCA Capture 5 Low	268
PCA0CPM0	0xDA	PCA Module 0 Mode Register	266
PCA0CPM1	0xDB	PCA Module 1 Mode Register	266
PCA0CPM2	0xDC	PCA Module 2 Mode Register	266
PCA0CPM3	0xDD	PCA Module 3 Mode Register	266
PCA0CPM4	0xDE	PCA Module 4 Mode Register	266
PCA0CPM5	0xDF	PCA Module 5 Mode Register	266
PCA0H	0xFA	PCA Counter High	267
PCA0L	0xF9	PCA Counter Low	267
PCA0MD	0xD9	PCA Mode	264
PCA0PWM	0xD9	PCA PWM Configuration	265
PCON	0x87	Power Control	128
PSCTL	0x8F	Program Store R/W Control	122
PSW	0xD0	Program Status Word	83
REF0CN	0xD1	Voltage Reference Control	62
REG0CN	0xC9	Voltage Regulator Control	73
RSTSRC	0xEF	Reset Source Configuration/Status	134
SBCON0	0xAB	UART0 Baud Rate Generator Control	212
SBRLH0	0xAD	UART0 Baud Rate Reload High Byte	213
SBRLL0	0xAC	UART0 Baud Rate Reload Low Byte	213
SBUF0	0x99	UART0 Data Buffer	212
SCON0	0x98	UART0 Control	210
SFR0CN	0x84	SFR Page Control	96
SFRLAST	0x86	SFR Stack Last Page	99
SFRNEXT	0x85	SFR Stack Next Page	98
SFRPAGE	0xA7	SFR Page Select	97
SMB0CF	0xC1	SMBus0 Configuration	193
SMB0CN	0xC0	SMBus0 Control	195
SMB0DAT	0xC2	SMBus0 Data	197
SMOD0	0xA9	UART0 Mode	211

Table 12.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
SN0	0xF9	Serial Number 0	84
SN1	0xFA	Serial Number 1	84
SN2	0xFB	Serial Number 2	84
SN3	0xFC	Serial Number 3	84
SP	0x81	Stack Pointer	82
SPI0CFG	0xA1	SPI0 Configuration	221
SPI0CKR	0xA2	SPI0 Clock Rate Control	223
SPI0CN	0xF8	SPI0 Control	222
SPI0DAT	0xA3	SPI0 Data	223
TCON	0x88	Timer/Counter Control	233
TH0	0x8C	Timer/Counter 0 High	236
TH1	0x8D	Timer/Counter 1 High	236
TL0	0x8A	Timer/Counter 0 Low	235
TL1	0x8B	Timer/Counter 1 Low	235
TMOD	0x89	Timer/Counter Mode	234
TMR2CN	0xC8	Timer/Counter 2 Control	240
TMR2H	0xCD	Timer/Counter 2 High	242
TMR2L	0xCC	Timer/Counter 2 Low	242
TMR2RLH	0xCB	Timer/Counter 2 Reload High	241
TMR2RLL	0xCA	Timer/Counter 2 Reload Low	241
TMR3CN	0x91	Timer/Counter 3 Control	246
TMR3H	0x95	Timer/Counter 3 High	248
TMR3L	0x94	Timer/Counter 3 Low	248
TMR3RLH	0x93	Timer/Counter 3 Reload High	247
TMR3RLL	0x92	Timer/Counter 3 Reload Low	247
VDM0CN	0xFF	V_{DD} Monitor Control	132
XBR0	0xE1	Port I/O Crossbar Control 0	154
XBR1	0xE2	Port I/O Crossbar Control 1	155
XBR2	0xC7	Port I/O Crossbar Control 2	156

SFR Definition 13.6. EIP2: Extended Interrupt Priority Enabled 2

Bit	7	6	5	4	3	2	1	0
Name						PMAT		PREG0
Type	R	R	R	R	R	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF7; SFR Page = 0x00 and 0x0F

Bit	Name	Function
7:3	Unused	Read = 00000b; Write = Don't Care.
2	PMAT	**Port Match Interrupt Priority Control.** This bit sets the priority of the Port Match interrupt. 0: Port Match interrupt set to low priority level. 1: Port Match interrupt set to high priority level.
1	Unused	Read = 0b; Write = Don't Care.
0	PREG0	**Voltage Regulator Dropout Interrupt Priority Control.** This bit sets the priority of the Voltage Regulator Dropout interrupt. 0: Voltage Regulator Dropout interrupt set to low priority level. 1: Voltage Regulator Dropout interrupt set to high priority level.

16.1. Power-On Reset

During power-up, the device is held in a reset state and the $\overline{RST}$ pin is driven low until V_{DD} settles above V_{RST}. A delay occurs before the device is released from reset; the delay decreases as the V_{DD} ramp time increases (V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST}). Figure 16.2. plots the power-on and V_{DD} monitor reset timing.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000) software can read the PORSF flag to determine if a power-up was the cause of reset. The content of internal data memory should be assumed to be undefined after a power-on reset. The V_{DD} monitor is enabled following a power-on reset.

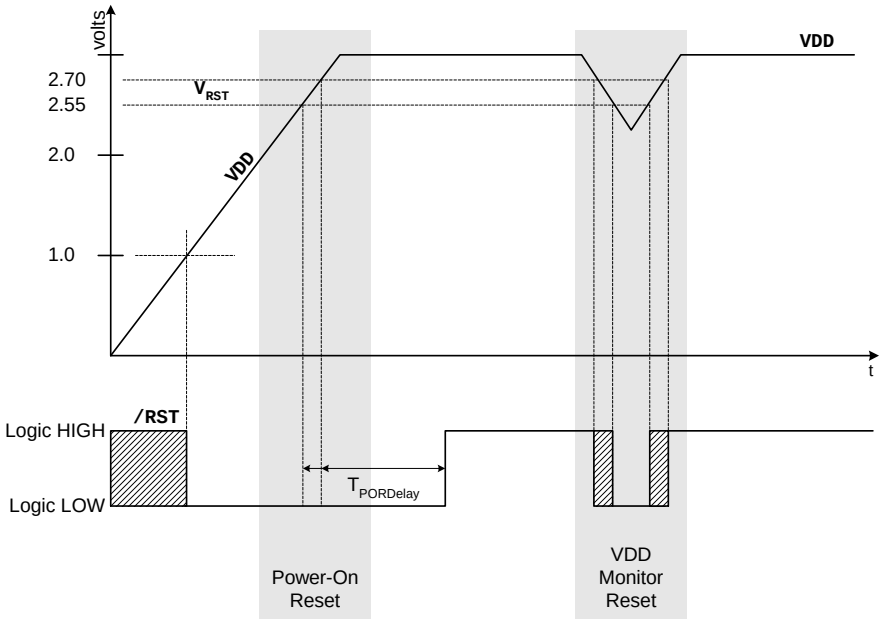


Figure 16.2. Power-On and V_{DD} Monitor Reset Timing

16.2. Power-Fail Reset/V_{DD} Monitor

When a power-down transition or power irregularity causes V_{DD} to drop below V_{RST}, the power supply monitor will drive the $\overline{RST}$ pin low and hold the CIP-51 in a reset state (see Figure 16.2). When V_{DD} returns to a level above V_{RST}, the CIP-51 will be released from the reset state. Note that even though internal data memory contents are not altered by the power-fail reset, it is impossible to determine if V_{DD} dropped below the level required for data retention. If the PORSF flag reads 1, the data may no longer be valid. The V_{DD} monitor is enabled after power-on resets. Its defined state (enabled/disabled) is not altered by any other reset source. For example, if the V_{DD} monitor is disabled by code and a software reset is performed, the V_{DD} monitor will still be disabled after the reset. **To protect the integrity of Flash contents, the V_{DD} monitor must be enabled to the higher setting (VDMLVL = 1) and selected as a reset source if software contains routines which erase or write Flash memory. If the V_{DD} monitor is not enabled and set to the high level, any erase or write performed on Flash memory will cause a Flash Error device reset.**

SFR Definition 17.2. OSCICN: Internal Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name	IOSCEN[1:0]		SUSPEND	IFRDY	Reserved	IFCN[2:0]		
Type	R/W	R/W	R/W	R	R	R/W		
Reset	1	1	0	1	0	0	0	0

SFR Address = 0xA1; SFR Page = 0x0F;

Bit	Name	Function
7:6	IOSCEN[1:0]	**Internal Oscillator Enable Bits.** 00: Oscillator Disabled. 01: Reserved. 10: Reserved. 11: Oscillator enabled in normal mode and disabled in suspend mode.
5	SUSPEND	**Internal Oscillator Suspend Enable Bit.** Setting this bit to logic 1 places the internal oscillator in SUSPEND mode. The internal oscillator resumes operation when one of the SUSPEND mode awakening events occurs.
4	IFRDY	**Internal Oscillator Frequency Ready Flag.** 0: Internal oscillator is not running at programmed frequency. 1: Internal oscillator is running at programmed frequency.
3	Reserved	Read = 0b; Write = 0b.
2:0	IFCN[2:0]	**Internal Oscillator Frequency Divider Control Bits.** 000: SYSCLK derived from Internal Oscillator divided by 128. 001: SYSCLK derived from Internal Oscillator divided by 64. 010: SYSCLK derived from Internal Oscillator divided by 32. 011: SYSCLK derived from Internal Oscillator divided by 16. 100: SYSCLK derived from Internal Oscillator divided by 8. 101: SYSCLK derived from Internal Oscillator divided by 4. 110: SYSCLK derived from Internal Oscillator divided by 2. 111: SYSCLK derived from Internal Oscillator divided by 1.

SFR Definition 18.3. XBR2: Port I/O Crossbar Register 1

Bit	7	6	5	4	3	2	1	0
Name	WEAKPUD	XBARE	Reserved					LIN0E
Type	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC7; SFR Page = 0x0F

Bit	Name	Function
7	WEAKPUD	**Port I/O Weak Pullup Disable.** 0: Weak Pullups enabled (except for Ports whose I/O are configured for analog mode). 1: Weak Pullups disabled.
6	XBARE	**Crossbar Enable.** 0: Crossbar disabled. 1: Crossbar enabled.
5:1	Reserved	Always Write to 00000b.
0	LIN0E	**LIN I/O Output Enable.** 0: LIN I/O unavailable at Port pin. 1: LIN_TX, LIN_RX routed to Port pins.

SFR Definition 18.8. P2MASK: Port 2 Mask Register

Bit	7	6	5	4	3	2	1	0
Name	P2MASK[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB2; SFR Page = 0x00

Bit	Name	Function
7:0	P2MASK[7:0]	**Port 2 Mask Value.** Selects P2 pins to be compared to the corresponding bits in P2MAT. 0: P2.n pin logic value is ignored and cannot cause a Port Mismatch event. 1: P2.n pin logic value is compared to P2MAT.n.
Note: Ports 2.2-P2.7 only available on 32-pin packages.		

SFR Definition 18.9. P2MAT: Port 2 Match Register

Bit	7	6	5	4	3	2	1	0
Name	P2MAT[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xB1; SFR Page = 0x00

Bit	Name	Function
7:0	P2MAT[7:0]	**Port 2 Match Value.** Match comparison value used on Port 2 for bits in P2MAT which are set to 1. 0: P2.n pin logic value is compared with logic LOW. 1: P2.n pin logic value is compared with logic HIGH.
Note: Ports 2.2-P2.7 only available on 32-pin packages.		

SFR Definition 18.23. P2SKIP: Port 2 Skip

Bit	7	6	5	4	3	2	1	0
Name	P2SKIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD6; SFR Page = 0x0F

Bit	Name	Function
7:0	P2SKIP[7:0]	**Port 2 Crossbar Skip Enable Bits.** These bits select Port 2 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar. 0: Corresponding P2.n pin is not skipped by the Crossbar. 1: Corresponding P2.n pin is skipped by the Crossbar.
Note: P2.2-P2.7 are only available on the 32-pin packages.		

SFR Definition 18.24. P3: Port 3

Bit	7	6	5	4	3	2	1	0
Name								P3
Type	R	R	R	R	R	R	R	R/W
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xB0; SFR Page = All Pages; Bit-Addressable

Bit	Name	Description	Write	Read
7:1	Unused	Read = 0000000b; Write = Don't Care.		
0	P3[0]	**Port 3 Data.** Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P3.n Port pin is logic LOW. 1: P3.n Port pin is logic HIGH.
Note: Port P3.0 is only available on the 32-pin packages.				

LIN Register Definition 19.7. LIN0ERR: LIN0 Error Register

Bit	7	6	5	4	3	2	1	0
Name				SYNCH	PRTY	TOUT	CHK	BITERR
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Indirect Address = 0x0A

Bit	Name	Function
7:5	Unused	Read = 000b; Write = Don't Care
4	SYNCH	**Synchronization Error Bit (slave mode only).** 0: No error with the SYNCH FIELD has been detected. 1: Edges of the SYNCH FIELD are outside of the maximum tolerance.
3	PRTY	**Parity Error Bit (slave mode only).** 0: No parity error has been detected. 1: A parity error has been detected.
2	TOUT	**Timeout Error Bit.** 0: A timeout error has not been detected. 1: A timeout error has been detected. This error is detected whenever one of the following conditions is met: • The master is expecting data from a slave and the slave does not respond. • The slave is expecting data but no data is transmitted on the bus. • A frame is not finished within the maximum frame length. • The application does not set the DTACK bit (LIN0CTRL.4) or STOP bit (LIN0CTRL.7) until the end of the reception of the first byte after the identifier.
1	CHK	**Checksum Error Bit.** 0: Checksum error has not been detected. 1: Checksum error has been detected.
0	BITERR	**Bit Transmission Error Bit.** 0: No error in transmission has been detected. 1: The bit value monitored during transmission is different than the bit value sent.

1. Clear RI0 to 0.
2. Read SBUF0.
3. Check RI0, and repeat at step 1 if RI0 is set to 1.

If the extra bit function is enabled (XBE0 = 1) and the parity function is disabled (PE0 = 0), the extra bit for the oldest byte in the FIFO can be read from the RBX0 bit (SCON0.2). If the extra bit function is not enabled, the value of the stop bit for the oldest FIFO byte will be presented in RBX0. When the parity function is enabled (PE0 = 1), hardware will check the received parity bit against the selected parity type (selected with S0PT[1:0]) when receiving data. If a byte with parity error is received, the PERR0 flag will be set to 1. This flag must be cleared by software. Note: when parity is enabled, the extra bit function is not available.

21.3.3. Multiprocessor Communications

UART0 supports multiprocessor communication between a master processor and one or more slave processors by special use of the extra data bit. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its extra bit is logic 1; in a data byte, the extra bit is always set to logic 0.

Setting the MCE0 bit (SMOD0.7) of a slave processor configures its UART such that when a stop bit is received, the UART will generate an interrupt only if the extra bit is logic 1 (RBX0 = 1) signifying an address byte has been received. In the UART interrupt handler, software will compare the received address with the slave's own assigned address. If the addresses match, the slave will clear its MCE0 bit to enable interrupts on the reception of the following data byte(s). Slaves that weren't addressed leave their MCE0 bits set and do not generate interrupts on the reception of the following data bytes, thereby ignoring the data. Once the entire message is received, the addressed slave resets its MCE0 bit to ignore all transmissions until it receives the next address byte.

Multiple addresses can be assigned to a single slave and/or a single address can be assigned to multiple slaves, thereby enabling "broadcast" transmissions to more than one slave simultaneously. The master processor can be configured to receive all transmissions or a protocol can be implemented such that the master/slave role is temporarily reversed to enable half-duplex transmission between the original master and slave(s).

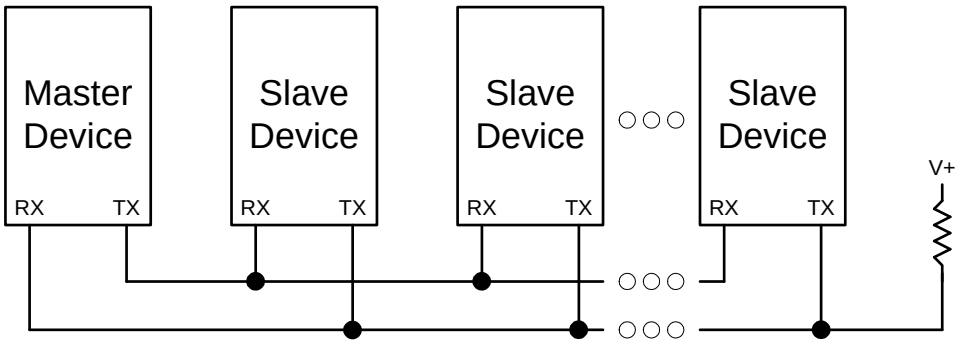


Figure 21.6. UART Multi-Processor Mode Interconnect Diagram

24. Programmable Counter Array

The Programmable Counter Array (PCA0) provides enhanced timer functionality while requiring less CPU intervention than the standard 8051 counter/timers. The PCA consists of a dedicated 16-bit counter/timer and six 16-bit capture/compare modules. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the Crossbar to Port I/O when enabled. The counter/timer is driven by a programmable timebase that can select between six sources: system clock, system clock divided by four, system clock divided by twelve, the external oscillator clock source divided by 8, Timer 0 overflows, or an external clock signal on the ECI input pin. Each capture/compare module may be configured to operate independently in one of six modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, 8 to 11-Bit PWM, or 16-Bit PWM (each mode is described in Section “24.3. Capture/Compare Modules” on page 252). The external oscillator clock option is ideal for real-time clock (RTC) functionality, allowing the PCA to be clocked by a precision external oscillator while the internal oscillator drives the system clock. The PCA is configured and controlled through the system controller's Special Function Registers. The PCA block diagram is shown in Figure 24.1

Important Note: The PCA Module 5 may be used as a watchdog timer (WDT), and is enabled in this mode following a system reset. **Access to certain PCA registers is restricted while WDT mode is enabled**. See Section 24.4 for details.

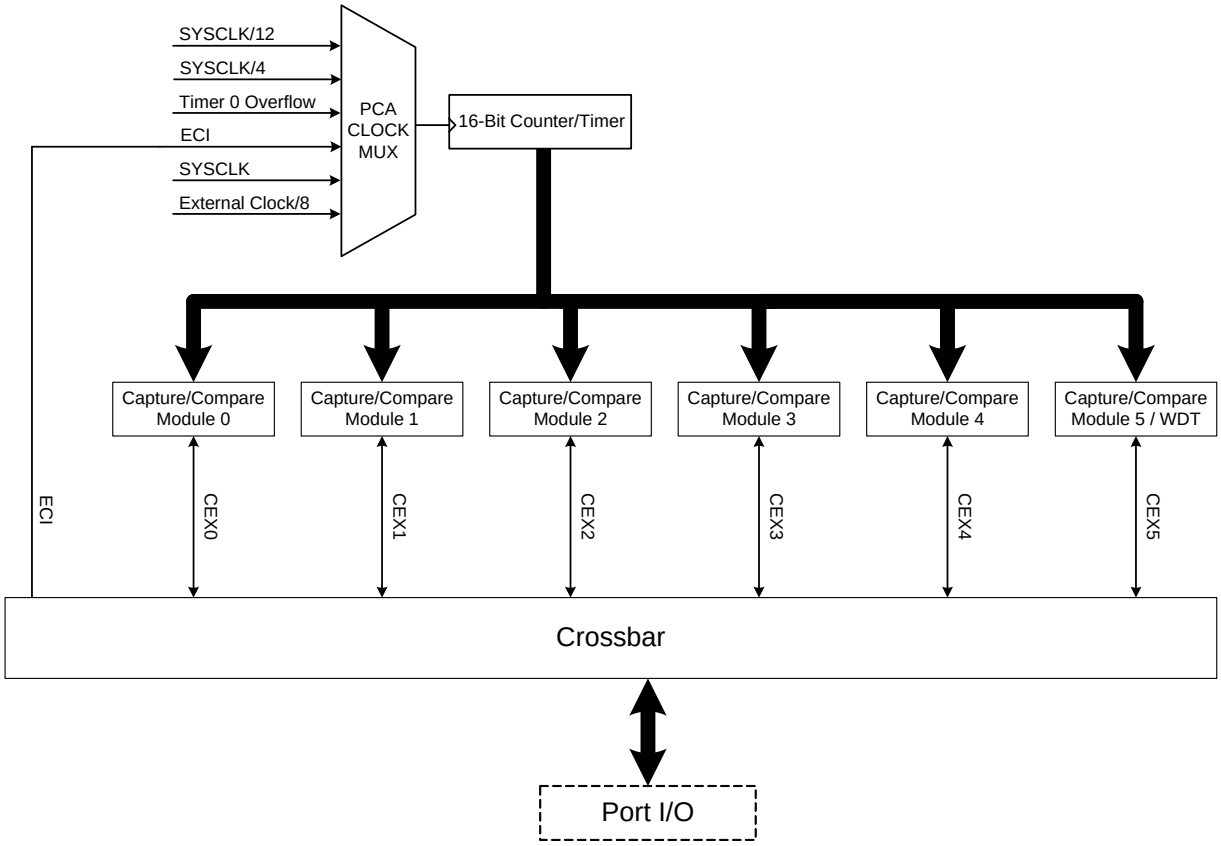


Figure 24.1. PCA Block Diagram

SFR Definition 24.2. PCA0MD: PCA Mode

Bit	7	6	5	4	3	2	1	0
Name	CIDL	WDTE	WDLCK		CPS[2:0]			ECF
Type	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

SFR Address = 0xD9; SFR Page = 0x00

Bit	Name	Function
7	CIDL	**PCA Counter/Timer Idle Control.** Specifies PCA behavior when CPU is in Idle Mode. 0: PCA continues to function normally while the system controller is in Idle Mode. 1: PCA operation is suspended while the system controller is in Idle Mode.
6	WDTE	**Watchdog Timer Enable** If this bit is set, PCA Module 5 is used as the watchdog timer. 0: Watchdog Timer disabled. 1: PCA Module 5 enabled as Watchdog Timer.
5	WDLCK	**Watchdog Timer Lock** This bit locks/unlocks the Watchdog Timer Enable. When WDLCK is set, the Watchdog Timer may not be disabled until the next system reset. 0: Watchdog Timer Enable unlocked. 1: Watchdog Timer Enable locked.
4	Unused	Read = 0b, Write = Don't care.
3:1	CPS[2:0]	**PCA Counter/Timer Pulse Select.** These bits select the timebase source for the PCA counter 000: System clock divided by 12 001: System clock divided by 4 010: Timer 0 overflow 011: High-to-low transitions on ECI (max rate = system clock divided by 4) 100: System clock 101: External clock divided by 8 (synchronized with the system clock) 11x: Reserved
0	ECF	**PCA Counter/Timer Overflow Interrupt Enable.** This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt. 0: Disable the CF interrupt. 1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.
Note: When the WDTE bit is set to 1, the other bits in the PCA0MD register cannot be modified. To change the contents of the PCA0MD register, the Watchdog Timer must first be disabled.		

SFR Definition 24.7. PCA0CPLn: PCA Capture Module Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0CPn[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: PCA0CPL0 = 0xFB, PCA0CPL1 = 0xE9, PCA0CPL2 = 0xEB, PCA0CPL3 = 0xED, PCA0CPL4 = 0xFD, PCA0CPL5 = 0xCE; SFR Page (all registers) = 0x00

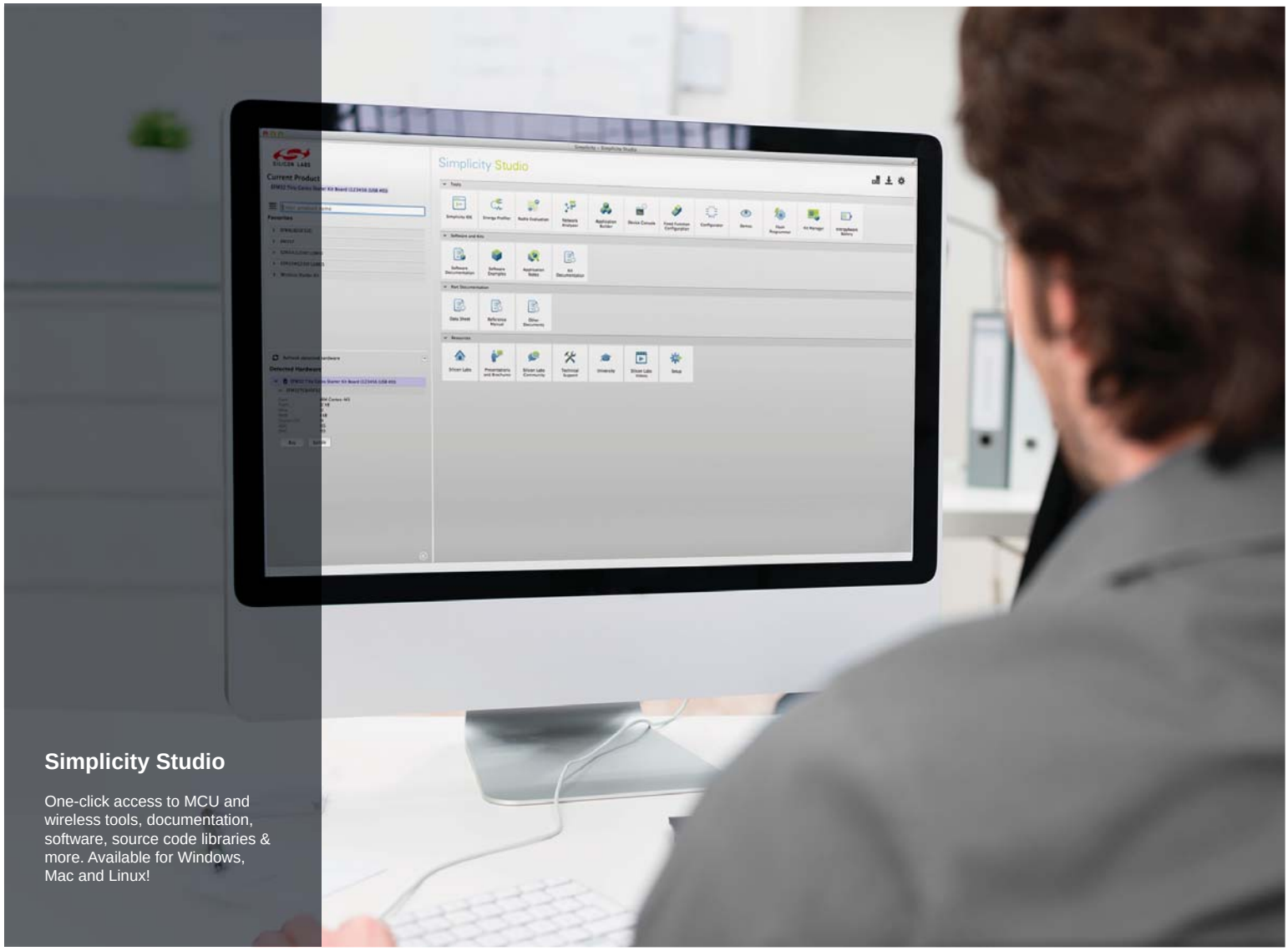
Bit	Name	Function
7:0	PCA0CPn[7:0]	**PCA Capture Module Low Byte.** The PCA0CPLn register holds the low byte (LSB) of the 16-bit capture module n. This register address also allows access to the low byte of the corresponding PCA channel's auto-reload value for 9, 10, or 11-bit PWM mode. The ARSEL bit in register PCA0PWM controls which register is accessed.
Note: A write to this register will clear the module's ECOMn bit to a 0.		

SFR Definition 24.8. PCA0CPHn: PCA Capture Module High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0CPn[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: PCA0CPH0 = 0xFC, PCA0CPH1 = 0xEA, PCA0CPH2 = 0xEC, PCA0CPH3 = 0xEE, PCA0CPH4 = 0xFE, PCA0CPH5 = 0xCF; SFR Page (all registers) = 0x00

Bit	Name	Function
7:0	PCA0CPn[15:8]	**PCA Capture Module High Byte.** The PCA0CPHn register holds the high byte (MSB) of the 16-bit capture module n. This register address also allows access to the high byte of the corresponding PCA channel's auto-reload value for 9, 10, or 11-bit PWM mode. The ARSEL bit in register PCA0PWM controls which register is accessed.
Note: A write to this register will set the module's ECOMn bit to a 1.		



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