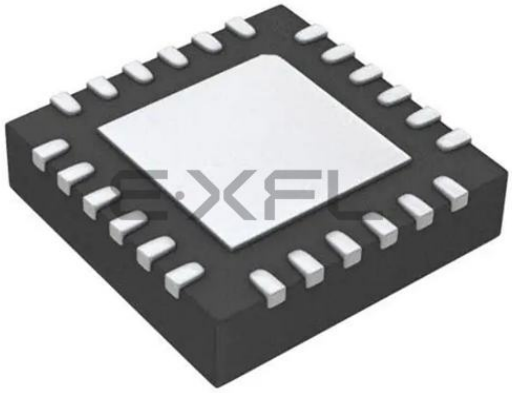

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), LINbus, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 18x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f546-imr

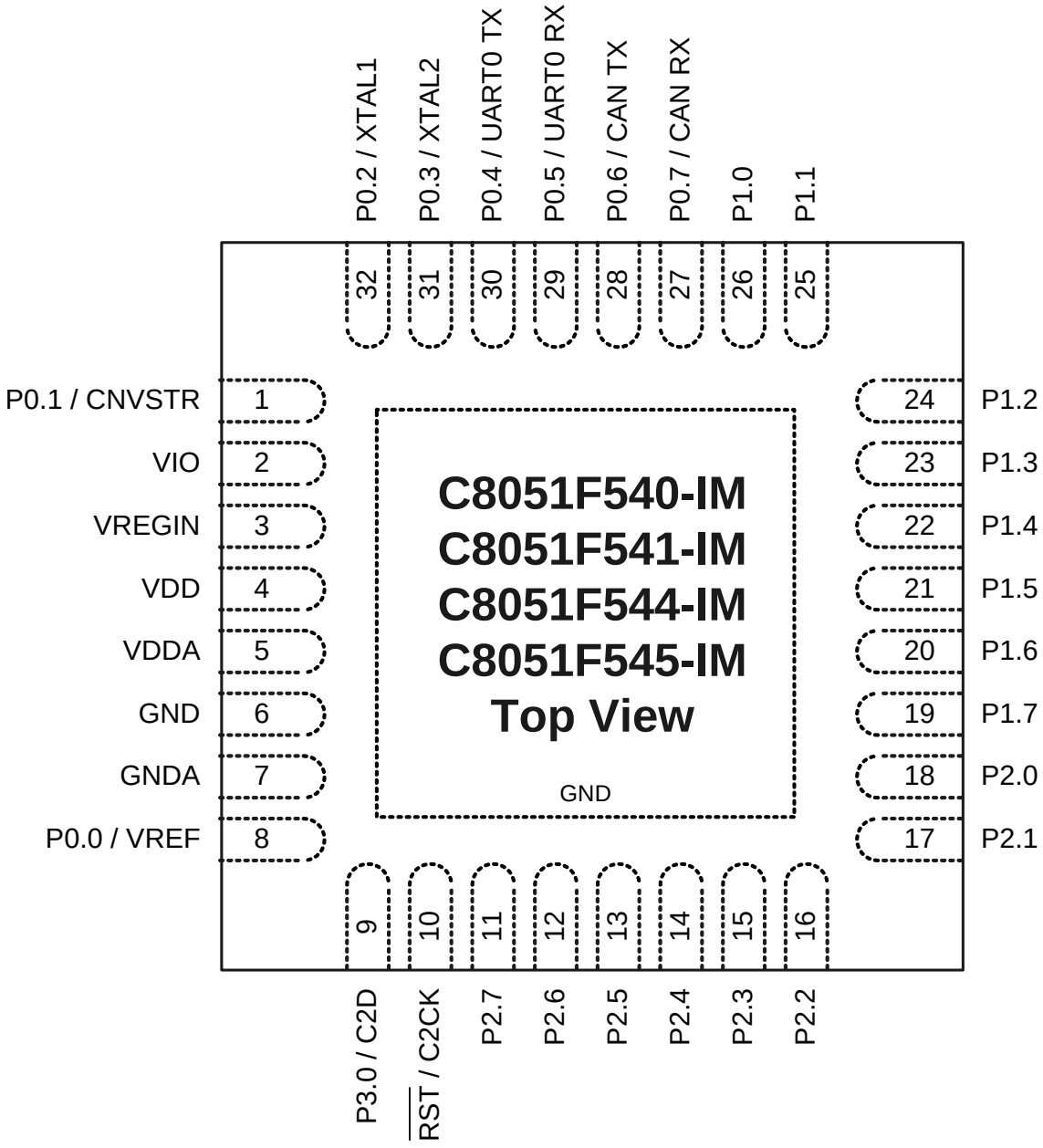

Figure 3.2. QFN-32 Pinout Diagram (Top View)

4.3. QFN-24 Package Specifications

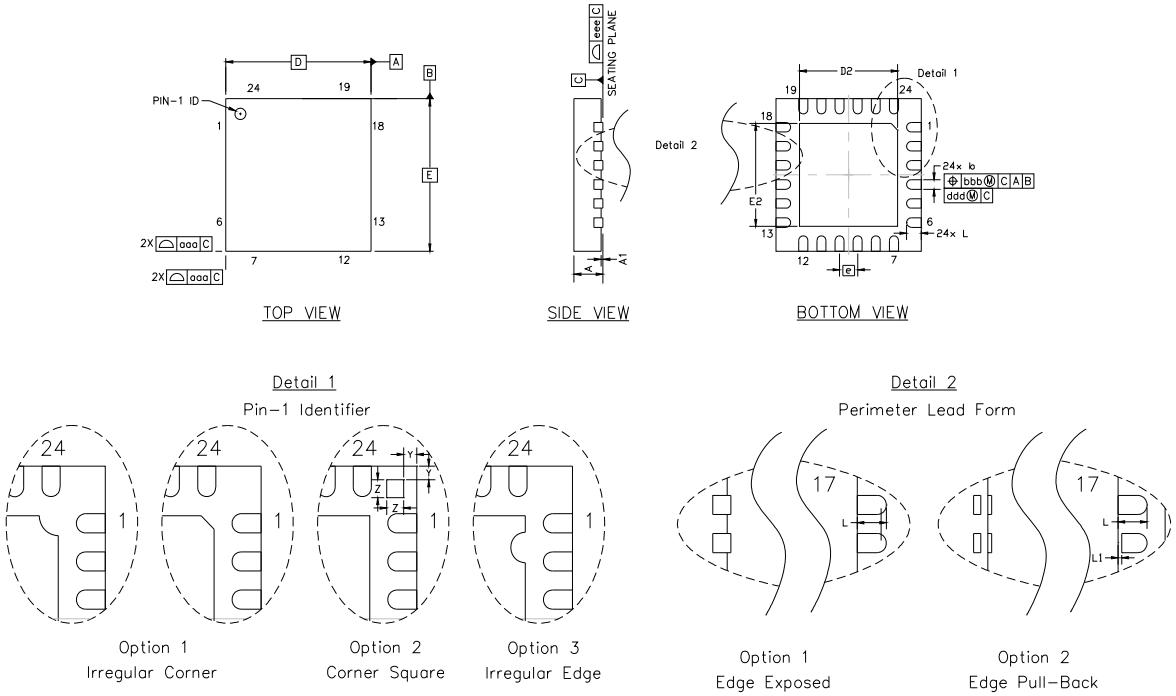

Figure 4.5. QFN-24 Package Drawing

Table 4.5. QFN-24 Package Dimensions

Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.70	0.75	0.80	L	0.30	0.40	0.50
A1	0.00	0.02	0.05	L1	0.00		0.15
b	0.18	0.25	0.30	aaa			0.15
D	4.00 BSC			bbb			0.10
D2	2.55	2.70	2.80	ddd			0.05
e	0.50 BSC			eee			0.08
E	4.00 BSC			Z		0.24	
E2	2.55	2.70	2.80	Y		0.18	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD, except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

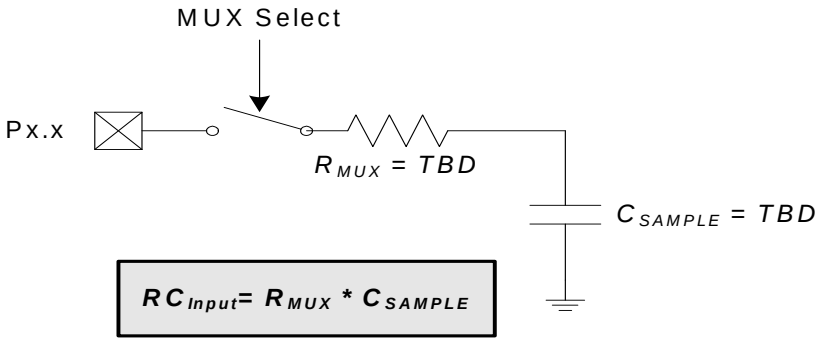

Figure 5.5. ADC0 Equivalent Input Circuit

5.3. Selectable Gain

ADC0 on the C8051F54x family of devices implements a selectable gain adjustment option. By writing a value to the gain adjust address range, the user can select gain values between 0 and 1.016.

For example, three analog sources to be measured have full-scale outputs of 5.0 V, 4.0 V, and 3.0 V, respectively. Each ADC measurement would ideally use the full dynamic range of the ADC with an internal voltage reference of 1.5 V or 2.2 V (set to 2.2 V for this example). When selecting the first source (5.0 V full-scale), a gain value of 0.44 (5 V full scale x 0.44 = 2.2 V full scale) provides a full-scale signal of 2.2 V when the input signal is 5.0 V. Likewise, a gain value of 0.55 (4 V full scale x 0.55 = 2.2 V full scale) for the second source and 0.73 (3 V full scale x 0.73 = 2.2 V full scale) for the third source provide full-scale ADC0 measurements when the input signal is full-scale.

Additionally, some sensors or other input sources have small part-to-part variations that must be accounted for to achieve accurate results. In this case, the programmable gain value could be used as a calibration value to eliminate these part-to-part variations.

5.3.1. Calculating the Gain Value

The ADC0 selectable gain feature is controlled by 13 bits in three registers. ADC0GNH contains the 8 upper bits of the gain value and ADC0GNL contains the 4 lower bits of the gain value. The final GAINADD bit (ADC0GNA.0) controls an optional extra 1/64 (0.016) of gain that can be added in addition to the ADC0GNH and ADC0GNL gain. The ADC0GNA.0 bit is set to 1 after a power-on reset.

The equivalent gain for the ADC0GNH, ADC0GNL and ADC0GNA registers is as follows:

$$gain = \left(\frac{GAIN}{4096}\right) + GAINADD \times \left(\frac{1}{64}\right)$$

Equation 5.2. Equivalent Gain from the ADC0GNH and ADC0GNL Registers

Where:
GAIN is the 12-bit word of ADC0GNH[7:0] and ADC0GNL[7:4]
GAINADD is the value of the GAINADD bit (ADC0GNA.0)

gain is the equivalent gain value from 0 to 1.016

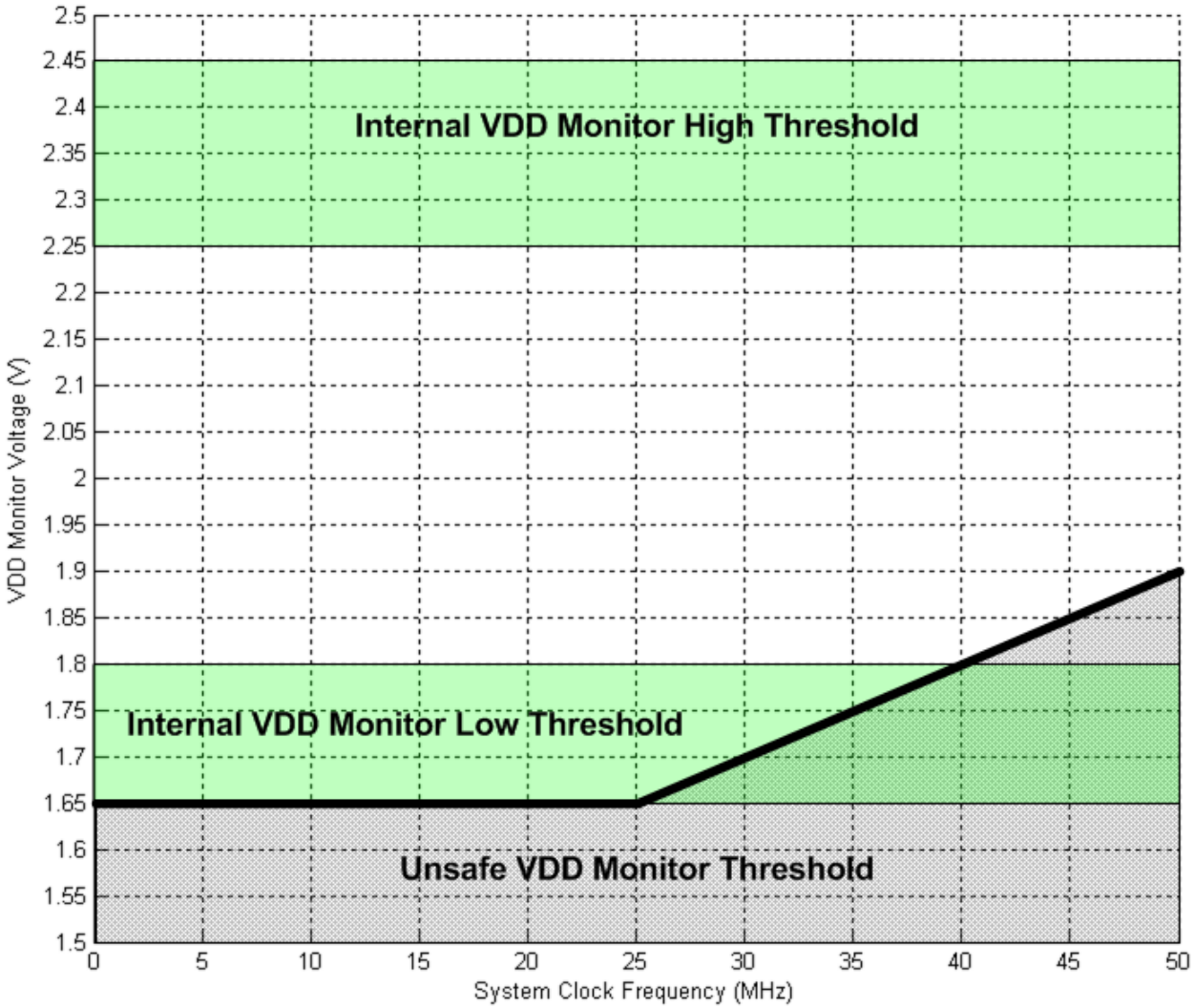

Figure 6.1. Minimum VDD Monitor Threshold vs. System Clock Frequency

Note: With system clock frequencies greater than 25 MHz, the V_{DD} monitor level should be set to the high threshold (VDMLVL = 1b in SFR VDM0CN) to prevent undefined CPU operation. The high threshold should only be used with an external regulator powering V_{DD} directly. See Figure 9.2 on page 73 for the recommended power supply connections.

Table 6.10. Temperature Sensor Electrical Characteristics

VDDA = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Linearity		—	±0.1	—	°C
Slope		—	3.33	—	mV/°C
Slope Error*		—	88	—	µV/°C
Offset	Temp = 0 °C	—	856	—	mV
Offset Error*	Temp = 0 °C	—	±14	—	mV
Power Supply Current		—	18	—	µA
Tracking Time		12	—	—	µs
***Note:** Represents one standard deviation from the mean.					

Table 6.11. Voltage Reference Electrical Characteristics

VDDA = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Internal Reference (REFBE = 1)					
Output Voltage	25 °C ambient (REFLV = 0)	1.45	1.50	1.55	V
	25 °C ambient (REFLV = 1), V_{DD} = 2.6 V	2.15	2.20	2.25	
VREF Short-Circuit Current		—	5	10	mA
VREF Temperature Coefficient		—	38	—	ppm/°C
Power Consumption	Internal	—	30	50	µA
Load Regulation	Load = 0 to 200 µA to AGND	—	3	—	µV/µA
VREF Turn-on Time 1	4.7 µF tantalum and 0.1 µF bypass	—	1.5	—	ms
VREF Turn-on Time 2	0.1 µF bypass	—	46	—	µs
Power Supply Rejection		—	1.2	—	mV/V
External Reference (REFBE = 0)					
Input Voltage Range		1.5	—	V_{DDA}	V
Input Current	Sample Rate = 200 ksps; VREF = 1.5 V	—	2.1	—	µA
Power Specifications					
Reference Bias Generator	REFBE = 1 or TEMPE = 1	—	21	40	µA

SFR Definition 8.3. CPT1CN: Comparator1 Control

Bit	7	6	5	4	3	2	1	0
Name	CP1EN	CP1OUT	CP1RIF	CP1FIF	CP1HYP[1:0]		CP1HYN[1:0]	
Type	R/W	R	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x9D; SFR Page = 0x00

Bit	Name	Function
7	CP1EN	**Comparator1 Enable Bit.** 0: Comparator1 Disabled. 1: Comparator1 Enabled.
6	CP1OUT	**Comparator1 Output State Flag.** 0: Voltage on CP1+ < CP1–. 1: Voltage on CP1+ > CP1–.
5	CP1RIF	**Comparator1 Rising-Edge Flag. Must be cleared by software.** 0: No Comparator1 Rising Edge has occurred since this flag was last cleared. 1: Comparator1 Rising Edge has occurred.
4	CP1FIF	**Comparator1 Falling-Edge Flag. Must be cleared by software.** 0: No Comparator1 Falling-Edge has occurred since this flag was last cleared. 1: Comparator1 Falling-Edge has occurred.
3:2	CP1HYP[1:0]	**Comparator1 Positive Hysteresis Control Bits.** 00: Positive Hysteresis Disabled. 01: Positive Hysteresis = 5 mV. 10: Positive Hysteresis = 10 mV. 11: Positive Hysteresis = 20 mV.
1:0	CP1HYN[1:0]	**Comparator1 Negative Hysteresis Control Bits.** 00: Negative Hysteresis Disabled. 01: Negative Hysteresis = 5 mV. 10: Negative Hysteresis = 10 mV. 11: Negative Hysteresis = 20 mV.

Table 10.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement Carry	1	1
CPL bit	Complement direct bit	2	2
ANL C, bit	AND direct bit to Carry	2	2
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2
JC rel	Jump if Carry is set	2	2/3*
JNC rel	Jump if Carry is not set	2	2/3*
JB bit, rel	Jump if direct bit is set	3	3/4*
JNB bit, rel	Jump if direct bit is not set	3	3/4*
JBC bit, rel	Jump if direct bit is set and clear bit	3	3/4*
Program Branching			
ACALL addr11	Absolute subroutine call	2	3*
LCALL addr16	Long subroutine call	3	4*
RET	Return from subroutine	1	5*
RETI	Return from interrupt	1	5*
AJMP addr11	Absolute jump	2	3*
LJMP addr16	Long jump	3	4*
SJMP rel	Short jump (relative address)	2	3*
JMP @A+DPTR	Jump indirect relative to DPTR	1	3*
JZ rel	Jump if A equals zero	2	2/3*
JNZ rel	Jump if A does not equal zero	2	2/3
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	4/5*
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/4*
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/4*
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/5*
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/3*
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/4*
NOP	No operation	1	1

Note: Certain instructions take a variable number of clock cycles to execute depending on instruction alignment and the FLRT setting (SFR Definition 14.3).

Table 12.2. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
ACC	0xE0	Accumulator	82
ADC0CF	0xBC	ADC0 Configuration	40
ADC0CN	0xE8	ADC0 Control	42
ADC0GTH	0xC4	ADC0 Greater-Than Compare High	44
ADC0GTL	0xC3	ADC0 Greater-Than Compare Low	44
ADC0H	0xBE	ADC0 High	41
ADC0L	0xBD	ADC0 Low	41
ADC0LTH	0xC6	ADC0 Less-Than Compare Word High	45
ADC0LTL	0xC5	ADC0 Less-Than Compare Word Low	45
ADC0MX	0xBB	ADC0 Mux Configuration	59
ADC0TK	0xBA	ADC0 Tracking Mode Select	43
B	0xF0	B Register	82
CCH0CN	0xE3	Cache Control	125
CKCON	0x8E	Clock Control	228
CLKMUL	0x97	Clock Multiplier	141
CLKSEL	0x8F	Clock Select	136
CPT0CN	0x9A	Comparator0 Control	65
CPT0MD	0x9B	Comparator0 Mode Selection	66
CPT0MX	0x9C	Comparator0 MUX Selection	70
CPT1CN	0x9D	Comparator1 Control	65
CPT1MD	0x9E	Comparator1 Mode Selection	66
CPT1MX	0x9F	Comparator1 MUX Selection	70
DPH	0x83	Data Pointer High	81
DPL	0x82	Data Pointer Low	81
EIE1	0xE6	Extended Interrupt Enable 1	111
EIE2	0xE7	Extended Interrupt Enable 2	111
EIP1	0xF6	Extended Interrupt Priority 1	112
EIP2	0xF7	Extended Interrupt Priority 2	113
EMI0CN	0xAA	External Memory Interface Control	88
FLKEY	0xB7	Flash Lock and Key	123
FLSCL	0xB6	Flash Scale	124
IE	0xA8	Interrupt Enable	109
IP	0xB8	Interrupt Priority	110
IT01CF	0xE4	INT0/INT1 Configuration	116
LIN0ADR	0xD3	LIN0 Address	177

13.2. Interrupt Register Descriptions

The SFRs used to enable the interrupt sources and set their priority level are described in this section. Refer to the data sheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

The level of Flash security depends on the Flash access method. The three Flash access methods that can be restricted are reads, writes, and erases from the C2 debug interface, user firmware executing on unlocked pages, and user firmware executing on locked pages. Table 14.1 summarizes the Flash security features of the C8051F54x devices.

Table 14.1. Flash Security Summary

Action	C2 Debug Interface	User Firmware executing from:	
		an unlocked page	a locked page
Read, Write or Erase unlocked pages (except page with Lock Byte)	Permitted	Permitted	Permitted
Read, Write or Erase locked pages (except page with Lock Byte)	Not Permitted	Flash Error Reset	Permitted
Read or Write page containing Lock Byte (if no pages are locked)	Permitted	Permitted	Permitted
Read or Write page containing Lock Byte (if any page is locked)	Not Permitted	Flash Error Reset	Permitted
Read contents of Lock Byte (if no pages are locked)	Permitted	Permitted	Permitted
Read contents of Lock Byte (if any page is locked)	Not Permitted	Flash Error Reset	Permitted
Erase page containing Lock Byte (if no pages are locked)	Permitted	Flash Error Reset	Flash Error Reset
Erase page containing Lock Byte—Unlock all pages (if any page is locked)	C2 Device Erase Only	Flash Error Reset	Flash Error Reset
Lock additional pages (change 1s to 0s in the Lock Byte)	Not Permitted	Flash Error Reset	Flash Error Reset
Unlock individual pages (change 0s to 1s in the Lock Byte)	Not Permitted	Flash Error Reset	Flash Error Reset
Read, Write or Erase Reserved Area	Not Permitted	See note	See note

Note: Flash Reads will return indeterminate data. Flash Writes and Erases are ignored.

C2 Device Erase—Erases all Flash pages including the page containing the Lock Byte.

Flash Error Reset—Not permitted; Causes Flash Error Device Reset (FERROR bit in RSTSRC is 1 after reset).

- All prohibited operations that are performed via the C2 interface are ignored (do not cause device reset).
- Locking any Flash page also locks the page containing the Lock Byte.
- Once written to, the Lock Byte cannot be modified except by performing a C2 Device Erase.
- If user code writes to the Lock Byte, the Lock does not take effect until the next device reset.

14.4.3. System Clock

1. If operating from an external crystal, be advised that crystal performance is susceptible to electrical interference and is sensitive to layout and to changes in temperature. If the system is operating in an electrically noisy environment, use the internal oscillator or use an external CMOS clock.
2. If operating from the external oscillator, switch to the internal oscillator during Flash write or erase operations. The external oscillator can continue to run, and the CPU can switch back to the external oscillator after the Flash operation has completed.

Additional Flash recommendations and example code can be found in ”AN201: Writing to Flash from Firmware" available from the Silicon Laboratories web site.

SFR Definition 14.1. PSCTL: Program Store R/W Control

Bit	7	6	5	4	3	2	1	0
Name							PSEE	PSWE
Type	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8F; SFR Page = 0x00

Bit	Name	Function
7:2	Unused	Read = 000000b, Write = don’t care.
1	PSEE	**Program Store Erase Enable.** Setting this bit (in combination with PSWE) allows an entire page of Flash program memory to be erased. If this bit is logic 1 and Flash writes are enabled (PSWE is logic 1), a write to Flash memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter. 0: Flash program memory erasure disabled. 1: Flash program memory erasure enabled.
0	PSWE	**Program Store Write Enable.** Setting this bit allows writing a byte of data to the Flash program memory using the MOVX write instruction. The Flash location should be erased before writing data. 0: Writes to Flash program memory disabled. 1: Writes to Flash program memory enabled; the MOVX write instruction targets Flash memory.

15. Power Management Modes

The C8051F54x devices have three software programmable power management modes: Idle, Stop, and Suspend. Idle mode and Stop mode are part of the standard 8051 architecture, while Suspend mode is an enhanced power-saving mode implemented by the high-speed oscillator peripheral.

Idle mode halts the CPU while leaving the peripherals and clocks active. In Stop mode, the CPU is halted, all interrupts and timers (except the Missing Clock Detector) are inactive, and the internal oscillator is stopped (analog peripherals remain in their selected states; the external oscillator is not affected). Suspend mode is similar to Stop mode in that the internal oscillator and CPU are halted, but the device can wake on events such as a Port Match or Comparator low output. Since clocks are running in Idle mode, power consumption is dependent upon the system clock frequency and the number of peripherals left in active mode before entering Idle. Stop mode and Suspend mode consume the least power because the majority of the device is shut down with no clocks active. SFR Definition 15.1 describes the Power Control Register (PCON) used to control the C8051F54x devices' Stop and Idle power management modes. Suspend mode is controlled by the SUSPEND bit in the OSCICN register (SFR Definition 17.2).

Although the C8051F54x has Idle, Stop, and Suspend modes available, more control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers or serial buses, draw little power when they are not in use. Turning off oscillators lowers power consumption considerably, at the expense of reduced functionality.

15.1. Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the hardware to halt the CPU and enter Idle mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during Idle mode.

Idle mode is terminated when an enabled interrupt is asserted or a reset occurs. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If Idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

Note: If the instruction following the write of the IDLE bit is a single-byte instruction and an interrupt occurs during the execution phase of the instruction that sets the IDLE bit, the CPU may not wake from Idle mode when a future interrupt occurs. Therefore, instructions that set the IDLE bit should be followed by an instruction that has two or more opcode bytes, for example:

```
// in 'C':
PCON |= 0x01;                  // set IDLE bit
PCON = PCON;                   // ... followed by a 3-cycle dummy instruction

; in assembly:
ORL PCON, #01h                 ; set IDLE bit
MOV PCON, PCON                 ; ... followed by a 3-cycle dummy instruction
```

If enabled, the Watchdog Timer (WDT) will eventually cause an internal watchdog reset and thereby terminate the Idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the Idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system. Refer to Section "16.6. PCA Watchdog Timer Reset" on page 133 for more information on the use and configuration of the WDT.

15.2. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the controller core to enter Stop mode as soon as the instruction that sets the bit completes execution. In Stop mode the internal oscillator, CPU, and all digital peripherals are stopped; the state of the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering Stop Mode. Stop mode can only be terminated by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout of 100 µs.

15.3. Suspend Mode

Setting the SUSPEND bit (OSCICN.5) causes the hardware to halt the CPU and the high-frequency internal oscillator, and go into Suspend mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. Most digital peripherals are not active in Suspend mode. The exception to this is the Port Match feature.

Suspend mode can be terminated by three types of events, a port match (described in Section “18.5. Port Match” on page 157), a Comparator low output (if enabled), or a device reset event. When Suspend mode is terminated, the device will continue execution on the instruction following the one that set the SUSPEND bit. If the wake event was configured to generate an interrupt, the interrupt will be serviced upon waking the device. If Suspend mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

Note: When entering Suspend mode, firmware must set the ZTCEN bit in REF0CN (SFR Definition 7.1).

16.1. Power-On Reset

During power-up, the device is held in a reset state and the $\overline{RST}$ pin is driven low until V_{DD} settles above V_{RST}. A delay occurs before the device is released from reset; the delay decreases as the V_{DD} ramp time increases (V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST}). Figure 16.2. plots the power-on and V_{DD} monitor reset timing.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000) software can read the PORSF flag to determine if a power-up was the cause of reset. The content of internal data memory should be assumed to be undefined after a power-on reset. The V_{DD} monitor is enabled following a power-on reset.

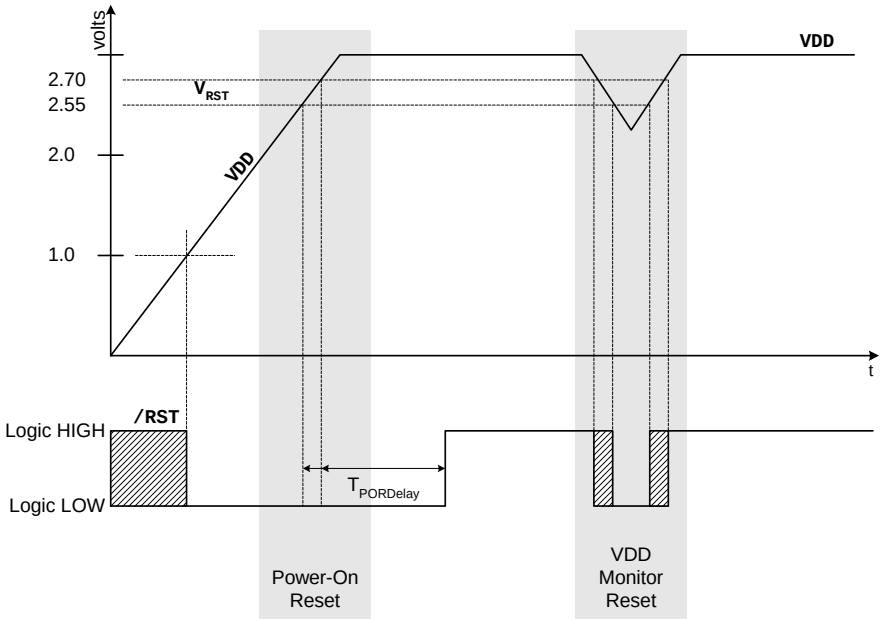

Figure 16.2. Power-On and V_{DD} Monitor Reset Timing

16.2. Power-Fail Reset/V_{DD} Monitor

When a power-down transition or power irregularity causes V_{DD} to drop below V_{RST}, the power supply monitor will drive the $\overline{RST}$ pin low and hold the CIP-51 in a reset state (see Figure 16.2). When V_{DD} returns to a level above V_{RST}, the CIP-51 will be released from the reset state. Note that even though internal data memory contents are not altered by the power-fail reset, it is impossible to determine if V_{DD} dropped below the level required for data retention. If the PORSF flag reads 1, the data may no longer be valid. The V_{DD} monitor is enabled after power-on resets. Its defined state (enabled/disabled) is not altered by any other reset source. For example, if the V_{DD} monitor is disabled by code and a software reset is performed, the V_{DD} monitor will still be disabled after the reset. **To protect the integrity of Flash contents, the V_{DD} monitor must be enabled to the higher setting (VDMLVL = 1) and selected as a reset source if software contains routines which erase or write Flash memory. If the V_{DD} monitor is not enabled and set to the high level, any erase or write performed on Flash memory will cause a Flash Error device reset.**

18.1.3. Interfacing Port I/O in a Multi-Voltage System

All Port I/O are capable of interfacing to digital logic operating at a supply voltage higher than V_{DD} and less than 5.25 V. Connect the V_{IO} pin to the voltage source of the interface logic.

18.2. Assigning Port I/O Pins to Analog and Digital Functions

Port I/O pins P0.0–P3.0 can be assigned to various analog, digital, and external interrupt functions. The Port pins assigned to analog functions should be configured for analog I/O, and Port pins assigned to digital or external interrupt functions should be configured for digital I/O.

18.2.1. Assigning Port I/O Pins to Analog Functions

Table 18.1 shows all available analog functions that require Port I/O assignments. **Port pins selected for these analog functions should have their corresponding bit in PnSKIP set to 1.** This reserves the pin for use by the analog function and does not allow it to be claimed by the Crossbar. Table 18.1 shows the potential mapping of Port I/O to each analog function.

Table 18.1. Port I/O Assignment for Analog Functions

Analog Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
ADC Input	P0.0–P3.0*	ADC0MX, PnSKIP
Comparator0 or Compartor1 Input	P0.0–P2.7*	CPT0MX, CPT1MX, PnSKIP
Voltage Reference (VREF0)	P0.0	REF0CN, PnSKIP
External Oscillator in Crystal Mode (XTAL1)	P0.2	OSCXCN, PnSKIP
External Oscillator in RC, C, or Crystal Mode (XTAL2)	P0.3	OSCXCN, PnSKIP
***Note:** P2.2-P2.7, P3.0 are only available on the 32-pin packages		

18.2.2. Assigning Port I/O Pins to Digital Functions

Any Port pins not assigned to analog functions may be assigned to digital functions or used as GPIO. Most digital functions rely on the Crossbar for pin assignment; however, some digital functions bypass the Crossbar in a manner similar to the analog functions listed above. **Port pins used by these digital functions and any Port pins selected for use as GPIO should have their corresponding bit in PnSKIP set to 1.** Table 18.2 shows all available digital functions and the potential mapping of Port I/O to each digital function.

Table 18.2. Port I/O Assignment for Digital Functions

Digital Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
UART0, SPI0, SMBus, LIN0, CP0, CP0A, CP1, CP1A, SYSCLK, PCA0 (CEX0-5 and ECI), T0 or T1.	Any Port pin available for assignment by the Crossbar. This includes P0.0–P3.0* pins which have their PnSKIP bit set to 0. **Note:** The Crossbar will always assign UART0 pins to P0.4 and P0.5.	XBR0, XBR1, XBR2
***Note:** P2.2-P2.7, P3.0 are only available on the 32-pin packages.		

19.7.2. LIN Indirect Access SFR Registers Definitions

Table 19.4 lists the 15 indirect registers used to configured and communicate with the LIN controller.

Table 19.4. LIN Registers* (Indirectly Addressable)

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LIN0DT1	0x00	DATA1[7:0]							
LIN0DT2	0x01	DATA2[7:0]							
LIN0DT3	0x02	DATA3[7:0]							
LIN0DT4	0x03	DATA4[7:0]							
LIN0DT5	0x04	DATA5[7:0]							
LIN0DT6	0x05	DATA67:0]							
LIN0DT7	0x06	DATA7[7:0]							
LIN0DT8	0x07	DATA8[7:0]							
LIN0CTRL	0x08	STOP(s)	SLEEP(s)	TXRX	DTACK(s)	RSTINT	RSTERR	WUPREQ	STREQ(m)
LIN0ST	0x09	ACTIVE	IDLTOUT	ABORT(s)	DTREQ(s)	LININT	ERROR	WAKEUP	DONE
LIN0ERR	0x0A				SYNCH(s)	PRTY(s)	TOUT	CHK	BITERR
LIN0SIZE	0x0B	ENHCHK				LINSIZE[3:0]			
LIN0DIV	0x0C	DIVLSB[7:0]							
LIN0MUL	0x0D	PRESCL[1:0]		LINMUL[4:0]					DIV9
LIN0ID	0x0E			ID5	ID4	ID3	ID2	ID1	ID0

***Note:** These registers are used in both master and slave mode. The register bits marked with (m) are accessible only in Master mode while the register bits marked with (s) are accessible only in slave mode. All other registers are accessible in both modes.

21.2. Data Format

UART0 has a number of available options for data formatting. Data transfers begin with a start bit (logic low), followed by the data bits (sent LSB-first), a parity or extra bit (if selected), and end with one or two stop bits (logic high). The data length is variable between 5 and 8 bits. A parity bit can be appended to the data, and automatically generated and detected by hardware for even, odd, mark, or space parity. The stop bit length is selectable between 1 and 2 bit times, and a multi-processor communication mode is available for implementing networked UART buses. All of the data formatting options can be configured using the SMOD0 register, shown in SFR Definition 21.2. Figure 21.2 shows the timing for a UART0 transaction without parity or an extra bit enabled. Figure 21.3 shows the timing for a UART0 transaction with parity enabled (PE0 = 1). Figure 21.4 is an example of a UART0 transaction when the extra bit is enabled (XBE0 = 1). Note that the extra bit feature is not available when parity is enabled, and the second stop bit is only an option for data lengths of 6, 7, or 8 bits.

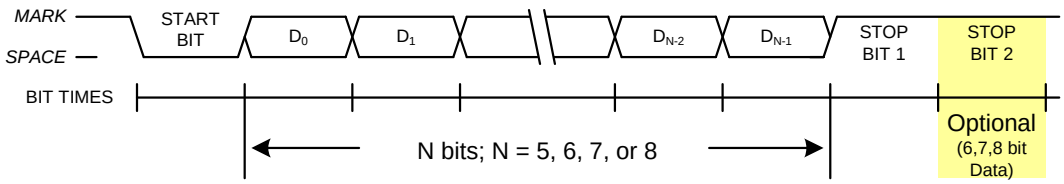

Figure 21.2. UART0 Timing Without Parity or Extra Bit

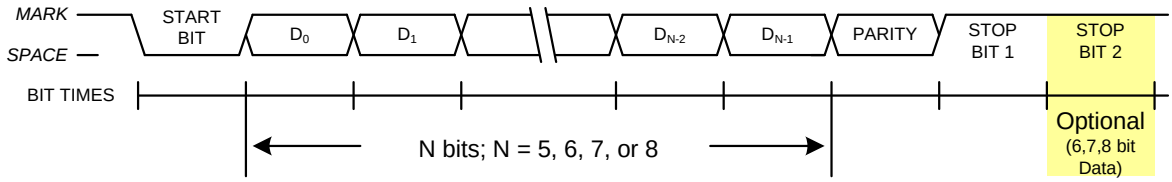

Figure 21.3. UART0 Timing With Parity

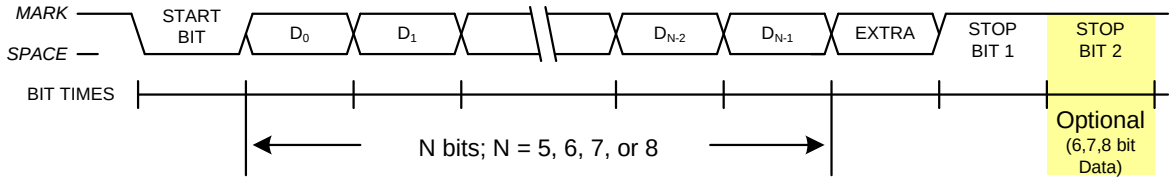

Figure 21.4. UART0 Timing With Extra Bit

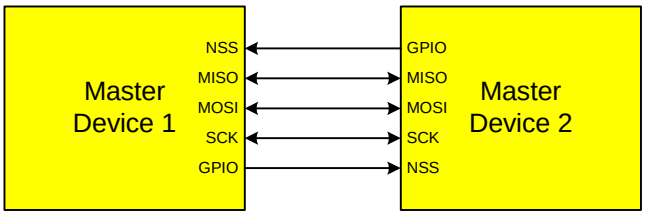

Figure 22.2. Multiple-Master Mode Connection Diagram

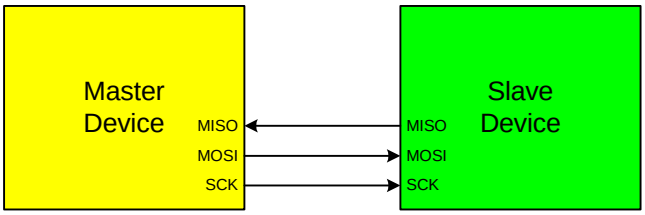

Figure 22.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram

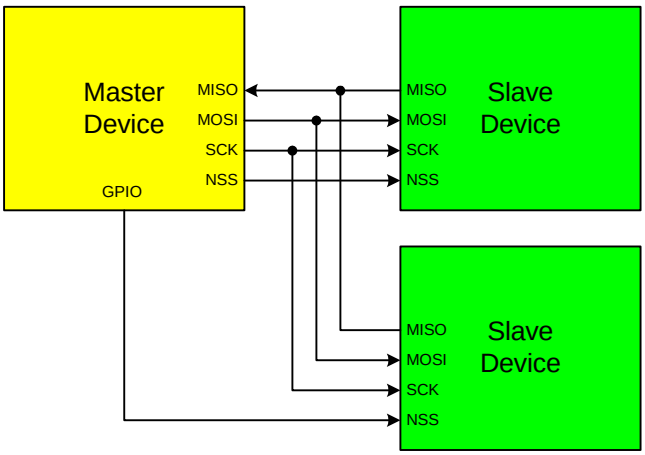

Figure 22.4. 4-Wire Single Master Mode and 4-Wire Slave Mode Connection Diagram

SFR Definition 23.4. TL0: Timer 0 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8A; SFR Page = All Pages

Bit	Name	Function
7:0	TL0[7:0]	**Timer 0 Low Byte.** The TL0 register is the low byte of the 16-bit Timer 0.

SFR Definition 23.5. TL1: Timer 1 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8B; SFR Page = All Pages

Bit	Name	Function
7:0	TL1[7:0]	**Timer 1 Low Byte.** The TL1 register is the low byte of the 16-bit Timer 1.

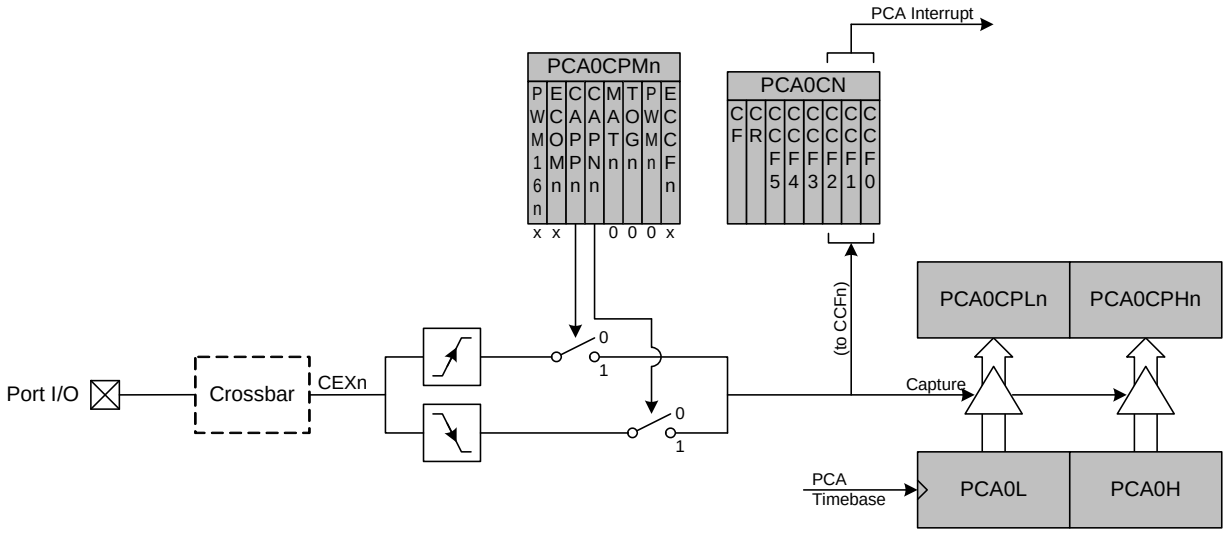

Figure 24.4. PCA Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.

24.3.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.