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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f643abpmc-gse2

- Hardware Watchdog Timer
  - Hardware watchdog timer is active after reset
  - Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval
- Reload Timers
  - 16-bit wide
  - Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
  - Event count function
- Free-Running Timers
  - Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
  - Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency
- Input Capture Units
  - 16-bit wide
  - Signals an interrupt upon external event
  - Rising edge, Falling edge or Both (rising & falling) edges sensitive
- Output Compare Units
  - 16-bit wide
  - Signals an interrupt when a match with Free-running Timer occurs
  - A pair of compare registers can be used to generate an output signal
- Programmable Pulse Generator
  - 16-bit down counter, cycle and duty setting registers
  - Can be used as 2 × 8-bit PPG
  - Interrupt at trigger, counter borrow and/or duty match
  - PWM operation and one-shot operation
  - Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
  - Can be triggered by software or reload timer
  - Can trigger ADC conversion
  - Timing point capture
  - Start delay
- Quadrature Position/Revolution Counter (QPRC)
  - Up/down count mode, Phase difference count mode, Count mode with direction
  - 16-bit position counter
  - 16-bit revolution counter
  - Two 16-bit compare registers with interrupt
  - Detection edge of the three external event input pins AIN, BIN and ZIN is configurable
- Real Time Clock
  - Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
  - Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
  - Read/write accessible second/minute/hour registers
  - Can signal interrupts every half second/second/minute/hour/day
  - Internal clock divider and prescaler provide exact 1s clock
- External Interrupts
  - Edge or Level sensitive
  - Interrupt mask bit per channel
  - Each available CAN channel RX has an external interrupt for wake-up
  - Selected USART channels SIN have an external interrupt for wake-up
- Non Maskable Interrupt
  - Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
  - Once enabled, cannot be disabled other than by reset
  - High or Low level sensitive
  - Pin shared with external interrupt 0
- I/O Ports
  - Most of the external pins can be used as general purpose I/O
  - All push-pull outputs (except when used as I^2C SDA/SCL line)
  - Bit-wise programmable as input/output or peripheral signal
  - Bit-wise programmable input enable
  - One input level per GPIO-pin (either Automotive or CMOS hysteresis)
  - Bit-wise programmable pull-up resistor
- Built-in On Chip Debugger (OCD)
  - One-wire debug tool interface
  - Break function:
    - Hardware break: 6 points (shared with code event)
    - Software break: 4096 points
  - Event function
    - Code event: 6 points (shared with hardware break)
    - Data event: 6 points
    - Event sequencer: 2 levels + reset
  - Execution time measurement function
  - Trace function: 42 branches
  - Security function
- Flash Memory
  - Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
  - Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
  - Supports automatic programming, Embedded Algorithm
  - Write/Erase/Erase-Suspend/Resume commands
  - A flag indicating completion of the automatic algorithm
  - Erase can be performed on each sector individually
  - Sector protection
  - Flash Security feature to protect the content of the Flash
  - Low voltage detection during Flash erases or writes

Contents

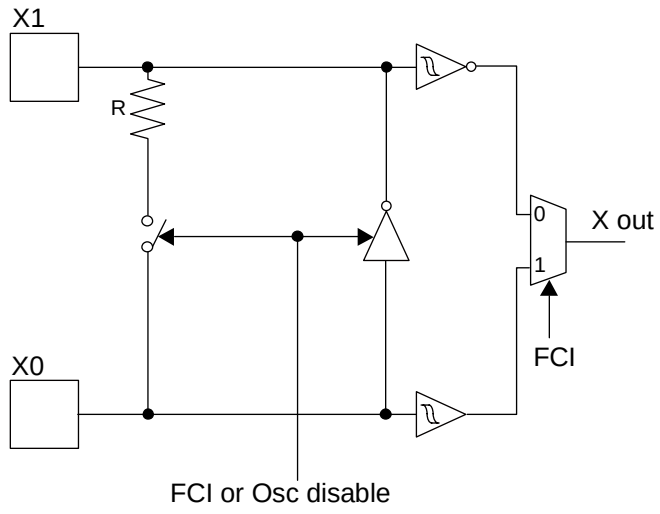
5. Pin Circuit Type

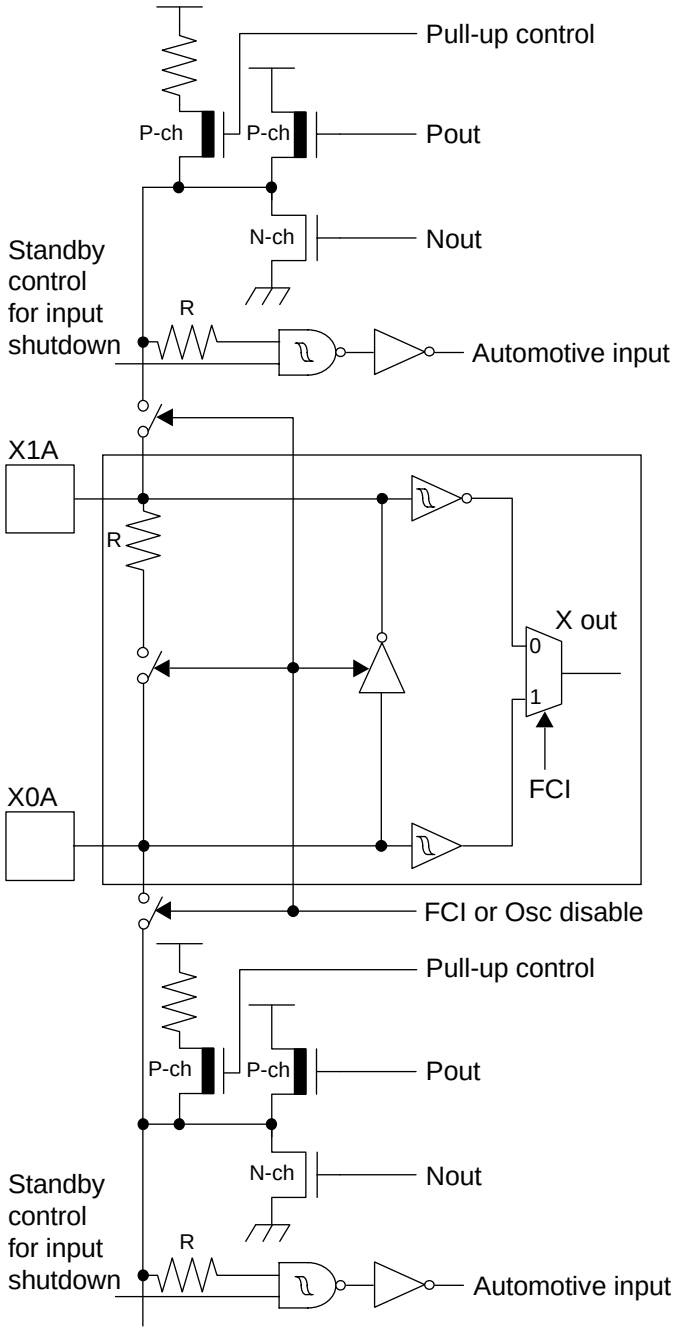
Pin no.	I/O circuit type*	Pin name
1	Supply	Vss
2	F	C
3	M	P03_7 / INT1 / SIN1
4	H	P13_0 / INT2 / SOT1
5	M	P13_1 / INT3 / SCK1
6	H	P13_2 / PPG0 / TIN0 / FRCK1
7	H	P13_3 / PPG1 / TOT0 / WOT
8	M	P13_4 / SIN0 / INT6
9	H	P13_5 / SOT0 / ADTG / INT7
10	M	P13_6 / SCK0 / CKOTX0
11	N	P04_4 / PPG3 / SDA0
12	N	P04_5 / PPG4 / SCL0
13	I	P06_2 / AN2 / INT5 / SIN5
14	K	P06_3 / AN3 / FRCK0
15	K	P06_4 / AN4 / IN0 / TTG0 / TTG4
16	K	P06_6 / AN6 / TIN1 / IN4_R
17	K	P06_7 / AN7 / TOT1 / IN5_R
18	Supply	AVcc
19	G	AVRH
20	G	AVRL
21	Supply	AVss
22	K	P05_0 / AN8
23	K	P05_2 / AN10 / OUT2
24	K	P05_3 / AN11 / OUT3
25	Supply	Vcc
26	Supply	Vss
27	K	P05_4 / AN12 / INT2_R / WOT_R
28	K	P05_6 / AN14 / TIN2
29	K	P05_7 / AN15 / TOT2
30	K	P08_0 / AN16
31	K	P08_1 / AN17
32	K	P08_2 / AN18
33	K	P08_3 / AN19
34	K	P08_4 / AN20 / OUT6
35	N	P04_6 / SDA1
36	N	P04_7 / SCL1
37	K	P08_5 / AN21 / OUT7
38	K	P08_6 / AN22 / PPG6_B

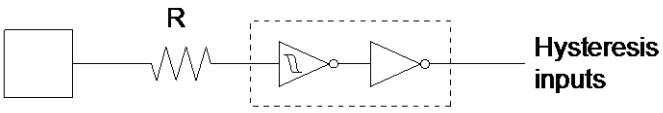
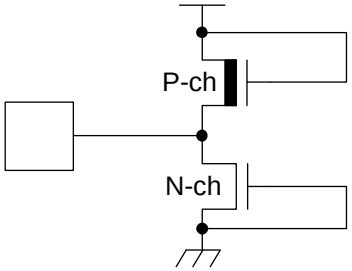
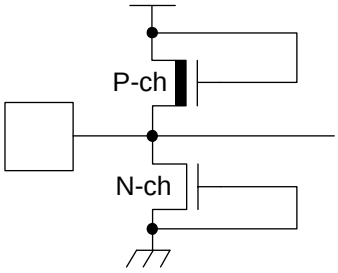
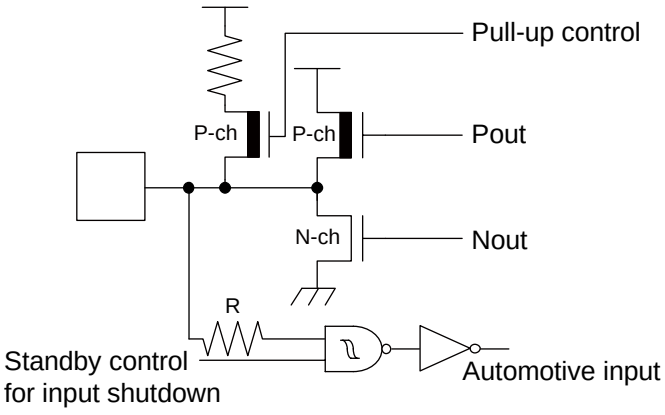
Pin no.	I/O circuit type*	Pin name
78	H	P00_4 / INT7_R / PPG9_B
79	H	P00_5 / IN6 / TTG2 / TTG6 / PPG10_B
80	H	P00_6 / IN7 / TTG3 / TTG7 / PPG11_B
81	H	P00_7 / INT14
82	M	P01_0 / SCK7
83	H	P01_1 / CKOT1 / OUT0 / SOT7
84	M	P01_2 / CKOTX1 / OUT1 / INT15 / SIN7
85	H	P01_3 / PPG5
86	M	P01_4 / SIN4 / INT8
87	H	P01_5 / SOT4
88	M	P01_6 / SCK4 / TTG12
89	M	P01_7 / CKOTX1_R / INT9 / TTG13 / ZIN0 / SCK7_R
90	H	P02_0 / CKOT1_R / INT10 / TTG14 / AIN0 / SOT7_R
91	M	P02_2 / IN7_R / CKOT0_R / INT12 / BIN0 / SIN7_R
92	M	P02_5 / OUT0_R / INT13 / SIN5_R
93	H	P03_0 / PPG4_B
94	H	P03_1 / PPG5_B
95	H	P03_2 / PPG14_B / SOT5_R
96	M	P03_3 / PPG15_B / SCK5_R
97	M	P03_4 / RX0 / INT4
98	H	P03_5 / TX0
99	H	P03_6 / INT0 / NMI
100	Supply	Vcc

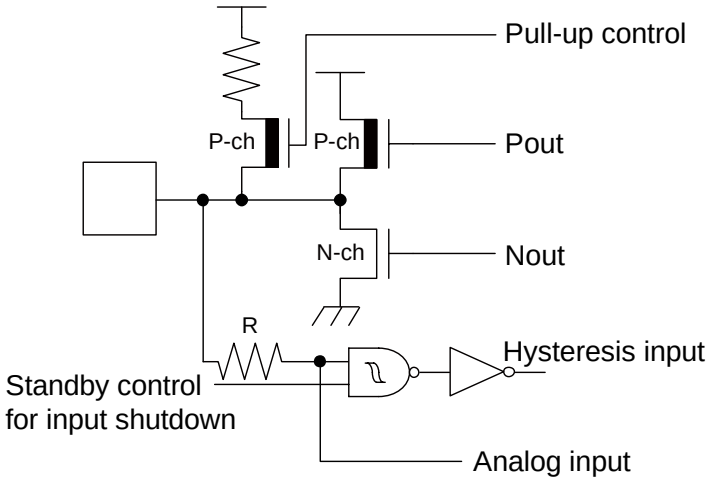
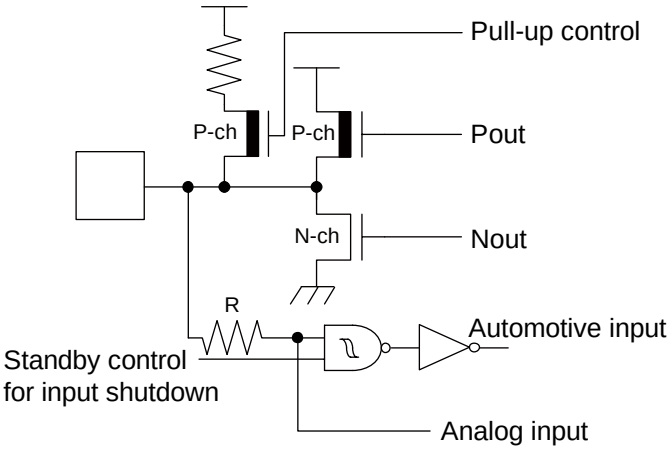
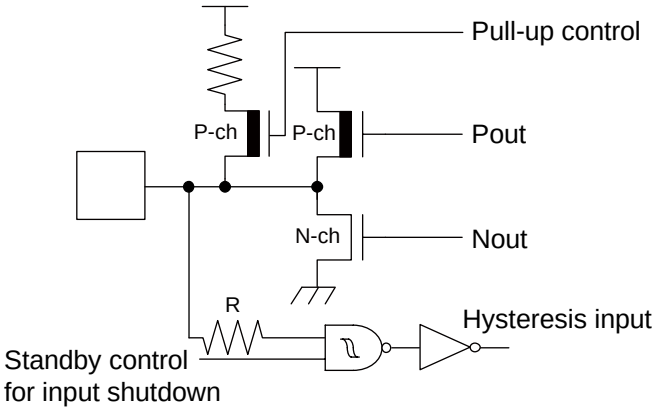
*: See “I/O Circuit Type” for details on the I/O circuit types.

6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. 1.0MΩ • The amplitude: 1.8V±0.15V to operate by the internal supply voltage

Type	Circuit	Remarks
B		Low-speed oscillation circuit shared with GPIO functionality: • Feedback resistor = approx. 5.0MΩ • GPIO functionality selectable (CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA), Automotive input with input shutdown function and programmable pull-up resistor)

Type	Circuit	Remarks
C		CMOS hysteresis input pin
F		Power supply input protection circuit
G		• A/D converter ref+ (AVRH)/ ref- (AVRL) power supply input pin with protection circuit • Without protection circuit against V_{CC} for pins AVRH/AVRL
H		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor

Type	Circuit	Remarks
I		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor • Analog input
K		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor • Analog input
M		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor

8. RAMSTART Addresses

Devices	Bank 0 RAM size	RAMSTART0
MB96F643	10KB	$00:5A00_H$
MB96F645	16KB	$00:4200_H$
MB96F646	24KB	$00:2200_H$
MB96F647	28KB	$00:1200_H$

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
40	$35C_H$	PPG2	Yes	40	Programmable Pulse Generator 2
41	358_H	PPG3	Yes	41	Programmable Pulse Generator 3
42	354_H	PPG4	Yes	42	Programmable Pulse Generator 4
43	350_H	PPG5	Yes	43	Programmable Pulse Generator 5
44	$34C_H$	PPG6	Yes	44	Programmable Pulse Generator 6
45	348_H	PPG7	Yes	45	Programmable Pulse Generator 7
46	344_H	PPG8	Yes	46	Programmable Pulse Generator 8
47	340_H	PPG9	Yes	47	Programmable Pulse Generator 9
48	$33C_H$	PPG10	Yes	48	Programmable Pulse Generator 10
49	338_H	PPG11	Yes	49	Programmable Pulse Generator 11
50	334_H	PPG12	Yes	50	Programmable Pulse Generator 12
51	330_H	PPG13	Yes	51	Programmable Pulse Generator 13
52	$32C_H$	PPG14	Yes	52	Programmable Pulse Generator 14
53	328_H	PPG15	Yes	53	Programmable Pulse Generator 15
54	324_H	-	-	54	Reserved
55	320_H	-	-	55	Reserved
56	$31C_H$	-	-	56	Reserved
57	318_H	-	-	57	Reserved
58	314_H	RLT0	Yes	58	Reload Timer 0
59	310_H	RLT1	Yes	59	Reload Timer 1
60	$30C_H$	RLT2	Yes	60	Reload Timer 2
61	308_H	RLT3	Yes	61	Reload Timer 3
62	304_H	-	-	62	Reserved
63	300_H	-	-	63	Reserved
64	$2FC_H$	RLT6	Yes	64	Reload Timer 6
65	$2F8_H$	ICU0	Yes	65	Input Capture Unit 0
66	$2F4_H$	ICU1	Yes	66	Input Capture Unit 1
67	$2F0_H$	-	-	67	Reserved
68	$2EC_H$	-	-	68	Reserved
69	$2E8_H$	ICU4	Yes	69	Input Capture Unit 4
70	$2E4_H$	ICU5	Yes	70	Input Capture Unit 5
71	$2E0_H$	ICU6	Yes	71	Input Capture Unit 6
72	$2DC_H$	ICU7	Yes	72	Input Capture Unit 7
73	$2D8_H$	-	-	73	Reserved
74	$2D4_H$	ICU9	Yes	74	Input Capture Unit 9
75	$2D0_H$	-	-	75	Reserved
76	$2CC_H$	-	-	76	Reserved
77	$2C8_H$	OCU0	Yes	77	Output Compare Unit 0
78	$2C4_H$	OCU1	Yes	78	Output Compare Unit 1
79	$2C0_H$	OCU2	Yes	79	Output Compare Unit 2
80	$2BC_H$	OCU3	Yes	80	Output Compare Unit 3
81	$2B8_H$	OCU4	Yes	81	Output Compare Unit 4

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage*1	V_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	
Analog power supply voltage*1	AV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
Analog reference voltage*1	AVRH, AVRL	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH > AVRL, AVRL $\geq AV_{SS}$
Input voltage*1	V_I	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V*3
Output voltage*1	V_O	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V*3
Maximum Clamp Current	I_{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins *4
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	-	26	mA	Applicable to general purpose I/O pins *4
"L" level maximum output current	I_{OL}	-	-	15	mA	
"L" level average output current	I_{OLAV}	-	-	4	mA	
"L" level maximum overall output current	ΣI_{OL}	-	-	66	mA	
"L" level average overall output current	ΣI_{OLAV}	-	-	33	mA	
"H" level maximum output current	I_{OH}	-	-	-15	mA	
"H" level average output current	I_{OHAV}	-	-	-4	mA	
"H" level maximum overall output current	ΣI_{OH}	-	-	-66	mA	
"H" level average overall output current	ΣI_{OHAV}	-	-	-33	mA	
Power consumption*5	P_D	T_A= +125°C	-	416*6	mW	
Operating ambient temperature	T_A	-	-40	+125*7	°C	
Storage temperature	T_{STG}	-	-55	+150	°C	

*1: This parameter is based on $V_{SS} = AV_{SS} = 0V$.

*2: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed V_{CC} + 0.3V. V_I should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/Output voltages of standard ports depend on V_{CC}.

*4: Applicable to all general purpose I/O pins (Pnn_m).

- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Sleep modes[*1]	I_{CCSPLL}	Vcc	PLL Sleep mode with CLKS1/2 = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	8.5	-	mA	T_A = +25°C
				-	-	14	mA	T_A = +105°C
				-	-	15.5	mA	T_A = +125°C
	$I_{CCSMAIN}$		Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	1	-	mA	T_A = +25°C
				-	-	4.5	mA	T_A = +105°C
				-	-	6	mA	T_A = +125°C
	I_{CCSRCH}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped)	-	0.6	-	mA	T_A = +25°C
				-	-	3.8	mA	T_A = +105°C
				-	-	5.3	mA	T_A = +125°C
	I_{CCSRCL}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 100kHz (CLKMC, CLKPLL and CLKSC stopped)	-	0.07	-	mA	T_A = +25°C
				-	-	2.8	mA	T_A = +105°C
				-	-	4.3	mA	T_A = +125°C
	I_{CCSSUB}		Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz, (CLKMC, CLKPLL and CLKRC stopped)	-	0.04	-	mA	T_A = +25°C
				-	-	2.5	mA	T_A = +105°C
				-	-	4	mA	T_A = +125°C

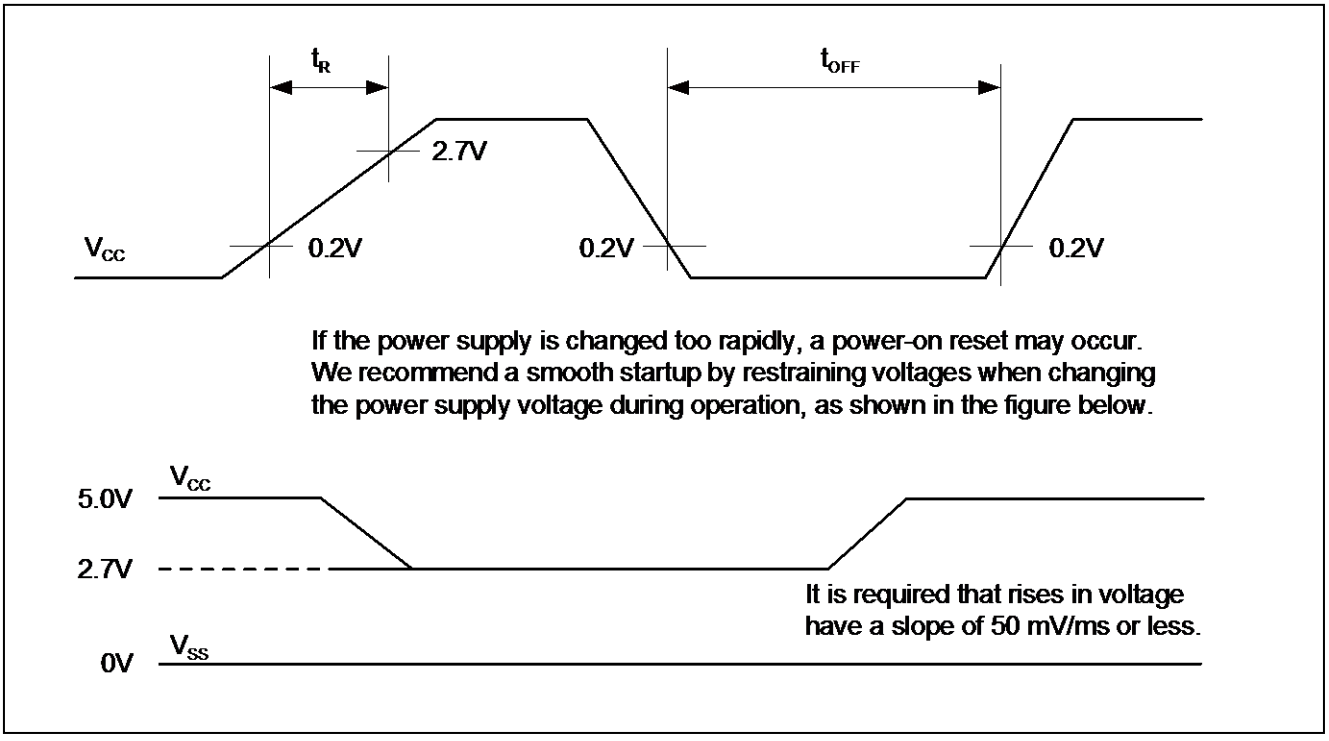
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Timer modes*2	I_{CCTPLL}	Vcc	PLL Timer mode with CLKPLL = 32MHz (CLKRC and CLKSC stopped)	-	1800	2250	µA	T_A = +25°C
				-	-	3220	µA	T_A = +105°C
				-	-	4025	µA	T_A = +125°C
	$I_{CCTMAIN}$		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	285	330	µA	T_A = +25°C
				-	-	1195	µA	T_A = +105°C
				-	-	2165	µA	T_A = +125°C
	I_{CCTRCH}		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped)	-	160	215	µA	T_A = +25°C
				-	-	1095	µA	T_A = +105°C
				-	-	2075	µA	T_A = +125°C
	I_{CCTRCL}		RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)	-	35	75	µA	T_A = +25°C
				-	-	905	µA	T_A = +105°C
				-	-	1880	µA	T_A = +125°C
	I_{CCTSUB}		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	65	µA	T_A = +25°C
				-	-	885	µA	T_A = +105°C
				-	-	1850	µA	T_A = +125°C

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH4}	4mA type	$4.5V \le V_{CC} \le 5.5V$ $I_{OH} = -4mA$	V_{CC} - 0.5	-	V_{CC}	V	
			$2.7V \le V_{CC} < 4.5V$ $I_{OH} = -1.5mA$					
	V_{OH3}	3mA type	$4.5V \le V_{CC} \le 5.5V$ $I_{OH} = -3mA$	V_{CC} - 0.5	-	V_{CC}	V	
			$2.7V \le V_{CC} < 4.5V$ $I_{OH} = -1.5mA$					
"L" level output voltage	V_{OL4}	4mA type	$4.5V \le V_{CC} \le 5.5V$ $I_{OL} = +4mA$	-	-	0.4	V	
			$2.7V \le V_{CC} < 4.5V$ $I_{OL} = +1.7mA$					
	V_{OL3}	3mA type	$2.7V \le V_{CC} < 5.5V$ $I_{OL} = +3mA$	-	-	0.4	V	
	V_{OLD}	DEBUG I/F	$V_{CC} = 2.7V$ $I_{OL} = +25mA$	0	-	0.25	V	
Input leak current	I_{IL}	Pnn_m	$V_{SS} < V_I < V_{CC}$ AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	- 1	-	+ 1	µA	
Pull-up resistance value	R_{PU}	Pnn_m	$V_{CC} = 5.0V \pm 10\%$	25	50	100	kΩ	
Input capacitance	C_{IN}	Other than C, Vcc, Vss, AVcc, AVss, AVRH, AVRL	-	-	5	15	pF	

14.4.7 Power-on Reset Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power on rise time	t_R	Vcc	0.05	-	30	ms
Power off time	t_{OFF}	Vcc	1	-	-	ms

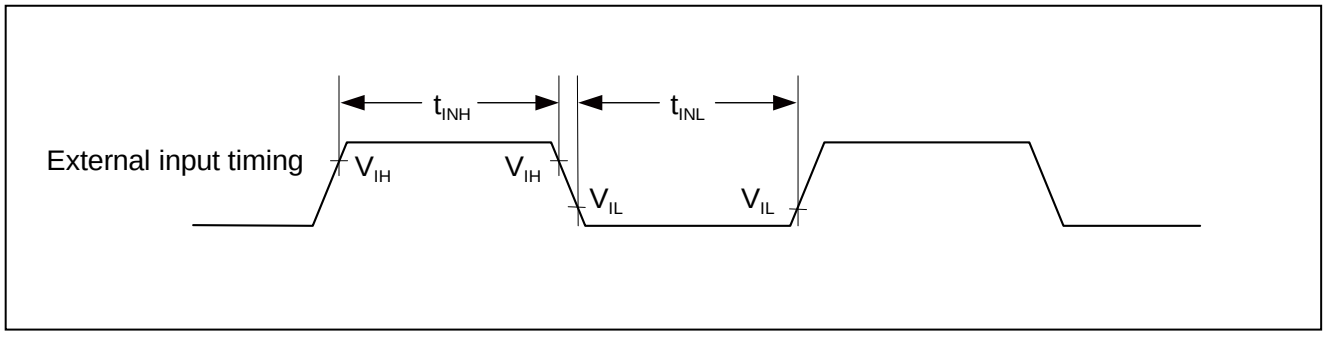


14.4.9 External Input Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{INH}, t_{INL}	Pnn_m	$2t_{CLKP1}$ +200 (t_{CLKP1}= $1/f_{CLKP1}$)*	-	ns	General Purpose I/O
		ADTG				A/D Converter trigger input
		TINn				Reload Timer
		TTGn				PPG trigger input
		FRCKn, FRCKn_R				Free-Running Timer input clock
		INn, INn_R				Input Capture
		AINn, BINn, ZINn				Quadrature Position/Revolution Counter
		INTn, INTn_R	200	-	ns	External Interrupt
		NMI				Non-Maskable Interrupt

*: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



14.4.10 I^2C Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	C_L = 50pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	µs
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	µs
(Repeated) START condition setup time SCL ↑ →SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs
Bus free time between "STOP condition" and "START condition"	t_{BUS}		4.7	-	1.3	-	µs
Pulse width of spikes which will be suppressed by input noise filter	t_{SP}	-	0	(1-1.5) × t_{CLKP1}*5	0	(1-1.5) × t_{CLKP1}*5	ns

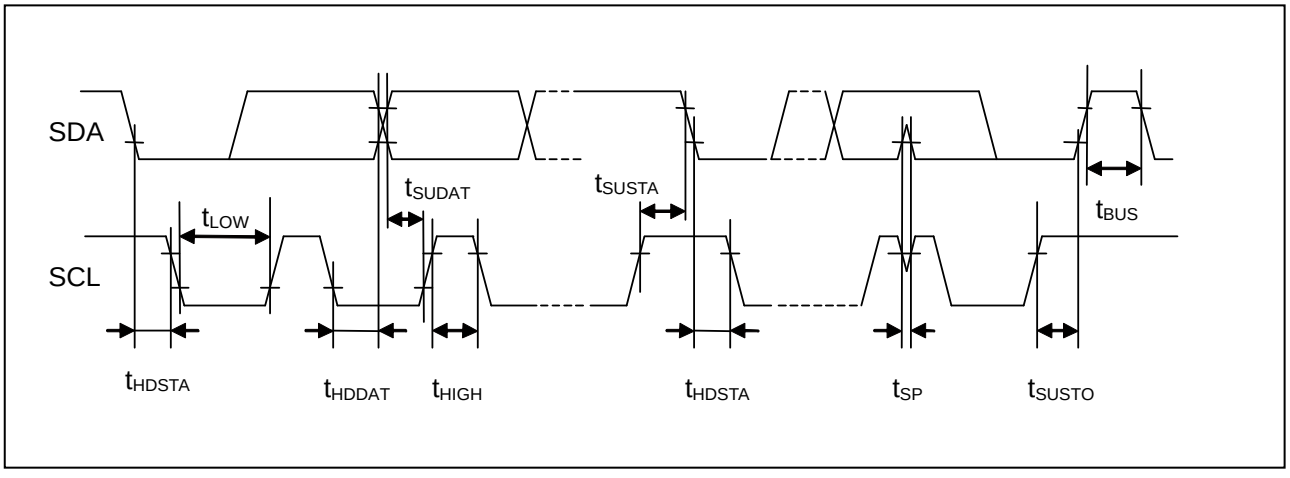
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

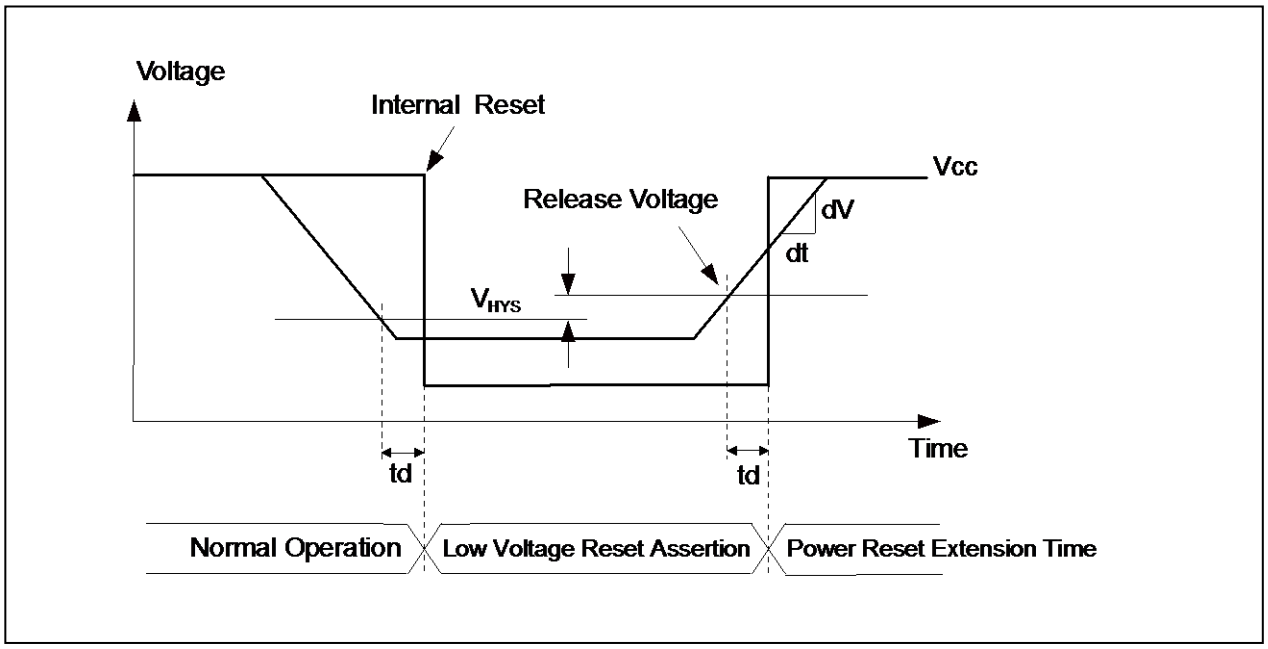
*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

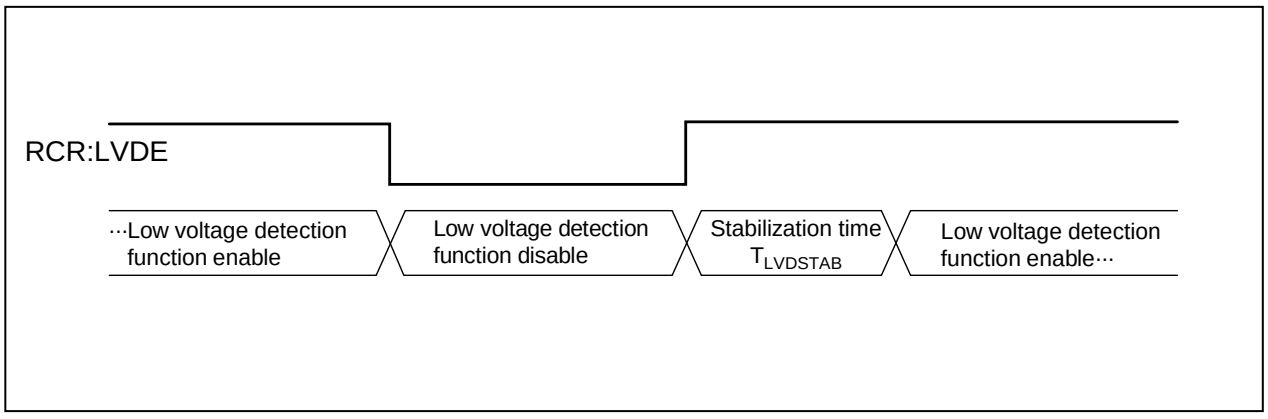
*3: A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250ns".

*4: For use at over 100 kHz, set the peripheral clock1 (CLKP1) to at least 6MHz.

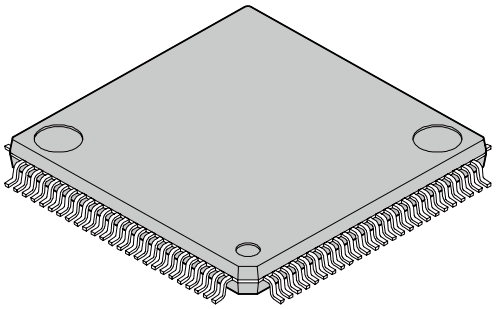
*5: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time.




Voltage
Internal Reset
Vcc
Release Voltage
dV
dt
V_{HYS}
Time
td
td
Normal Operation
Low Voltage Reset Assertion
Power Reset Extension Time

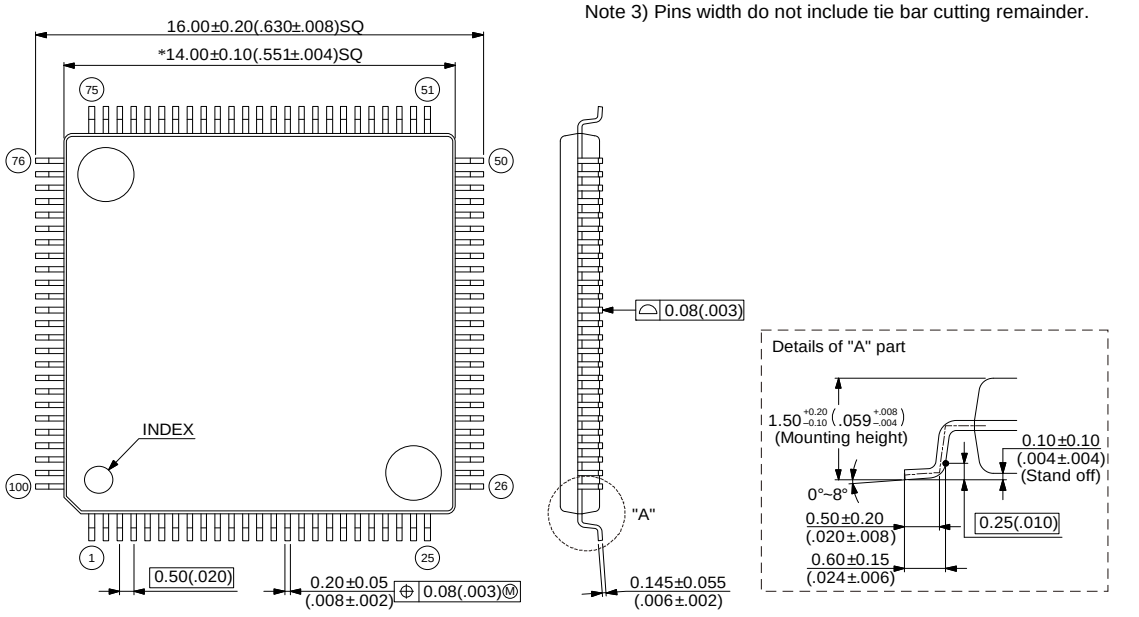

RCR:LVDE
···Low voltage detection function enable
Low voltage detection function disable
Stabilization time $T_{LVDSTAB}$
Low voltage detection function enable···

17. Package Dimension

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50

100-pin plastic LQFP
(FPT-100P-M20)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Page	Section	Change Results
57	Electrical Characteristics 7. Flash Memory Write/Erase Characteristics	Changed the Note While the Flash memory is written or erased, shutdown of the external power (VCC) is prohibited. In the application system where the external power (VCC) might be shut down while writing, be sure to turn the power off by using an external voltage detector. → While the Flash memory is written or erased, shutdown of the external power (VCC) is prohibited. In the application system where the external power (VCC) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.
Revision 2.1		
-	-	Company name and layout design change

NOTE: Please see "Document History" about later revised information.