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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f645rbpmc-gse2

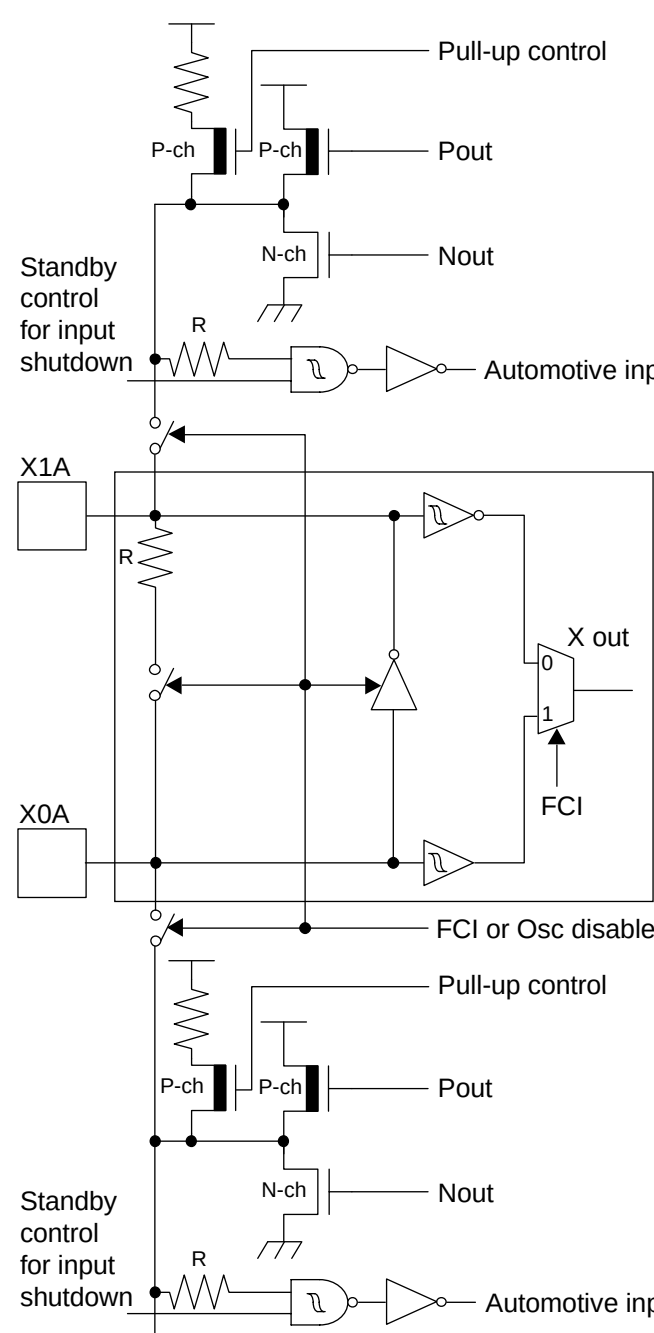
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4. Pin Description

Pin name	Feature	Description
ADTG	ADC	A/D converter trigger input pin
AINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
ANn	ADC	A/D converter channel n input pin
AVcc	Supply	Analog circuits power supply pin
AVRH	ADC	A/D converter high reference voltage input pin
AVRL	ADC	A/D converter low reference voltage input pin
AVss	Supply	Analog circuits power supply pin
BINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock Output function	Clock Output function n output pin
CKOTn_R	Clock Output function	Relocated Clock Output function n output pin
CKOTXn	Clock Output function	Clock Output function n inverted output pin
CKOTXn_R	Clock Output function	Relocated Clock Output function n inverted output pin
DEBUG I/F	OCD	On Chip Debugger input/output pin
FRCKn	Free-Running Timer	Free-Running Timer n input pin
FRCKn_R	Free-Running Timer	Relocated Free-Running Timer n input pin
INn	ICU	Input Capture Unit n input pin
INn_R	ICU	Relocated Input Capture Unit n input pin
INTn	External Interrupt	External Interrupt n input pin
INTn_R	External Interrupt	Relocated External Interrupt n input pin
MD	Core	Input pin for specifying the operating mode
NMI	External Interrupt	Non-Maskable Interrupt input pin
OUTn	OCU	Output Compare Unit n waveform output pin
OUTn_R	OCU	Relocated Output Compare Unit n waveform output pin
Pnn_m	GPIO	General purpose I/O pin
PPGn	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_R	PPG	Relocated Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
RSTX	Core	Reset input pin
RXn	CAN	CAN interface n RX input pin
SCKn	USART	USART n serial clock input/output pin
SCKn_R	USART	Relocated USART n serial clock input/output pin
SCLn	I ² C	I ² C interface n clock I/O input/output pin
SDAn	I ² C	I ² C interface n serial data I/O input/output pin
SINn	USART	USART n serial data input pin
SINn_R	USART	Relocated USART n serial data input pin
SOTn	USART	USART n serial data output pin
SOTn_R	USART	Relocated USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TOTn	Reload Timer	Reload Timer n output pin

Pin name	Feature	Description
TTGn	PPG	Programmable Pulse Generator n trigger input pin
TXn	CAN	CAN interface n TX output pin
Vcc	Supply	Power supply pin
Vss	Supply	Power supply pin
WOT	RTC	Real Time clock output pin
WOT_R	RTC	Relocated Real Time clock output pin
X0	Clock	Oscillator input pin
X0A	Clock	Subclock Oscillator input pin
X1	Clock	Oscillator output pin
X1A	Clock	Subclock Oscillator output pin
ZINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin

Type	Circuit	Remarks
B	 The circuit diagram illustrates a low-speed oscillation circuit shared with GPIO functionality. It features two identical input/output blocks. Each block includes a pull-up control (P-ch MOSFET), a pull-up resistor (R), a standby control for input shutdown, an automotive input (N-ch MOSFET), and an automotive input buffer. The output stage consists of a P-ch MOSFET (Pout), an N-ch MOSFET (Nout), and a feedback resistor (R). The output is connected to a multiplexer (X out) with inputs 0 and 1, controlled by FCI. The circuit is also controlled by FCI or Osc disable.	Low-speed oscillation circuit shared with GPIO functionality: • Feedback resistor = approx. $5.0\text{M}\Omega$ • GPIO functionality selectable (CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$), Automotive input with input shutdown function and programmable pull-up resistor)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
40	35C _H	PPG2	Yes	40	Programmable Pulse Generator 2
41	358 _H	PPG3	Yes	41	Programmable Pulse Generator 3
42	354 _H	PPG4	Yes	42	Programmable Pulse Generator 4
43	350 _H	PPG5	Yes	43	Programmable Pulse Generator 5
44	34C _H	PPG6	Yes	44	Programmable Pulse Generator 6
45	348 _H	PPG7	Yes	45	Programmable Pulse Generator 7
46	344 _H	PPG8	Yes	46	Programmable Pulse Generator 8
47	340 _H	PPG9	Yes	47	Programmable Pulse Generator 9
48	33C _H	PPG10	Yes	48	Programmable Pulse Generator 10
49	338 _H	PPG11	Yes	49	Programmable Pulse Generator 11
50	334 _H	PPG12	Yes	50	Programmable Pulse Generator 12
51	330 _H	PPG13	Yes	51	Programmable Pulse Generator 13
52	32C _H	PPG14	Yes	52	Programmable Pulse Generator 14
53	328 _H	PPG15	Yes	53	Programmable Pulse Generator 15
54	324 _H	-	-	54	Reserved
55	320 _H	-	-	55	Reserved
56	31C _H	-	-	56	Reserved
57	318 _H	-	-	57	Reserved
58	314 _H	RLT0	Yes	58	Reload Timer 0
59	310 _H	RLT1	Yes	59	Reload Timer 1
60	30C _H	RLT2	Yes	60	Reload Timer 2
61	308 _H	RLT3	Yes	61	Reload Timer 3
62	304 _H	-	-	62	Reserved
63	300 _H	-	-	63	Reserved
64	2FC _H	RLT6	Yes	64	Reload Timer 6
65	2F8 _H	ICU0	Yes	65	Input Capture Unit 0
66	2F4 _H	ICU1	Yes	66	Input Capture Unit 1
67	2F0 _H	-	-	67	Reserved
68	2EC _H	-	-	68	Reserved
69	2E8 _H	ICU4	Yes	69	Input Capture Unit 4
70	2E4 _H	ICU5	Yes	70	Input Capture Unit 5
71	2E0 _H	ICU6	Yes	71	Input Capture Unit 6
72	2DC _H	ICU7	Yes	72	Input Capture Unit 7
73	2D8 _H	-	-	73	Reserved
74	2D4 _H	ICU9	Yes	74	Input Capture Unit 9
75	2D0 _H	-	-	75	Reserved
76	2CC _H	-	-	76	Reserved
77	2C8 _H	OCU0	Yes	77	Output Compare Unit 0
78	2C4 _H	OCU1	Yes	78	Output Compare Unit 1
79	2C0 _H	OCU2	Yes	79	Output Compare Unit 2
80	2BC _H	OCU3	Yes	80	Output Compare Unit 3
81	2B8 _H	OCU4	Yes	81	Output Compare Unit 4

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
82	2B4 _H	-	-	82	Reserved
83	2B0 _H	OCU6	Yes	83	Output Compare Unit 6
84	2AC _H	OCU7	Yes	84	Output Compare Unit 7
85	2A8 _H	-	-	85	Reserved
86	2A4 _H	-	-	86	Reserved
87	2A0 _H	-	-	87	Reserved
88	29C _H	-	-	88	Reserved
89	298 _H	FRT0	Yes	89	Free-Running Timer 0
90	294 _H	FRT1	Yes	90	Free-Running Timer 1
91	290 _H	FRT2	Yes	91	Free-Running Timer 2
92	28C _H	-	-	92	Reserved
93	288 _H	RTC0	No	93	Real Time Clock
94	284 _H	CAL0	No	94	Clock Calibration Unit
95	280 _H	-	-	95	Reserved
96	27C _H	IIC0	Yes	96	I ² C interface 0
97	278 _H	IIC1	Yes	97	I ² C interface 1
98	274 _H	ADC0	Yes	98	A/D Converter 0
99	270 _H	-	-	99	Reserved
100	26C _H	-	-	100	Reserved
101	268 _H	LINR0	Yes	101	LIN USART 0 RX
102	264 _H	LINT0	Yes	102	LIN USART 0 TX
103	260 _H	LINR1	Yes	103	LIN USART 1 RX
104	25C _H	LINT1	Yes	104	LIN USART 1 TX
105	258 _H	LINR2	Yes	105	LIN USART 2 RX
106	254 _H	LINT2	Yes	106	LIN USART 2 TX
107	250 _H	-	-	107	Reserved
108	24C _H	-	-	108	Reserved
109	248 _H	LINR4	Yes	109	LIN USART 4 RX
110	244 _H	LINT4	Yes	110	LIN USART 4 TX
111	240 _H	LINR5	Yes	111	LIN USART 5 RX
112	23C _H	LINT5	Yes	112	LIN USART 5 TX
113	238 _H	-	-	113	Reserved
114	234 _H	-	-	114	Reserved
115	230 _H	LINR7	Yes	115	LIN USART 7 RX
116	22C _H	LINT7	Yes	116	LIN USART 7 TX
117	228 _H	-	-	117	Reserved
118	224 _H	-	-	118	Reserved
119	220 _H	-	-	119	Reserved
120	21C _H	-	-	120	Reserved

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
121	218 _H	-	-	121	Reserved
122	214 _H	-	-	122	Reserved
123	210 _H	-	-	123	Reserved
124	20C _H	-	-	124	Reserved
125	208 _H	-	-	125	Reserved
126	204 _H	-	-	126	Reserved
127	200 _H	-	-	127	Reserved
128	1FC _H	-	-	128	Reserved
129	1F8 _H	-	-	129	Reserved
130	1F4 _H	-	-	130	Reserved
131	1F0 _H	-	-	131	Reserved
132	1EC _H	-	-	132	Reserved
133	1E8 _H	FLASHA	Yes	133	Flash memory A interrupt
134	1E4 _H	-	-	134	Reserved
135	1E0 _H	-	-	135	Reserved
136	1DC _H	-	-	136	Reserved
137	1D8 _H	QPRC0	Yes	137	Quad Position/Revolution counter 0
138	1D4 _H	QPRC1	Yes	138	Quad Position/Revolution counter 1
139	1D0 _H	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	1CC _H	-	-	140	Reserved
141	1C8 _H	-	-	141	Reserved
142	1C4 _H	-	-	142	Reserved
143	1C0 _H	-	-	143	Reserved

■Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

12.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

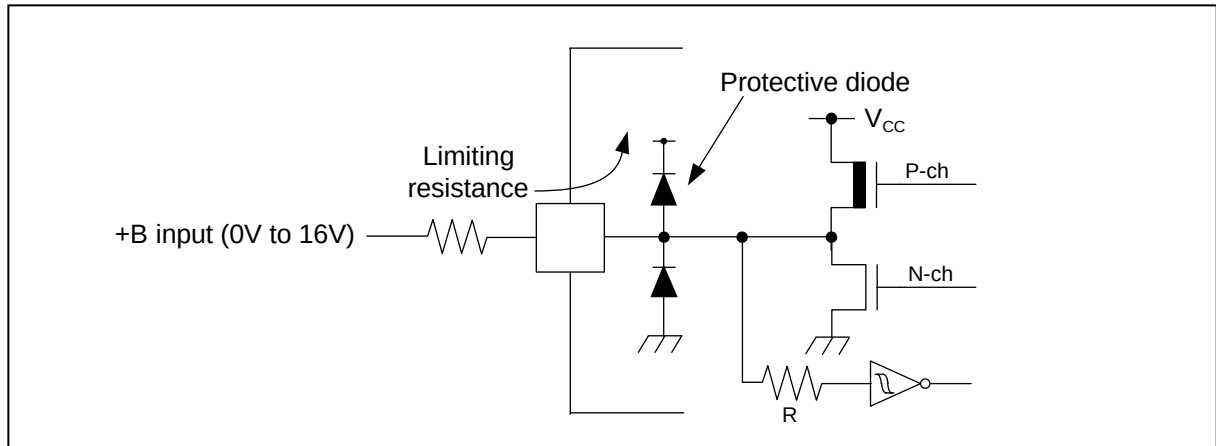
1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
- The DEBUG I/F pin has only a protective diode against VSS. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.
- Sample recommended circuits:



*5: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.

The actual power dissipation depends on the customer application and can be calculated as follows:

$$P_D = P_{IO} + P_{INT}$$

$$P_{IO} = \sum (V_{OL} \times I_{OL} + V_{OH} \times I_{OH}) \text{ (I/O load power dissipation, sum is performed on all I/O ports)}$$

$$P_{INT} = V_{CC} \times (I_{CC} + I_A) \text{ (internal power dissipation)}$$

I_{CC} is the total core current consumption into V_{CC} as described in the "DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.

I_A is the analog current consumption into AV_{CC} .

*6: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*7: Write/erase to a large sector in flash memory is warranted with $T_A \leq +105^\circ\text{C}$.

WARNING

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.3 DC Characteristics

14.3.1 Current Rating

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes ¹	I _{CCPLL}	V _{CC}	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz	-	27	-	mA	T _A = +25°C
			Flash 0 wait	-	-	37	mA	T _A = +105°C
			(CLKRC and CLKSC stopped)	-	-	38.5	mA	T _A = +125°C
	I _{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz	-	3.5	-	mA	T _A = +25°C
			Flash 0 wait	-	-	8	mA	T _A = +105°C
			(CLKPLL, CLKSC and CLKRC stopped)	-	-	9.5	mA	T _A = +125°C
	I _{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz	-	1.8	-	mA	T _A = +25°C
			Flash 0 wait	-	-	6	mA	T _A = +105°C
			(CLKMC, CLKPLL and CLKSC stopped)	-	-	7.5	mA	T _A = +125°C
	I _{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz	-	0.16	-	mA	T _A = +25°C
			Flash 0 wait	-	-	3.5	mA	T _A = +105°C
			(CLKMC, CLKPLL and CLKSC stopped)	-	-	5	mA	T _A = +125°C
	I _{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz	-	0.1	-	mA	T _A = +25°C
			Flash 0 wait	-	-	3.3	mA	T _A = +105°C
			(CLKMC, CLKPLL and CLKRC stopped)	-	-	4.8	mA	T _A = +125°C

14.3.2 Pin Characteristics
 $(V_{CC} = AV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +125^{\circ}C)$

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Port inputs Pnn_m	-	$V_{CC} \times 0.7$	-	$V_{CC} + 0.3$	V	CMOS Hysteresis input
			-	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	AUTOMOTIVE Hysteresis input
	V_{IHx0S}	X0	External clock in "Fast Clock Input mode"	$V_D \times 0.8$	-	V_D	V	$V_D=1.8V \pm 0.15V$
	V_{IHx0AS}	X0A	External clock in "Oscillation mode"	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
	V_{IHR}	RSTX	-	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	CMOS Hysteresis input
	V_{IHM}	MD	-	$V_{CC} - 0.3$	-	$V_{CC} + 0.3$	V	CMOS Hysteresis input
	V_{IHD}	DEBUG I/F	-	2.0	-	$V_{CC} + 0.3$	V	TTL Input
"L" level input voltage	V_{IL}	Port inputs Pnn_m	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.3$	V	CMOS Hysteresis input
			-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.5$	V	AUTOMOTIVE Hysteresis input
	V_{ILx0S}	X0	External clock in "Fast Clock Input mode"	V_{SS}	-	$V_D \times 0.2$	V	$V_D=1.8V \pm 0.15V$
	V_{ILx0AS}	X0A	External clock in "Oscillation mode"	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
	V_{ILR}	RSTX	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	CMOS Hysteresis input
	V_{ILM}	MD	-	$V_{SS} - 0.3$	-	$V_{SS} + 0.3$	V	CMOS Hysteresis input
	V_{ILD}	DEBUG I/F	-	$V_{SS} - 0.3$	-	0.8	V	TTL Input

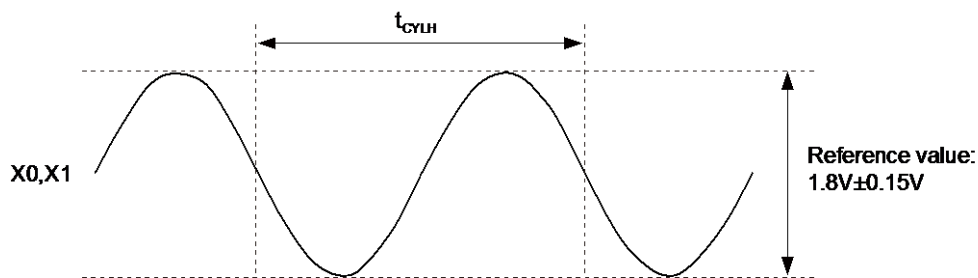
14.4 AC Characteristics

14.4.1 Main Clock Input Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_D = 1.8V \pm 0.15V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$)

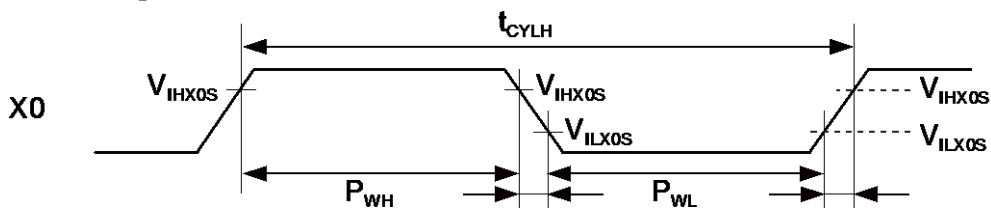
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f_C	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL off
			4	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL on
Input clock cycle	t_{CYLH}	-	125	-	-	ns	
Input clock pulse width	P_{WH}, P_{WL}	-	55	-	-	ns	

When using the crystal oscillator



The amplitude changes by resistance, capacity which added outside or the difference of the device.

When using the external clock



14.4.3 Built-in RC Oscillation Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	f_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	80	160	320	μs	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	μs	When using fast frequency of RC oscillator (256 RC clock cycles)

14.4.4 Internal Clock Timing

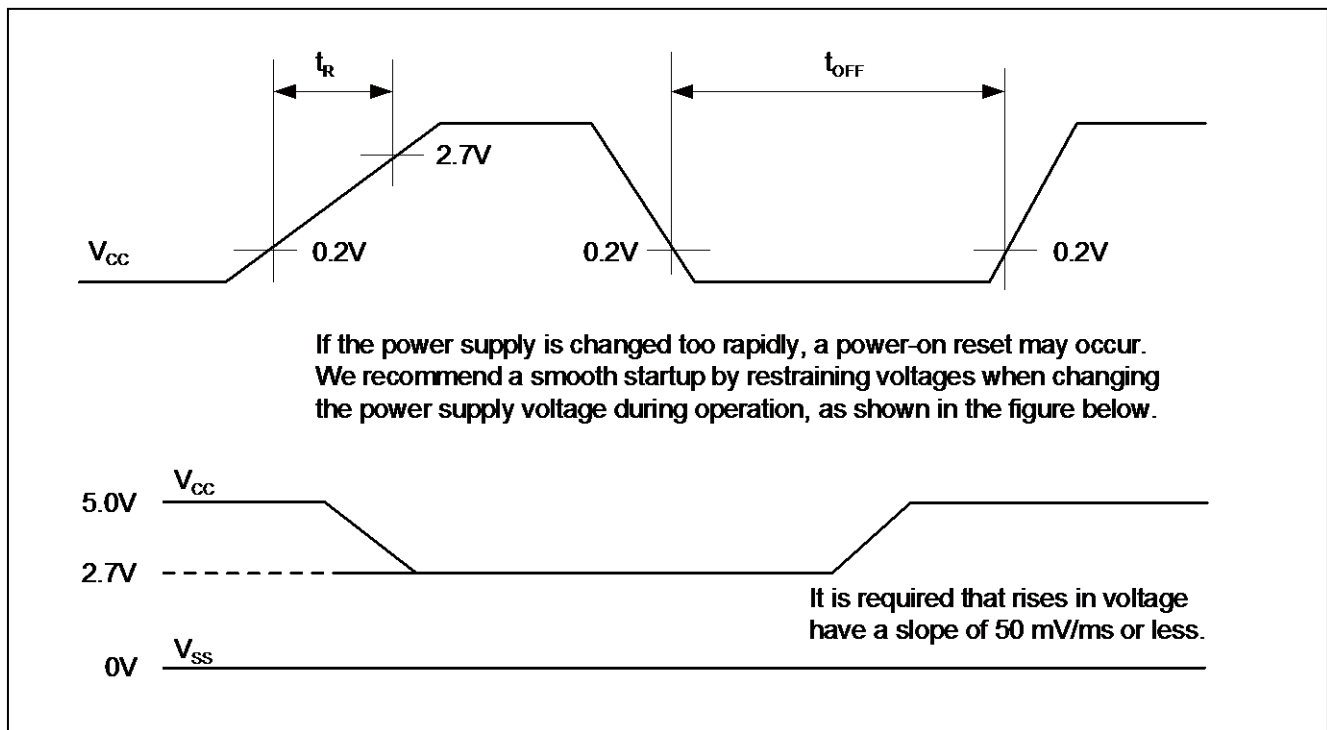
($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

14.4.7 Power-on Reset Timing

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

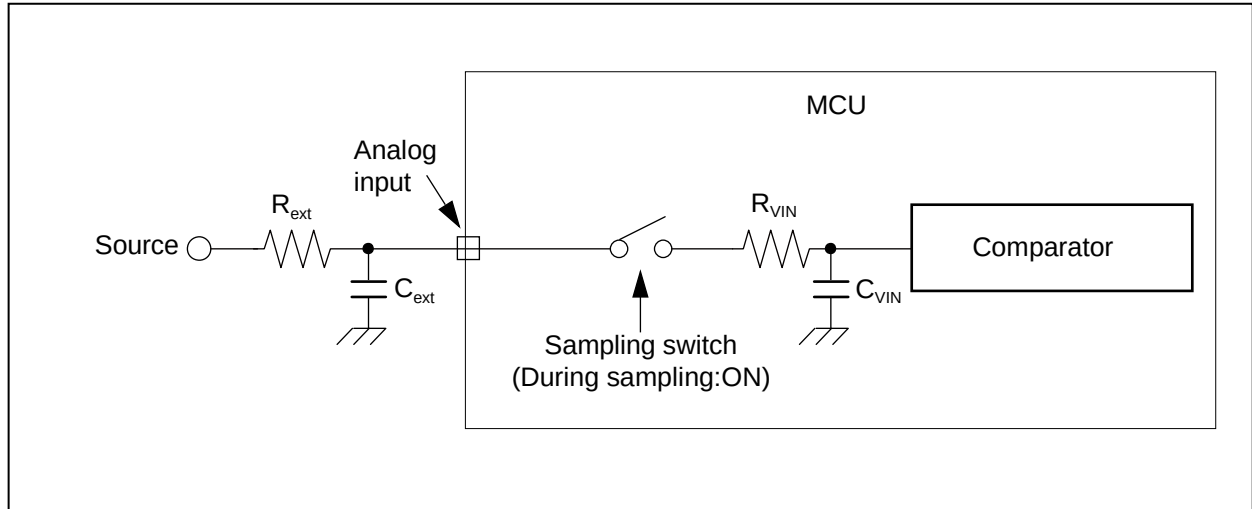
Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power on rise time	t_R	Vcc	0.05	-	30	ms
Power off time	t_{OFF}	Vcc	1	-	-	ms



14.5.2 Accuracy and Setting of the A/D Converter Sampling Time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (T_{samp}) depends on the external driving impedance R_{ext} , the board capacitance of the A/D converter input pin C_{ext} and the AV_{CC} voltage level. The following replacement model can be used for the calculation:



R_{ext} : External driving impedance

C_{ext} : Capacitance of PCB at A/D converter input

C_{VIN} : Analog input capacity (I/O, analog switch and ADC are contained)

R_{VIN} : Analog input impedance (I/O, analog switch and ADC are contained)

The following approximation formula for the replacement model above can be used:

$$T_{\text{samp}} = 7.62 \times (R_{\text{ext}} \times C_{\text{ext}} + (R_{\text{ext}} + R_{\text{VIN}}) \times C_{\text{VIN}})$$

- Do not select a sampling time below the absolute minimum permitted value.
($0.5\mu\text{s}$ for $4.5\text{V} \leq AV_{\text{CC}} \leq 5.5\text{V}$, $1.2\mu\text{s}$ for $2.7\text{V} \leq AV_{\text{CC}} < 4.5\text{V}$)
- If the sampling time cannot be sufficient, connect a capacitor of about $0.1\mu\text{F}$ to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current I_{IL} (static current before the sampling switch) or the analog input leakage current I_{AIN} (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current I_{IL} cannot be compensated by an external capacitor.
- The accuracy gets worse as $|AV_{\text{RH}} - AV_{\text{RL}}|$ becomes smaller.

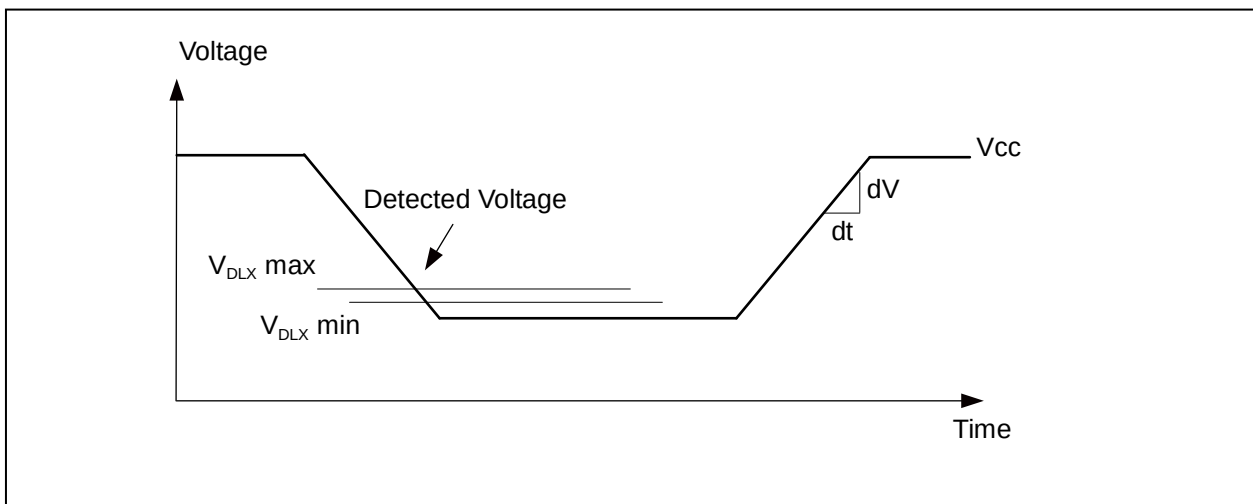
14.6 Low Voltage Detection Function Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

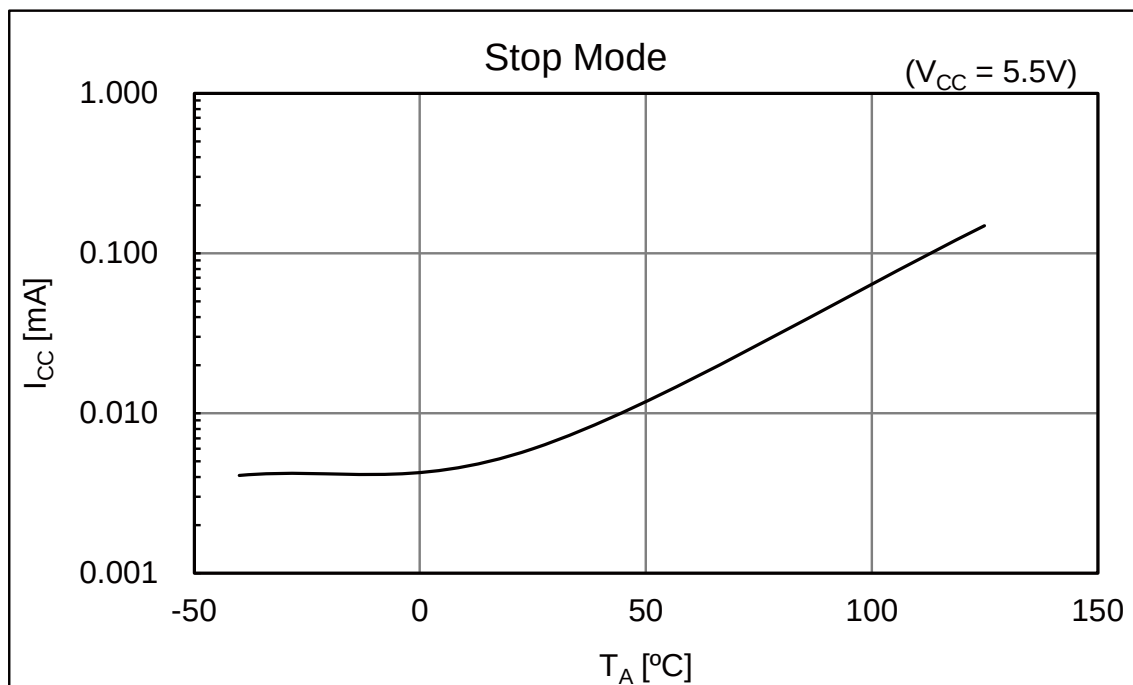
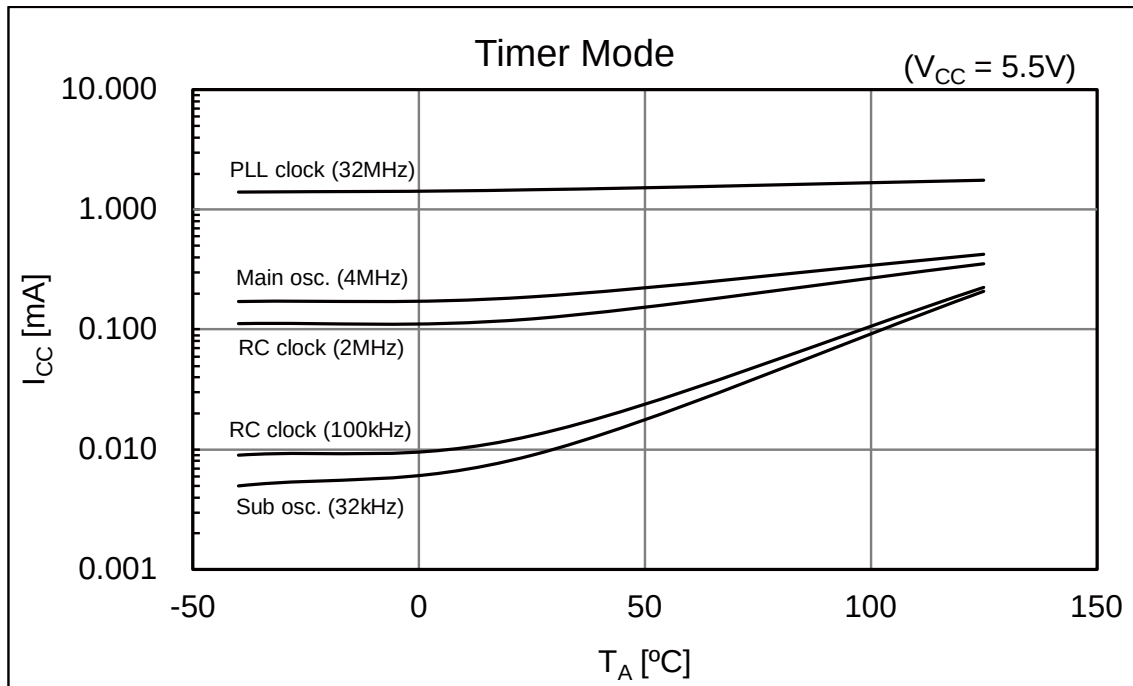
Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Detected voltage ^{*1}	V_{DL0}	CILCR:LVL = 0000 _B	2.70	2.90	3.10	V
	V_{DL1}	CILCR:LVL = 0001 _B	2.79	3.00	3.21	V
	V_{DL2}	CILCR:LVL = 0010 _B	2.98	3.20	3.42	V
	V_{DL3}	CILCR:LVL = 0011 _B	3.26	3.50	3.74	V
	V_{DL4}	CILCR:LVL = 0100 _B	3.45	3.70	3.95	V
	V_{DL5}	CILCR:LVL = 0111 _B	3.73	4.00	4.27	V
	V_{DL6}	CILCR:LVL = 1001 _B	3.91	4.20	4.49	V
Power supply voltage change rate ^{*2}	dV/dt	-	- 0.004	-	+ 0.004	V/ μ s
Hysteresis width	V_{HYS}	CILCR:LVHYS=0	-	-	50	mV
		CILCR:LVHYS=1	80	100	120	mV
Stabilization time	$T_{LVDSTAB}$	-	-	-	75	μ s
Detection delay time	t_d	-	-	-	30	μ s

*1: If the power supply voltage fluctuates within the time less than the detection delay time (t_d), there is a possibility that the low voltage detection will occur or stop after the power supply voltage passes the detection range.

*2: In order to perform the low voltage detection at the detection voltage (V_{DLX}), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.



■ MB96F647



16. Ordering Information

MCU with CAN controller

Part number	Flash memory	Package*
MB96F643RBPMC-GSE1	Flash A (96.5KB)	100-pin plastic LQFP (FPT-100P-M20)
MB96F643RBPMC-GSE2		
MB96F645RBPMC-GSE1	Flash A (160.5KB)	100-pin plastic LQFP (FPT-100P-M20)
MB96F645RBPMC-GSE2		
MB96F646RBPMC-GSE1	Flash A (288.5KB)	100-pin plastic LQFP (FPT-100P-M20)
MB96F646RBPMC-GSE2		
MB96F647RBPMC-GSE1	Flash A (416.5KB)	100-pin plastic LQFP (FPT-100P-M20)
MB96F647RBPMC-GSE2		

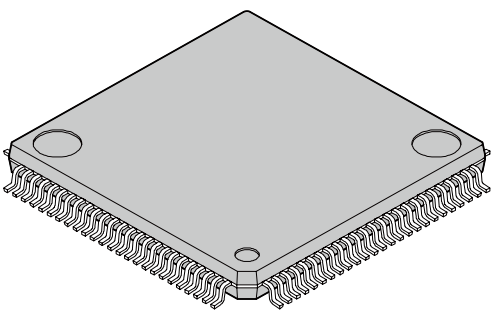
*: For details about package, see "Package Dimension".

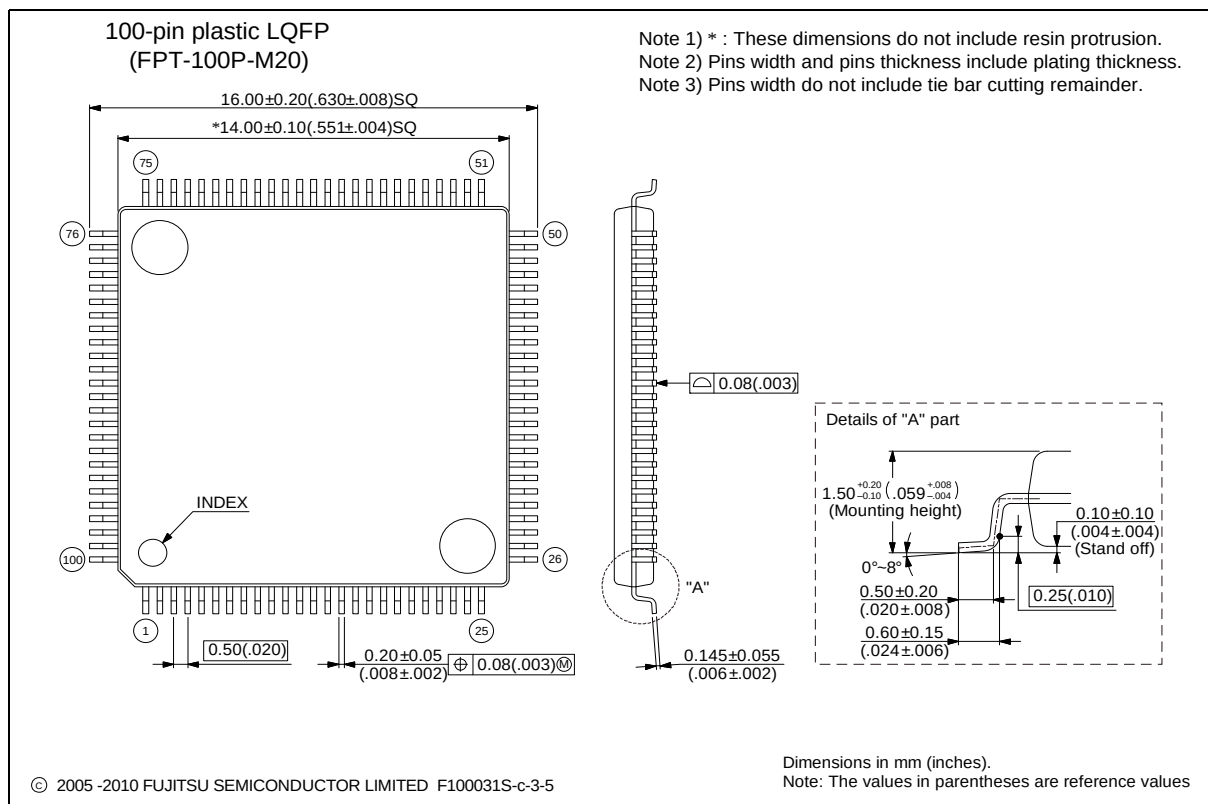
MCU without CAN controller

Part number	Flash memory	Package*
MB96F643ABPMC-GSE1	Flash A (96.5KB)	100-pin plastic LQFP (FPT-100P-M20)
MB96F643ABPMC-GSE2		
MB96F645ABPMC-GSE1	Flash A (160.5KB)	100-pin plastic LQFP (FPT-100P-M20)
MB96F645ABPMC-GSE2		

*: For details about package, see "Package Dimension".

17. Package Dimension

 100-pin plastic LQFP (FPT-100P-M20)	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
	Code (Reference)	P-LFQFP100-14×14-0.50



18. Major Changes

Spanion Publication Number: MB96640_DS704-00009

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 2.0		
4	Features	Changed the description of "External Interrupts" Interrupt mask and pending bit per channel → Interrupt mask bit per channel
26 to 29	Handling Precautions	Added a section
37	Electrical Characteristics 3. DC Characteristics (1) Current Rating	Changed the Conditions for I_{CCSRCH} $CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz$, → $CLKS1/2 = CLKP1/2 = CLKRC = 2MHz$,
		Changed the Conditions for I_{CCSRCL} $CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz$ → $CLKS1/2 = CLKP1/2 = CLKRC = 100kHz$
38		Changed the Conditions for I_{CCTPLL} PLL Timer mode with $CLKP1 = 32MHz$ → PLL Timer mode with $CLKPLL = 32MHz$
		Changed the Value of "Power supply current in Timer modes" I_{CCTPLL} Typ: $2485\mu A \rightarrow 1800\mu A$ ($T_A = +25^\circ C$) Max: $2715\mu A \rightarrow 2250\mu A$ ($T_A = +25^\circ C$) Max: $4095\mu A \rightarrow 3220\mu A$ ($T_A = +105^\circ C$) Max: $5065\mu A \rightarrow 4025\mu A$ ($T_A = +125^\circ C$)
		Changed the Conditions for I_{CCTRCL} RC Timer mode with $CLKRC = 100kHz$, SMCR:LPMSS = 0 ($CLKPLL$, $CLKMC$ and $CLKSC$ stopped) → RC Timer mode with $CLKRC = 100kHz$ ($CLKPLL$, $CLKMC$ and $CLKSC$ stopped)
39		Changed the annotation *2 Power supply for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current. → The current for "On Chip Debugger" part is not included.
50	4. AC Characteristics (10) I^2C timing	Added parameter, "Noise filter" and an annotation *5 for it Added t_{SP} to the figure
52	5. A/D Converter (2) Accuracy and Setting of the A/D Converter Sampling Time	Deleted the unit "[Min]" from approximation formula of Sampling time
57	7. Flash Memory Write/Erase Characteristics	Changed the condition ($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_D = 1.8V \pm 0.15V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$) → ($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$)