



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

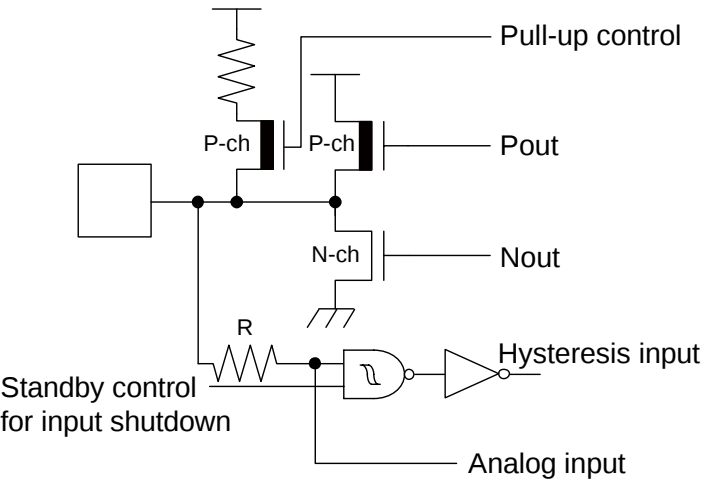
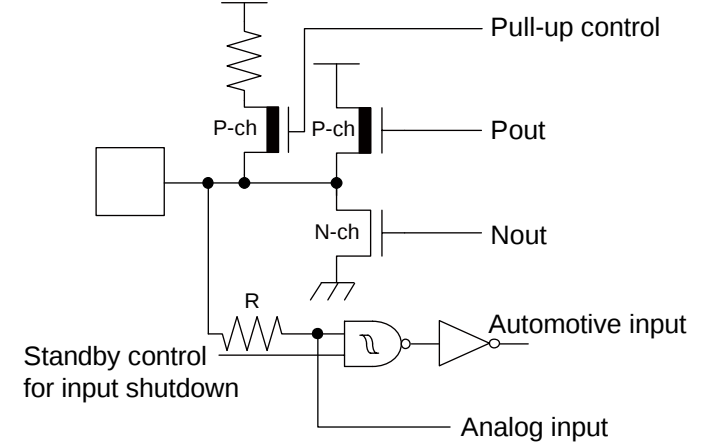
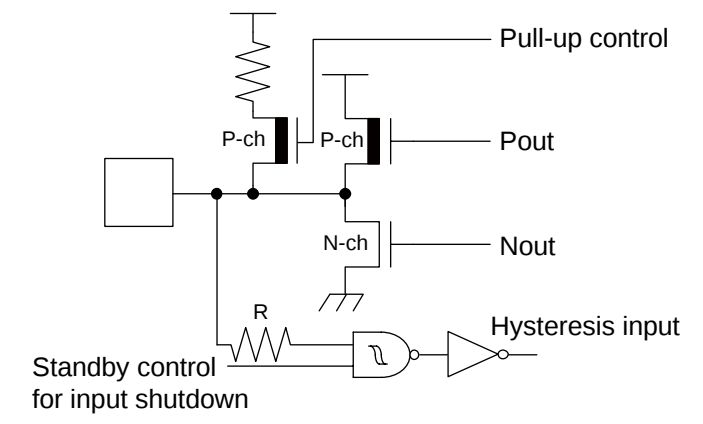
Details

Product Status	Obsolete
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	28K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f647rbpmc-gse2

14.4.9 External Input Timing	48
14.4.10 I ² C Timing.....	49
14.5 A/D Converter.....	50
14.5.1 Electrical Characteristics for the A/D Converter	50
14.5.2 Accuracy and Setting of the A/D Converter Sampling Time	51
14.5.3 Definition of A/D Converter Terms	52
14.6 Low Voltage Detection Function Characteristics	54
14.7 Flash Memory Write/Erase Characteristics	56
15. Example Characteristics	57
16. Ordering Information	60
17. Package Dimension	61
18. Major Changes	62
Document History.....	64

Pin name	Feature	Description
TTGn	PPG	Programmable Pulse Generator n trigger input pin
TXn	CAN	CAN interface n TX output pin
Vcc	Supply	Power supply pin
Vss	Supply	Power supply pin
WOT	RTC	Real Time clock output pin
WOT_R	RTC	Relocated Real Time clock output pin
X0	Clock	Oscillator input pin
X0A	Clock	Subclock Oscillator input pin
X1	Clock	Oscillator output pin
X1A	Clock	Subclock Oscillator output pin
ZINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin

Pin no.	I/O circuit type*	Pin name
39	K	P08_7 / AN23 / PPG7_B
40	K	P09_0 / AN24 / PPG8_R
41	K	P09_1 / AN25 / PPG9_R
42	K	P09_2 / AN26 / PPG10_R
43	K	P09_3 / AN27 / PPG11_R
44	H	P17_1 / PPG12_R
45	H	P17_2 / PPG13_R
46	I	P10_0 / SIN2 / TIN3 / AN28 / INT11
47	H	P10_1 / SOT2 / TOT3
48	M	P10_2 / SCK2 / PPG6
49	H	P10_3 / PPG7
50	Supply	Vcc
51	Supply	Vss
52	O	DEBUG I/F
53	H	P17_0
54	C	MD
55	A	X0
56	A	X1
57	Supply	Vss
58	B	P04_0 / X0A
59	B	P04_1 / X1A
60	C	RSTX
61	H	P11_0
62	H	P11_1 / PPG0_R
63	H	P11_2 / PPG1_R
64	H	P11_3 / PPG2_R
65	H	P11_4 / PPG3_R
66	H	P11_5 / PPG4_R
67	H	P11_6 / FRCK0_R / ZIN1
68	H	P11_7 / IN0_R / AIN1
69	H	P12_0 / IN1_R / BIN1
70	H	P12_3 / OUT2_R
71	H	P12_7 / INT1_R
72	H	P00_0 / INT3_R / FRCK2
73	H	P00_1 / INT4_R
74	H	P00_2 / INT5_R
75	Supply	Vcc
76	Supply	Vss
77	H	P00_3 / INT6_R / PPG8_B

Type	Circuit	Remarks
I	 Pull-up control Pout Nout Standby control for input shutdown R Hysteresis input Analog input	• CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor • Analog input
K	 Pull-up control Pout Nout Standby control for input shutdown R Automotive input Analog input	• CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • Automotive input with input shutdown function • Programmable pull-up resistor • Analog input
M	 Pull-up control Pout Nout Standby control for input shutdown R Hysteresis input Analog input	• CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

MB96640		
Pin Number	USART Number	Normal Function
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
46	USART2	SIN2
47		SOT2
48		SCK2
86	USART4	SIN4
87		SOT4
88		SCK4

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
40	35C _H	PPG2	Yes	40	Programmable Pulse Generator 2
41	358 _H	PPG3	Yes	41	Programmable Pulse Generator 3
42	354 _H	PPG4	Yes	42	Programmable Pulse Generator 4
43	350 _H	PPG5	Yes	43	Programmable Pulse Generator 5
44	34C _H	PPG6	Yes	44	Programmable Pulse Generator 6
45	348 _H	PPG7	Yes	45	Programmable Pulse Generator 7
46	344 _H	PPG8	Yes	46	Programmable Pulse Generator 8
47	340 _H	PPG9	Yes	47	Programmable Pulse Generator 9
48	33C _H	PPG10	Yes	48	Programmable Pulse Generator 10
49	338 _H	PPG11	Yes	49	Programmable Pulse Generator 11
50	334 _H	PPG12	Yes	50	Programmable Pulse Generator 12
51	330 _H	PPG13	Yes	51	Programmable Pulse Generator 13
52	32C _H	PPG14	Yes	52	Programmable Pulse Generator 14
53	328 _H	PPG15	Yes	53	Programmable Pulse Generator 15
54	324 _H	-	-	54	Reserved
55	320 _H	-	-	55	Reserved
56	31C _H	-	-	56	Reserved
57	318 _H	-	-	57	Reserved
58	314 _H	RLT0	Yes	58	Reload Timer 0
59	310 _H	RLT1	Yes	59	Reload Timer 1
60	30C _H	RLT2	Yes	60	Reload Timer 2
61	308 _H	RLT3	Yes	61	Reload Timer 3
62	304 _H	-	-	62	Reserved
63	300 _H	-	-	63	Reserved
64	2FC _H	RLT6	Yes	64	Reload Timer 6
65	2F8 _H	ICU0	Yes	65	Input Capture Unit 0
66	2F4 _H	ICU1	Yes	66	Input Capture Unit 1
67	2F0 _H	-	-	67	Reserved
68	2EC _H	-	-	68	Reserved
69	2E8 _H	ICU4	Yes	69	Input Capture Unit 4
70	2E4 _H	ICU5	Yes	70	Input Capture Unit 5
71	2E0 _H	ICU6	Yes	71	Input Capture Unit 6
72	2DC _H	ICU7	Yes	72	Input Capture Unit 7
73	2D8 _H	-	-	73	Reserved
74	2D4 _H	ICU9	Yes	74	Input Capture Unit 9
75	2D0 _H	-	-	75	Reserved
76	2CC _H	-	-	76	Reserved
77	2C8 _H	OCU0	Yes	77	Output Compare Unit 0
78	2C4 _H	OCU1	Yes	78	Output Compare Unit 1
79	2C0 _H	OCU2	Yes	79	Output Compare Unit 2
80	2BC _H	OCU3	Yes	80	Output Compare Unit 3
81	2B8 _H	OCU4	Yes	81	Output Compare Unit 4

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
121	218 _H	-	-	121	Reserved
122	214 _H	-	-	122	Reserved
123	210 _H	-	-	123	Reserved
124	20C _H	-	-	124	Reserved
125	208 _H	-	-	125	Reserved
126	204 _H	-	-	126	Reserved
127	200 _H	-	-	127	Reserved
128	1FC _H	-	-	128	Reserved
129	1F8 _H	-	-	129	Reserved
130	1F4 _H	-	-	130	Reserved
131	1F0 _H	-	-	131	Reserved
132	1EC _H	-	-	132	Reserved
133	1E8 _H	FLASHA	Yes	133	Flash memory A interrupt
134	1E4 _H	-	-	134	Reserved
135	1E0 _H	-	-	135	Reserved
136	1DC _H	-	-	136	Reserved
137	1D8 _H	QPRC0	Yes	137	Quad Position/Revolution counter 0
138	1D4 _H	QPRC1	Yes	138	Quad Position/Revolution counter 1
139	1D0 _H	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	1CC _H	-	-	140	Reserved
141	1C8 _H	-	-	141	Reserved
142	1C4 _H	-	-	142	Reserved
143	1C0 _H	-	-	143	Reserved

14.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V _{CC} , AV _{CC}	2.7	-	5.5	V	
		2.0	-	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor at C pin	C _S	0.5	1.0 to 3.9	4.7	μF	1.0μF (Allowance within ± 50%) 3.9μF (Allowance within ± 20%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V _{CC} must use the one of a capacity value that is larger than C _S .

WARNING

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

14.3 DC Characteristics

14.3.1 Current Rating

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes ¹	I _{CCPLL}	V _{CC}	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz	-	27	-	mA	T _A = +25°C
			Flash 0 wait	-	-	37	mA	T _A = +105°C
			(CLKRC and CLKSC stopped)	-	-	38.5	mA	T _A = +125°C
	I _{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz	-	3.5	-	mA	T _A = +25°C
			Flash 0 wait	-	-	8	mA	T _A = +105°C
			(CLKPLL, CLKSC and CLKRC stopped)	-	-	9.5	mA	T _A = +125°C
	I _{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz	-	1.8	-	mA	T _A = +25°C
			Flash 0 wait	-	-	6	mA	T _A = +105°C
			(CLKMC, CLKPLL and CLKSC stopped)	-	-	7.5	mA	T _A = +125°C
	I _{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz	-	0.16	-	mA	T _A = +25°C
			Flash 0 wait	-	-	3.5	mA	T _A = +105°C
			(CLKMC, CLKPLL and CLKSC stopped)	-	-	5	mA	T _A = +125°C
	I _{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz	-	0.1	-	mA	T _A = +25°C
			Flash 0 wait	-	-	3.3	mA	T _A = +105°C
			(CLKMC, CLKPLL and CLKRC stopped)	-	-	4.8	mA	T _A = +125°C

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V _{OH4}	4mA type	4.5V ≤ V _{CC} ≤ 5.5V I _{OH} = -4mA	V _{CC} - 0.5	-	V _{CC}	V	
			2.7V ≤ V _{CC} < 4.5V I _{OH} = -1.5mA					
	V _{OH3}	3mA type	4.5V ≤ V _{CC} ≤ 5.5V I _{OH} = -3mA	V _{CC} - 0.5	-	V _{CC}	V	
			2.7V ≤ V _{CC} < 4.5V I _{OH} = -1.5mA					
"L" level output voltage	V _{OL4}	4mA type	4.5V ≤ V _{CC} ≤ 5.5V I _{OL} = +4mA	-	-	0.4	V	
			2.7V ≤ V _{CC} < 4.5V I _{OL} = +1.7mA					
	V _{OL3}	3mA type	2.7V ≤ V _{CC} < 5.5V I _{OL} = +3mA	-	-	0.4	V	
	V _{OLD}	DEBUG I/F	V _{CC} = 2.7V I _{OL} = +25mA	0	-	0.25	V	
Input leak current	I _{IL}	Pnn_m	V _{SS} < V _I < V _{CC} AV _{SS} , AV _{RL} < V _I < AV _{CC} , AV _{RH}	- 1	-	+ 1	μA	
Pull-up resistance value	R _{PU}	Pnn_m	V _{CC} = 5.0V ±10%	25	50	100	kΩ	
Input capacitance	C _{IN}	Other than C, V _{CC} , V _{SS} , AV _{CC} , AV _{SS} , AV _{RH} , AV _{RL}	-	-	5	15	pF	

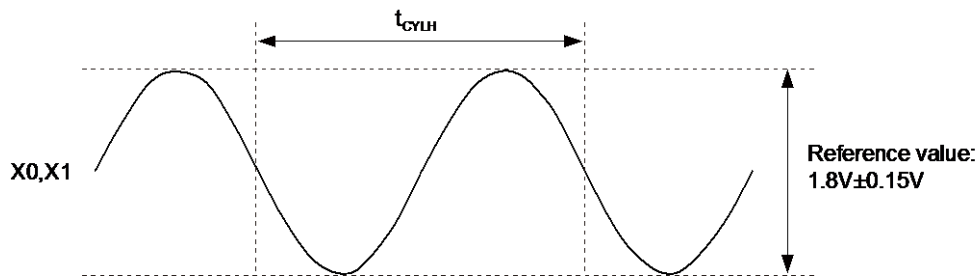
14.4 AC Characteristics

14.4.1 Main Clock Input Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_D = 1.8V \pm 0.15V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$)

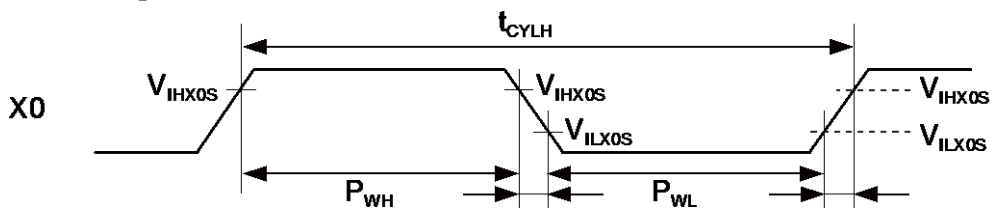
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f_C	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL off
			4	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL on
Input clock cycle	t_{CYLH}	-	125	-	-	ns	
Input clock pulse width	P_{WH}, P_{WL}	-	55	-	-	ns	

When using the crystal oscillator



The amplitude changes by resistance, capacity which added outside or the difference of the device.

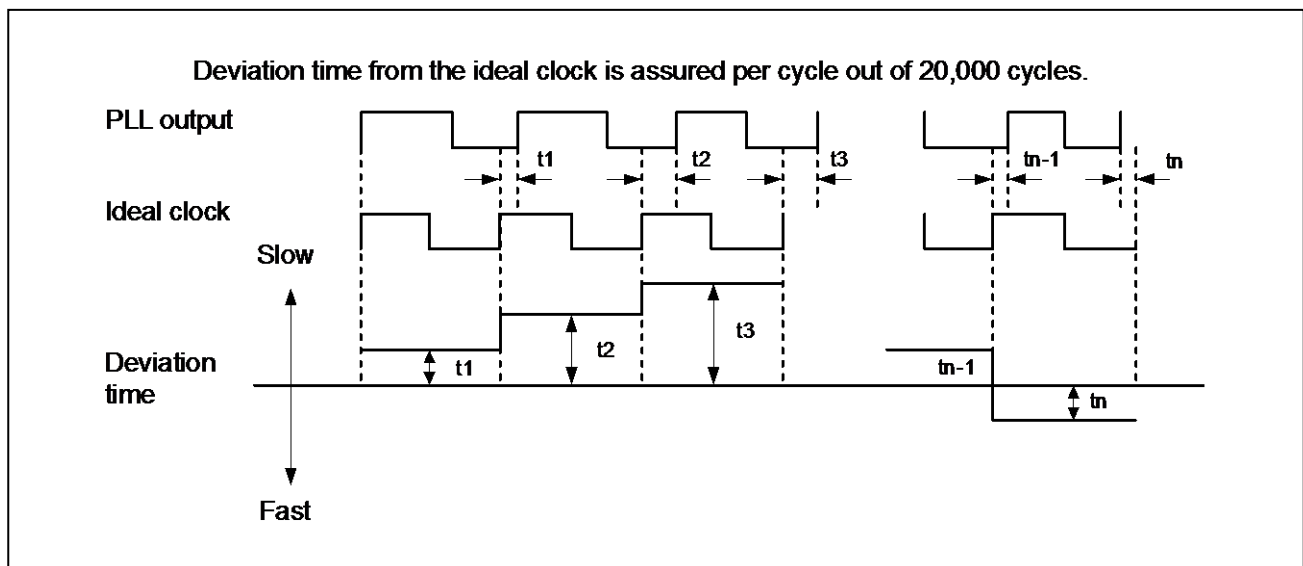
When using the external clock



14.4.5 Operating Conditions of PLL

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

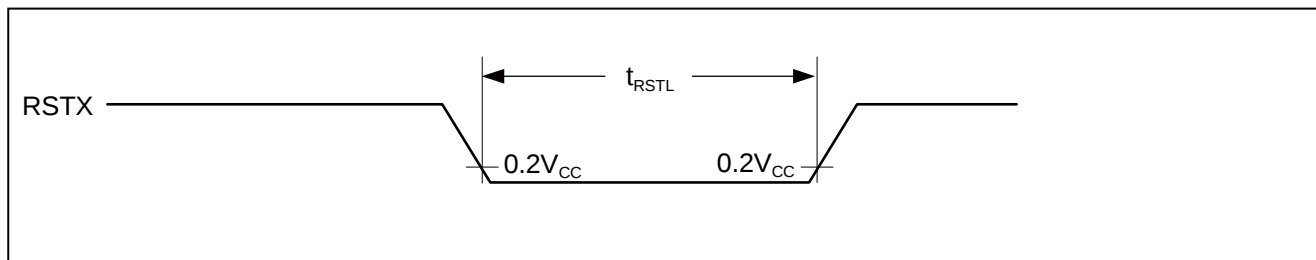
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) $\geq 4MHz$



14.4.6 Reset Input

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

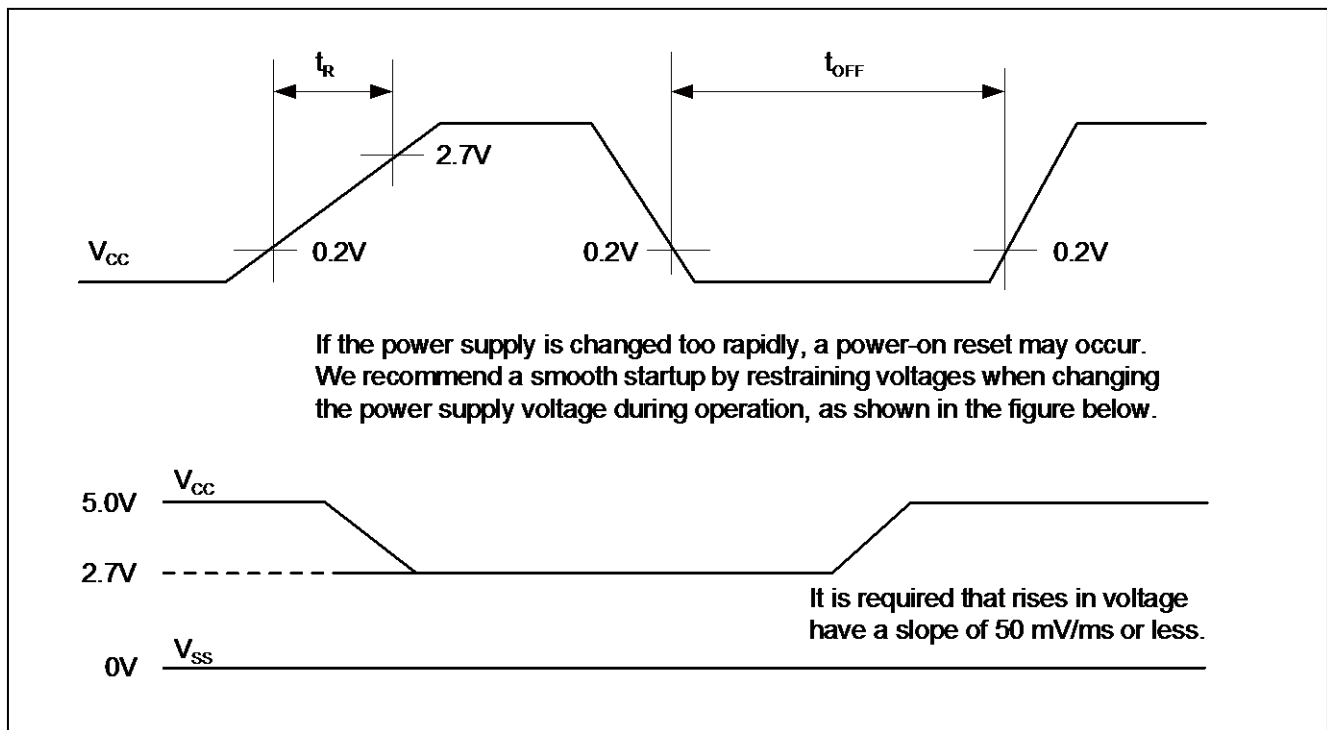
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	μs
Rejection of reset input time			1	-	μs



14.4.7 Power-on Reset Timing

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power on rise time	t_R	VCC	0.05	-	30	ms
Power off time	t_{OFF}	VCC	1	-	-	ms



14.4.8 USART Timing

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, $C_L = 50pF$)

Parameter	Symbol	Pin name	Conditions	$4.5V \leq V_{CC} < 5.5V$		$2.7V \leq V_{CC} < 4.5V$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode	$4t_{CLKP1}$	-	$4t_{CLKP1}$	-	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCKn, SOTn		- 20	+ 20	- 30	+ 30	ns
SOT $\rightarrow$ SCK $\uparrow$ delay time	t_{OVSHI}	SCKn, SOTn		$N \times t_{CLKP1} - 20^*$	-	$N \times t_{CLKP1} - 30^*$	-	ns
SIN $\rightarrow$ SCK $\uparrow$ setup time	t_{IVSHI}	SCKn, SINn		$t_{CLKP1} + 45$	-	$t_{CLKP1} + 55$	-	ns
SCK $\uparrow \rightarrow$ SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKn	External shift clock mode	$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKn		$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVE}	SCKn, SOTn		-	$2t_{CLKP1} + 45$	-	$2t_{CLKP1} + 55$	ns
SIN $\rightarrow$ SCK $\uparrow$ setup time	t_{IVSHE}	SCKn, SINn		$t_{CLKP1}/2 + 10$	-	$t_{CLKP1}/2 + 10$	-	ns
SCK $\uparrow \rightarrow$ SIN hold time	t_{SHIXE}	SCKn, SINn		$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
SCK fall time	t_F	SCKn		-	20	-	20	ns
SCK rise time	t_R	SCKn		-	20	-	20	ns

Notes:

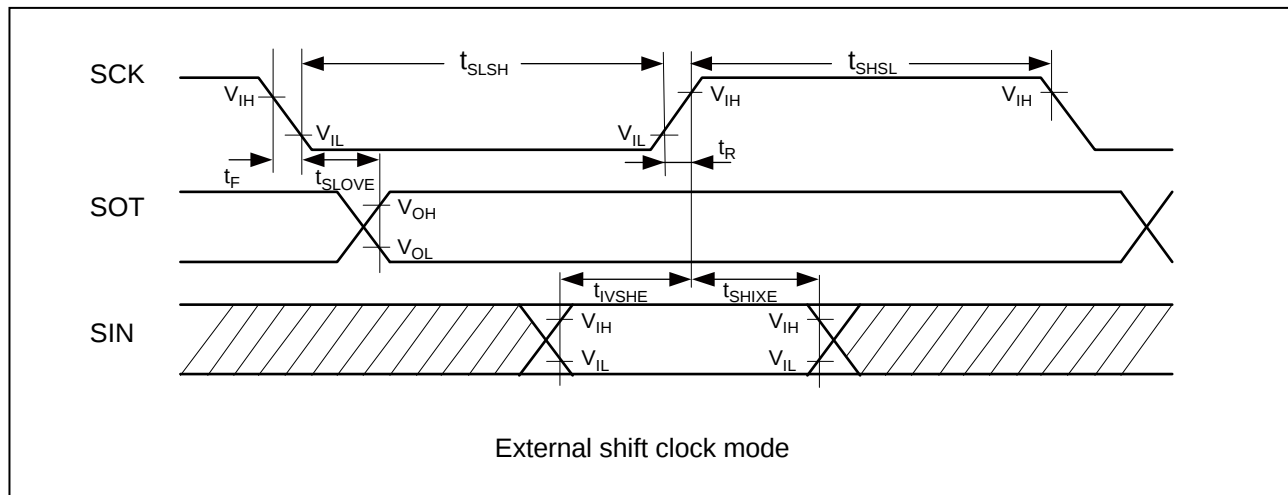
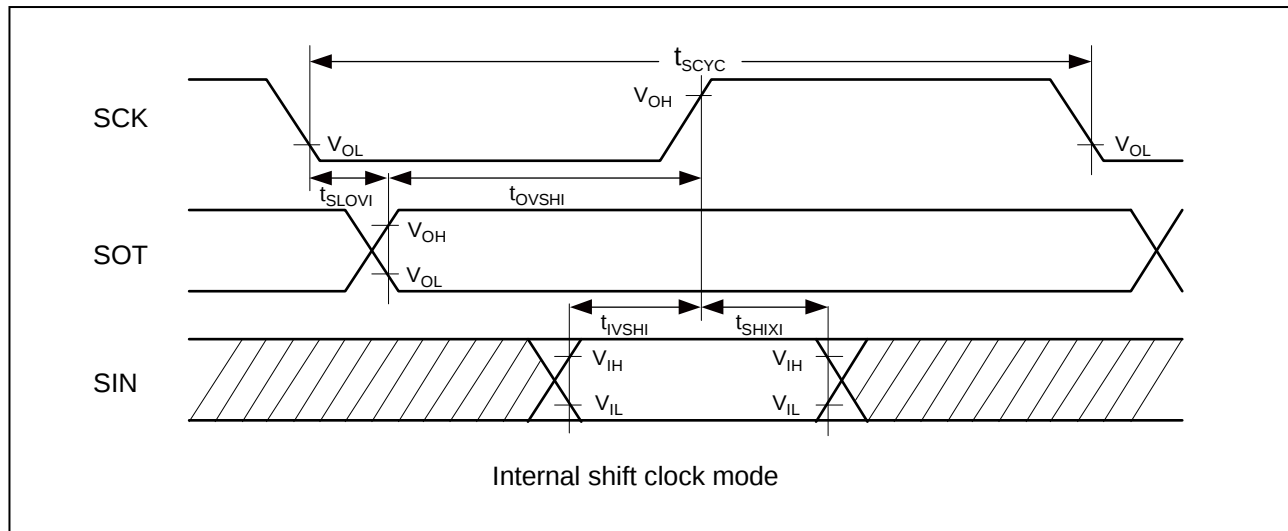
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "MB96600 series HARDWARE MANUAL".
- t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit: ns
- These characteristics only guarantee the same relocate port number.
For example, the combination of SCKn and SOTn_R is not guaranteed.

*: Parameter N depends on t_{SCYC} and can be calculated as follows:

- If $t_{SCYC} = 2 \times k \times t_{CLKP1}$, then $N = k$, where k is an integer > 2
- If $t_{SCYC} = (2 \times k + 1) \times t_{CLKP1}$, then $N = k + 1$, where k is an integer > 1

Examples:

t_{SCYC}	N
$4 \times t_{CLKP1}$	2
$5 \times t_{CLKP1}, 6 \times t_{CLKP1}$	3
$7 \times t_{CLKP1}, 8 \times t_{CLKP1}$	4
...	...



14.4.10 I²C Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode* ⁴		Unit
			Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	C _L = 50pF, R = (V _p /I _{OL})* ¹	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	t _{HDSTA}		4.0	-	0.6	-	μs
SCL clock "L" width	t _{LOW}		4.7	-	1.3	-	μs
SCL clock "H" width	t _{HIGH}		4.0	-	0.6	-	μs
(Repeated) START condition setup time SCL ↑ → SDA ↓	t _{SUSTA}		4.7	-	0.6	-	μs
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}		0	3.45* ²	0	0.9* ³	μs
Data setup time SDA ↓ ↑ → SCL ↑	t _{SUDAT}		250	-	100	-	ns
STOP condition setup time SCL ↑ → SDA ↑	t _{SUSTO}		4.0	-	0.6	-	μs
Bus free time between "STOP condition" and "START condition"	t _{BUS}		4.7	-	1.3	-	μs
Pulse width of spikes which will be suppressed by input noise filter	t _{SP}	-	0	(1-1.5) × t _{CLKP1} * ⁵	0	(1-1.5) × t _{CLKP1} * ⁵	ns

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.

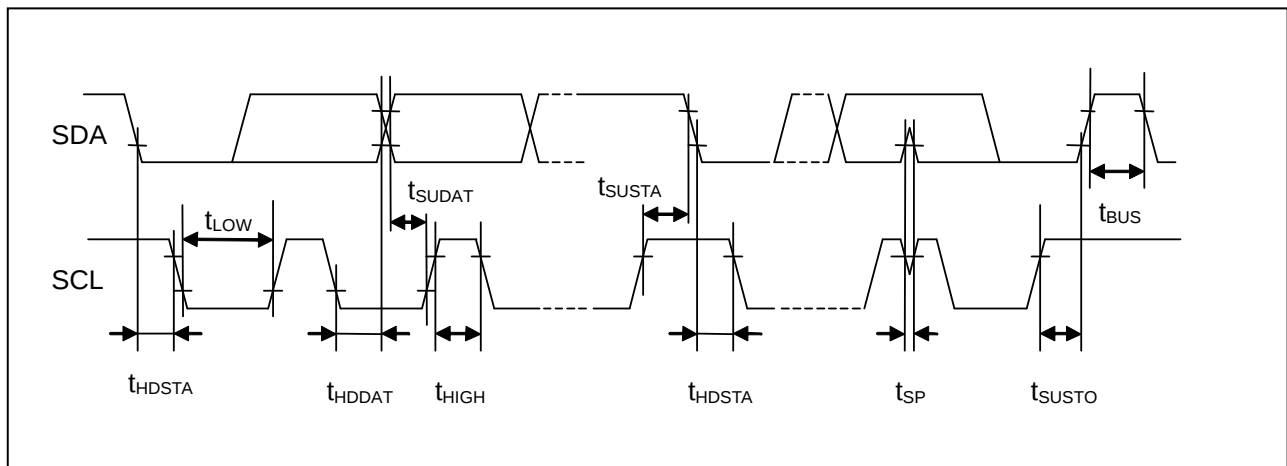
V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

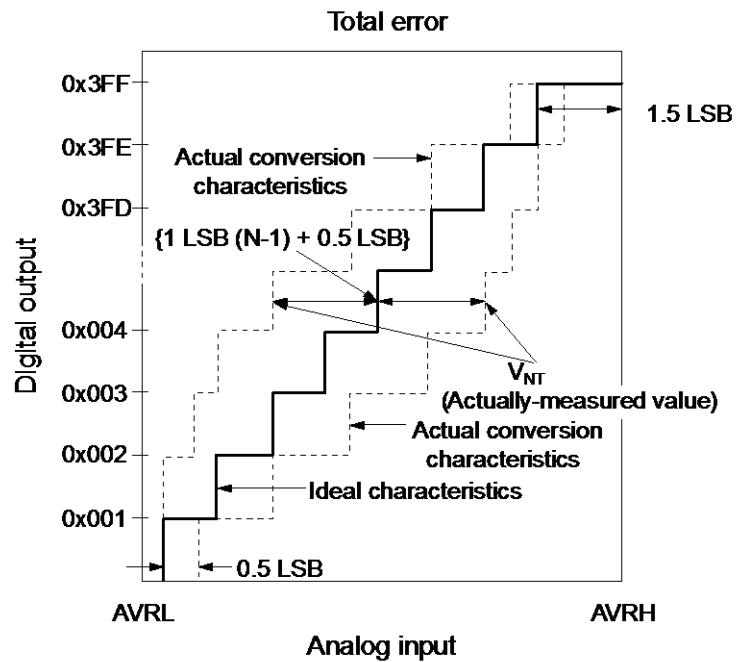
*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250ns".

*4: For use at over 100 kHz, set the peripheral clock1 (CLKP1) to at least 6MHz.

*5: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time.





$$1\text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{\text{NT}} - \{1\text{LSB} \times (\text{N} - 1) + 0.5\text{LSB}\}}{1\text{LSB}}$$

N : A/D converter digital output value.

V_{NT} : Voltage at which the digital output changes from 0x (N + 1) to 0xN.

V_{OT} (Ideal value) = AVRL + 0.5LSB[V]

V_{FST} (Ideal value) = AVRH - 1.5LSB[V]

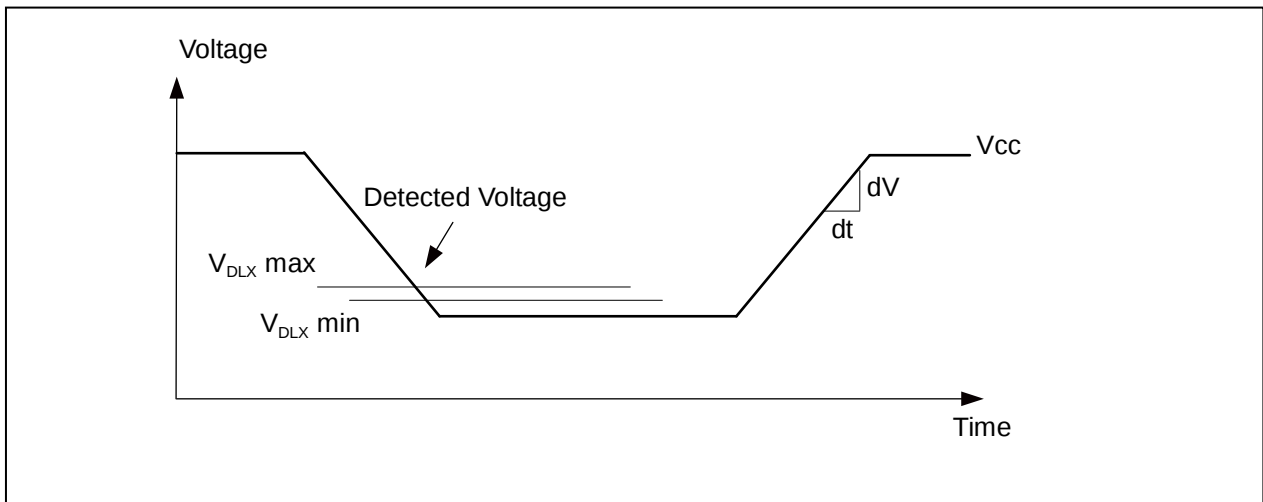
14.6 Low Voltage Detection Function Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Detected voltage ^{*1}	V_{DL0}	CILCR:LVL = 0000 _B	2.70	2.90	3.10	V
	V_{DL1}	CILCR:LVL = 0001 _B	2.79	3.00	3.21	V
	V_{DL2}	CILCR:LVL = 0010 _B	2.98	3.20	3.42	V
	V_{DL3}	CILCR:LVL = 0011 _B	3.26	3.50	3.74	V
	V_{DL4}	CILCR:LVL = 0100 _B	3.45	3.70	3.95	V
	V_{DL5}	CILCR:LVL = 0111 _B	3.73	4.00	4.27	V
	V_{DL6}	CILCR:LVL = 1001 _B	3.91	4.20	4.49	V
Power supply voltage change rate ^{*2}	dV/dt	-	- 0.004	-	+ 0.004	V/ μ s
Hysteresis width	V_{HYS}	CILCR:LVHYS=0	-	-	50	mV
		CILCR:LVHYS=1	80	100	120	mV
Stabilization time	$T_{LVDSTAB}$	-	-	-	75	μ s
Detection delay time	t_d	-	-	-	30	μ s

*1: If the power supply voltage fluctuates within the time less than the detection delay time (t_d), there is a possibility that the low voltage detection will occur or stop after the power supply voltage passes the detection range.

*2: In order to perform the low voltage detection at the detection voltage (V_{DLX}), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.



14.7 Flash Memory Write/Erase Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	$T_A \leq +105^{\circ}C$	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	$T_A \leq +105^{\circ}C$	-	25	400	μs	Not including system-level overhead time.
	Small Sector	-	-	25	400	μs	
Chip erase time		$T_A \leq +105^{\circ}C$	-	11.51	55.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage ($-0.004V/\mu s$ to $+0.004V/\mu s$) after the external power falls below the detection voltage (V_{DLX})^{*1}.

Write/Erase cycles and data hold time

Write/Erase cycles (cycle)	Data hold time (year)
1,000	20^{*2}
10,000	10^{*2}
100,000	5^{*2}

*1: See "14.6 Low Voltage Detection Function Characteristics".

*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at $+85^{\circ}C$).

15. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

■ MB96F647

