Dave Embedded Systems - DXLH5290I Datasheet

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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Active
Module/Board Type	MPU Core
Core Processor	ARM® Cortex®-A9, i.MX6 Quad
Co-Processor	-
Speed	1GHz
Flash Size	512MB (NAND), 32MB (NOR)
RAM Size	2GB
Connector Type	SO-DIMM-204
Size / Dimension	-
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/dave-embedded-systems/dxlh5290i

Table of Contents

1 Preface

1.1 About this manual

This Hardware Manual describes the **AXEL LITE** CPU module design and functions.
Precise specifications for the Freescale i.MX6 processor can be found in the CPU datasheets and/or reference manuals.

1.2 Copyrights/Trademarks

1.3 Standards

DAVE Embedded Systems is certified to ISO 9001 standards.

1.4 Disclaimers

DAVE Embedded Systems does not assume any responsibility about availability, supplying and support regarding all the products mentioned in this manual that are not strictly part of the **AXEL LITE** CPU module.
AXEL LITE CPU Modules are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. **DAVE Embedded Systems** customers who are using or selling these products for use in such applications do so at their own risk and agree to fully indemnify **DAVE Embedded Systems** for any damage resulting from such improper use or sale.

1.5 Warranty

AXEL LITE is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, **DAVE Embedded Systems** will at its discretion decide to repair

2 Introduction

AXEL LITE is the new top-class Single - Dual - Quad Core ARM Cortex-A9 CPU module by DAVE Embedded Systems, based on the recent NXP i.MX6 application processor. Thanks to **AXEL LITE**, customers have the chance to save time and resources by using a compact solution that permits to reach scalable performances that perfectly fits the application requirements avoiding complexities on the carrier board. The use of this processor enables extensive system-level differentiation of new applications in many industry fields, where high-performance and extremely compact form factor (67,5 mm x 43 mm) are key factors. Smarter system designs are made possible, following the trends in functionalities and interfaces of the new, state-of-the-art embedded products.

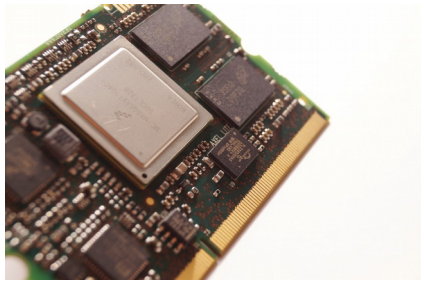


Fig. 1: AXEL-LITE- Powered by I.MX6 processor

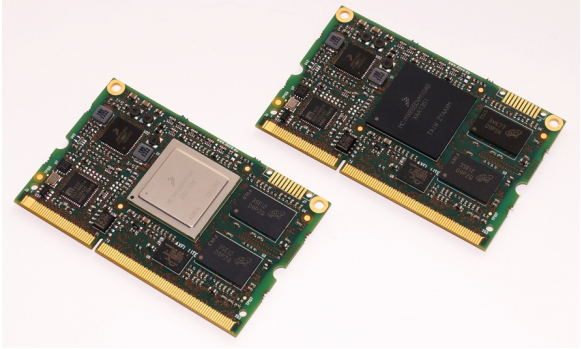


Fig. 2: AXEL-LITE – Solo / Dual / Quad core ARM Cortex A9

AXEL LITE enables designers to create smart products suitable for harsh mechanical and thermal environments, allowing the development of high computing and reliable solutions. Thanks to the tight integration between the ARM Core-based processing system, designers are able to share the application through the multi-core platform and/or to divide the task on different cores in order to match with specific application requirements (thanks to AMP is possible to create application where RTOS and Linux works together on different cores). **AXEL LITE** is designed in order to keep full compatibility

2.1 Product Highlights

- Unmatched performances thanks to Solo / Dual / Quad Core @ 1.2 GHz
- All memories you need on-board
- Boot from NOR for safe applications
- Enabling massive computing applications thanks to wide range DDR3 RAM memory up to 2GB
- Single 3V3 Power Supply
- Reduced carrier complexity: SDIO, dual CAN, USB, Ethernet with on-board PHY, GPIOs
- Multiple video outputs available
- H264 Video encoding and decoding
- Multiple video inputs available

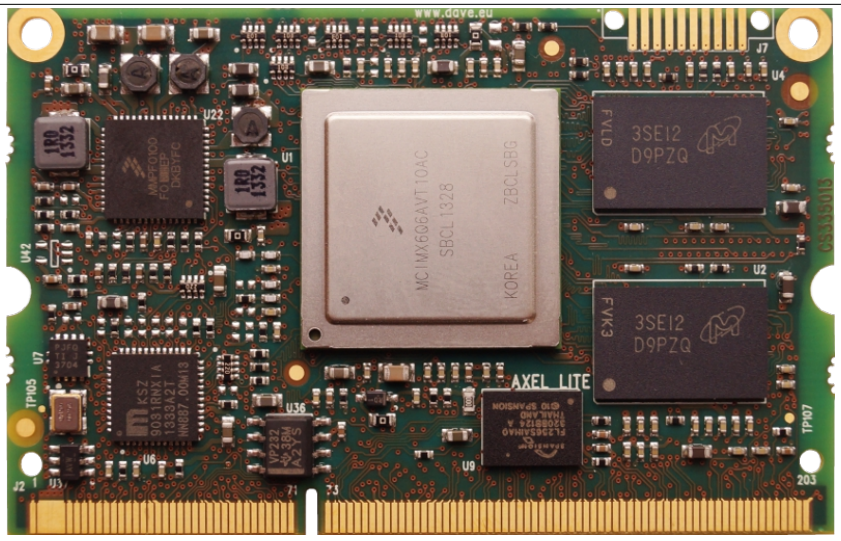


Fig. 3: AXEL LITE SOM (top view)

- Video and night vision equipment
- Multimedia-focused products
- Entertainment and gaming appliances

The i.MX6 application processor is composed of the following major functional blocks:

- ARM Cortex-A9 MPCore 2x/4x CPU Processor, featuring:
  - 1 Megabyte unified L2 cache shared by all CPU cores
  - NEON MPE co-processor
  - General Interrupt Controller (GIC) with 128 interrupt support
  - Snoop Control Unit (SCU)
  - External memories interconnect
- Hardware accelerators, including:
  - VPU -Video Processing Unit
  - Two IPUv3H -Image Processing Unit (version 3H)
  - 2D/3D/Vector graphics accelerators
- Connectivity peripherals, including
  - PCIe
  - SATA
  - SD/SDIO/MMC
  - Serial buses: USB, UART, I²C, SPI, ...

Size min	16 MByte
Size max	64 MByte
Chip select	ECSPI1_SS0
Bootable	Yes

Tab. 8: NOR flash specifications

For **AXEL LITE** models that have the NOR flash bank populated, the eCSPI channel 1 is mapped by design on the following multiplexed pins:

NOR signal	Function	I.MX6 signal	I.MX6 ball #
NOR_CS0n	Chip select	EIM_EB2	E22
NOR_DQ0/MOSI	Serial Input	EIM_D18	D24
NOR_DQ1/MISO	Serial Output	EIM_D17	F21
NOR_SCLQ	Serial clock	EIM_D16	C25

Tab. 9: eCSPI1 pin mapping

3.4 NAND flash bank

On board main storage memory is a 8-bit wide NAND flash connected to the CPU's Raw NAND flash controller. Optionally, it can act as boot peripheral.
The following table reports the NAND flash specifications:

CPU connection	Raw NAND flash controller
Page size	512 byte, 2 kbyte or 4 kbyte
Size min	128 MByte
Size max	2 GByte
Width	8 bit
Chip select	NANDF_CS0
Bootable	Yes

Tab. 10: NAND flash specifications

3.5 Memory Map

For detailed information, please refer to chapter 2 “Memory Maps” of the i.MX Applications Processor Reference Manual.

The PSU is composed of two main blocks:

- power management integrated circuit (PMIC, NXP PF0100E0 - on request this part is available in automotive grade)
- additional generic power management circuitry that completes PMIC functionalities.

The PSU:

- generates the proper power-up sequence required by i.MX processor and surrounding memories and peripherals
- synchronizes the powering up of carrier board in order to prevent back power
- provides some spare regulated voltages that can be used to power carrier board devices

5.1.1 Power-up sequence

The typical power-up sequence is the following:

1. (optional) PMIC_LICELL is powered
2. 3.3VIN main power supply rail is powered
3. CPU_PORn (active-low) is driven low
4. PMIC activates PMIC_VSNVS power output
5. PMIC_PWRON signal is pulled-up (unless carrier board circuitry keeps this signal low for any reason)
6. PMIC transitions from OFF to ON state
7. PMIC initiates power-up sequence needed by MX6 processor
8. BOARD_PGOOD signal is raised; this active-high signal indicates that SoM's I/O is powered. This signal can be used to manage carrier board power up sequence in order to prevent back powering (from SoM to carrier board or vice versa)
9. CPU_PORn is released.

5.1.2 Power rails and related signals

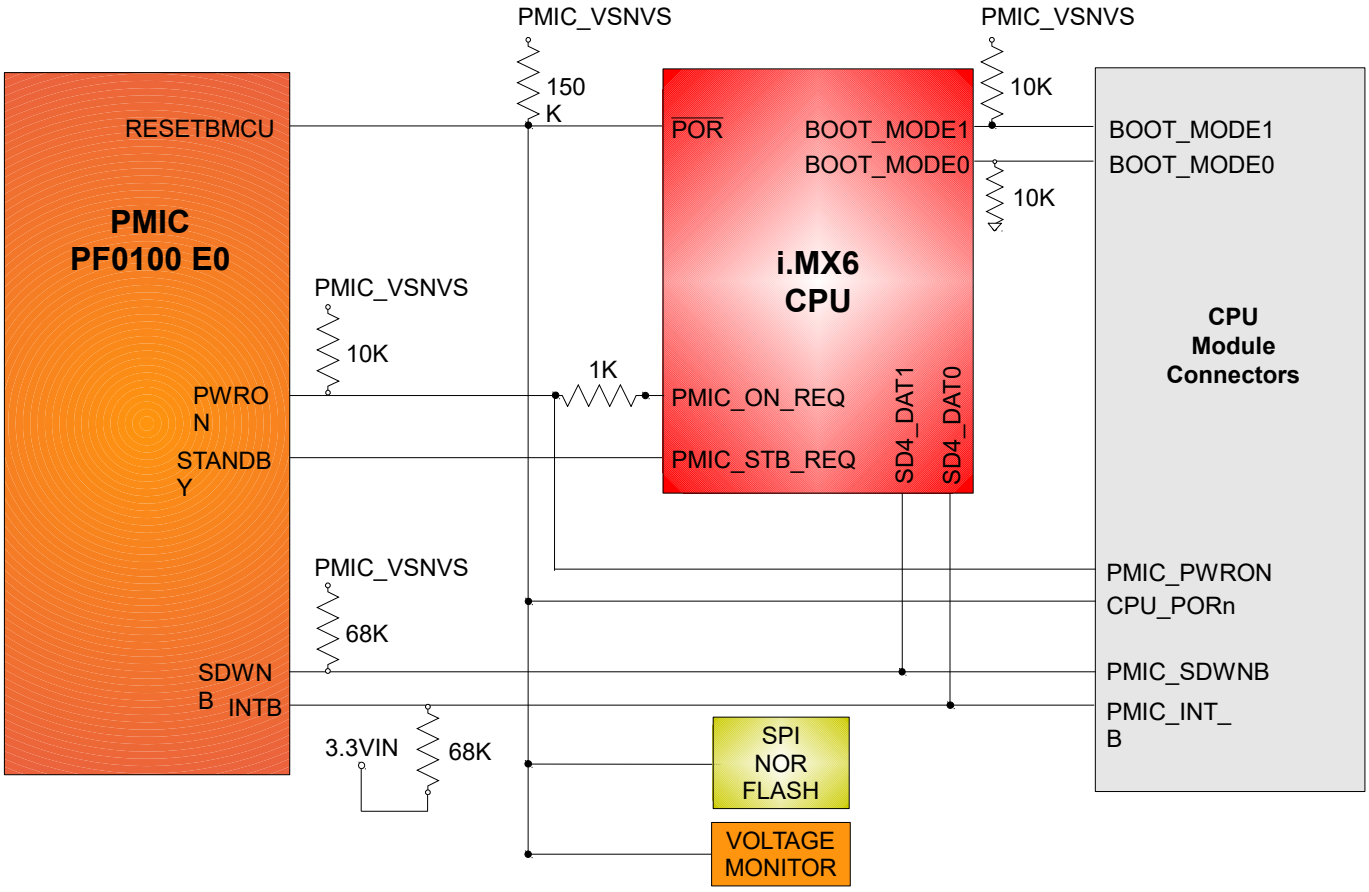
The following list describes in detail power rails and power related signals. **Please note that PMIC regulators output voltages can be changed only if explicitly allowed.**

- 3.3VIN: this is external main power rail. Voltage range is 3.3V ±5%
- PMIC_CELL: PMIC's coin cell supply input/output
- BOARD_PGOOD: this output signal is used to indicate when carrier board's circuitry interfacing **AXEL LITE**'s I/Os has to be powered up

For further details, please refer to the PMIC documentation: *http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MMPF0100%7CPF0100*

5.2 Reset scheme and control signals

The following picture shows the simplified block diagram of reset scheme and voltage monitoring.



The available reset signals are described in detail in the following sections.

5.2.1 CPU_PORn

The following devices can assert this active-low signal:

- PMIC
- multiple-voltage monitor: this device monitors several critical power voltages and triggers a reset pulse in case any of these exhibits a brownout

recovery operations. For further information on how to use the JTAG interface, please contact the Technical Support Team.

5.5.2 USB Recovery

The USB Serial Downloader provides a means to download the bootloader image to the chip over USB serial connection. Please refer to the XELK Quick Start Guide for further details.

5.5.3 SD/MMC Recovery

MMC recovery is a valuable options that requires no special hardware at all, apart a properly formatted MMC. When SD/MMC boot option is selected, bootrom looks for a valid bootloader on SD/MMC. Once the board is running after booting from SD, reprogramming the flash memory is straightforward. The SD peripheral used for boot is MMC/SD/SDIO1 (please refer to 7.11.1).

5.6 Multiplexing

Most of the i.MX 6 processor pins have multiple signal options. These signal to pin and pin to signal options are selected by the input output multiplexer called IOMUX. The IOMUX enables flexible IO multiplexing and is also used to configure other pin characteristics, such as voltage level, drive strength, and hysteresis. Each IO pad has default and up to seven alternate functions, which are software configurable.

Please refer to the following sections of the i.MX6 APRM for further information pin assignment:

- chapter 4 “External Signals and Pin Multiplexing”
- section 4.1 “Pin assignments”
- section 4.2 “Muxing options”
- chapter 36 “IOMUX Controller (IOMUXC)”

J2 – ODD [1-203]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.53	SD3_DATA7	CPU.SD3_DATA7	F13				
J2.55	SD3_CMD	CPU.SD3_CMD	B13				
J2.57	DGND	DGND	-				
J2.59	SD3_CLK	CPU.SD3_CLK	D14				
J2.61	SD2_DATA0	CPU.SD2_DATA0	A22				
J2.63	SD2_DATA1	CPU.SD2_DATA1	E20				
J2.65	SD2_DATA2	CPU.SD2_DATA2	A23				
J2.67	SD2_DATA3	CPU.SD2_DATA3	B22				
J2.69	SD2_CMD	CPU.SD2_CMD	F19				
J2.71	SD2_CLK	CPU.SD2_CLK	C21				
J2.73	DGND	DGND	-				
J2.75	SD1_DAT0	CPU.SD1_DAT0	A21	NVCC_			
J2.77	SD1_DAT1	CPU.SD1_DAT1	C20	NVCC_			
J2.79	SD1_DAT2	CPU.SD1_DAT2	E19	NVCC_			
J2.81	SD1_DAT3	CPU.SD1_DAT3	F18	NVCC_			
J2.83	SD1_CMD	CPU.SD1_CMD	B21	NVCC_			
J2.85	SD1_CLK	CPU.SD1_CLK	D20	NVCC_			
J2.87	DGND	DGND	-				
J2.89	KEY_COL0/ECSPI1_SCLK	CPU.KEY_COL0	W5				Not available as ECSPI1 signals on AXEL LITE's models which mount the NOR SPI flash. For further details, please refer to section 3.3.
J2.91	KEY_ROW0/ECSPI1_MOSI	CPU.KEY_ROW0	V6				
J2.93	KEY_COL1/ECSPI1_MISO	CPU.KEY_COL1	U7				
J2.95	KEY_ROW1/ECSPI1_SS0	CPU.KEY_ROW1	U6				
J2.97	KEY_COL2/ECSPI1_SS1	CPU.KEY_COL2	W6				
J2.99	KEY_ROW2	CPU.KEY_ROW2	W4				
J2.101	KEY_COL3/I2C2_SCL	CPU.KEY_COL3	U5				Used internally. Please refer to 7.8.2.
J2.103	KEY_ROW3/I2C2_SDA	CPU.KEY_ROW3	T7				Used internally. Please refer to 7.8.2.
J2.105	KEY_COL4	CPU.KEY_COL4	T6				
J2.107	KEY_ROW4	CPU.KEY_ROW4	V5				
J2.109	DGND	DGND	-				
J2.111	HDMI_CLKN	CPU.HDMI_CLKN	J5				
J2.113	HDMI_CLKP	CPU.HDMI_CLKP	J6				
J2.115	HDMI_D0N	CPU.HDMI_D0N	K5				

J2 – EVEN [2-204]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.12	DGND	DGND	-				
J2.14	PMIC_LICELL	PMIC.LICELL	42				
J2.16	CPU_ONOFF	CPU.CPU_ONOFF	D12				
J2.18	BOARD_PGOOD		-				
J2.20	BOOT_MODE_SEL	BOOT MODE SELECTION	-				
J2.22	CPU_PORN	CPU.CPU_PORN	C11				
J2.24	PMIC_PWRON	PMIC.PWRON	56				
J2.26	GPIO_0	CPU.GPIO_0	T5				
J2.28	GPIO_1	CPU.GPIO_1	T4				
J2.30	DGND	DGND	-				
J2.32	GPIO_2	CPU.GPIO_2	T1				
J2.34	GPIO_3/I2C3_SCL	CPU.GPIO_3	R7				
J2.36	GPIO_4	CPU.GPIO_4	R6				
J2.38	GPIO_5	CPU.GPIO_5	R4				
J2.40	GPIO_6/I2C3_SDA	CPU.GPIO_6	T3				
J2.42	GPIO_7//FLEXCAN1_H	CPU.GPIO_7	R3				Mount option. Please refer to section 7.9.1.
J2.44	GPIO_8//FLEXCAN1_L	CPU.GPIO_8	R5				Mount option. Please refer to section 7.9.1.
J2.46	GPIO_9	CPU.GPIO_9	T2				
J2.48	GPIO_16	CPU.GPIO_16	R2				
J2.50	GPIO_17	CPU.GPIO_17	R1				
J2.52	GPIO_18	CPU.GPIO_18	P6				
J2.54	GPIO_19	CPU.GPIO_19	P5				
J2.56	DGND	DGND	-				
J2.58	CSI0_PIXCLK	CPU.CSI0_PIXCLK	P1				
J2.60	CSI0_MCLK	CPU.CSI0_MCLK	P4				
J2.62	CSI0_VSYNC	CPU.CSI0_VSYNC	N2				
J2.64	CSI0_DATA_EN	CPU.CSI0_DATA_EN	P3				
J2.66	CSI0_DAT4	CPU.CSI0_DAT4	N1				
J2.68	CSI0_DAT5	CPU.CSI0_DAT5	P2				
J2.70	CSI0_DAT6	CPU.CSI0_DAT6	N4				
J2.72	CSI0_DAT7	CPU.CSI0_DAT7	N3				
J2.74	CSI0_DAT8	CPU.CSI0_DAT8	N6				

J2 – EVEN [2-204]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.140	DISP0_DAT3	CPU.DISP0_DAT3	P21	NVCC_			
J2.142	DISP0_DAT4	CPU.DISP0_DAT4	P20	NVCC_			
J2.144	DISP0_DAT5	CPU.DISP0_DAT5	R25	NVCC_			
J2.146	DGND	DGND	-				
J2.148	DISP0_DAT6	CPU.DISP0_DAT6	R23	NVCC_			
J2.150	DISP0_DAT7	CPU.DISP0_DAT7	R24	NVCC_			
J2.152	DISP0_DAT8	CPU.DISP0_DAT8	R22	NVCC_			
J2.154	DISP0_DAT9	CPU.DISP0_DAT9	T25	NVCC_			
J2.156	DISP0_DAT10	CPU.DISP0_DAT10	R21	NVCC_			
J2.158	DISP0_DAT11	CPU.DISP0_DAT11	T23	NVCC_			
J2.160	DISP0_DAT12	CPU.DISP0_DAT12	T24	NVCC_			
J2.162	DISP0_DAT13	CPU.DISP0_DAT13	R20	NVCC_			
J2.164	DGND	DGND	-				
J2.166	DISP0_DAT14	CPU.DISP0_DAT14	U25	NVCC_			
J2.168	DISP0_DAT15	CPU.DISP0_DAT15	T22	NVCC_			
J2.170	DISP0_DAT16	CPU.DISP0_DAT16	T21	NVCC_			
J2.172	DISP0_DAT17	CPU.DISP0_DAT17	U24	NVCC_			
J2.174	DISP0_DAT18	CPU.DISP0_DAT18	V25	NVCC_			
J2.176	DISP0_DAT19	CPU.DISP0_DAT19	U23	NVCC_			
J2.178	DISP0_DAT20	CPU.DISP0_DAT20	U22	NVCC_			
J2.180	DISP0_DAT21	CPU.DISP0_DAT21	T20	NVCC_			
J2.182	DISP0_DAT22	CPU.DISP0_DAT22	V24	NVCC_			
J2.184	DISP0_DAT23	CPU.DISP0_DAT23	W24	NVCC_			
J2.186	USB_OTG_VBUS	CPU.USB_OTG_VBUS	E9	NVCC_			
J2.188	USB_H1_VBUS	CPU.USB_H1_VBUS	D10	NVCC_			
J2.190	DGND	DGND	-				
J2.192	ENET_RX_ER	CPU.ENET_RX_ER	W23				
J2.194	ENET_RXD0	CPU.ENET_RXD0	W21				
J2.196	USB_OTG_DN	CPU.USB_OTG_DN	B6	NVCC_			
J2.198	USB_OTG_DP	CPU.USB_OTG_DP	A6	NVCC_			
J2.200	USB_HOST_DP	CPU.USB_HOST_DP	E10	NVCC_			
J2.202	USB_HOST_DN	CPU.USB_HOST_DN	F10	NVCC_			

7 Peripheral interfaces

AXEL LITE modules implement a number of peripheral interfaces through the SO-DIMM connector. The following notes apply to those interfaces:

- Some interfaces/signals are available only with/without certain configuration options of the **AXEL LITE** module. Each signal's availability is noted in the "Notes" column on the table of each interface.

- The peripherals described in the following sections represent the default configuration for the **AXEL LITE** SOM, which match with the features provided by the electronics implemented on the module.

The signals for each interface are described in the related tables. The following notes summarize the column headers for these tables:

- "Pin name" – The symbolic name of each signal
- "Conn. Pin" – The pin number on the module connectors
- "Function" – Signal description
- "Notes" – This column summarizes configuration requirements and recommendations for each signal.

7.1 Notes on pin assignment

For further information, please refer to section 5.6 "Multiplexing".

7.2 Gigabit Ethernet

On-board Ethernet PHY (Micrel KSZ9031RNX) provides interface signals required to implement the 10/100/1000 Mbps Ethernet port. The transceiver is connected to the triple speed Ethernet MAC (ENET module) through RGMII interface.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ETH0_TXRX0_P	J2.19	Media Dependent Interface[0], positive pin	

7.6.3 UART3

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART3_CTS	J2.185 J2.199 J2.45	Clear to send	
UART3_RTS	J2.201 J2.37	Request to send	
UART3_RX_DATA	J2.189	Serial/infrared data receive	
UART3_TX_DATA	J2.187	Serial/infrared data transmit	

7.6.4 UART4

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART4_RX_DATA	J2.91	Serial/infrared data receive	
UART4_TX_DATA	J2.89	Serial/infrared data transmit	

7.6.5 UART5

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART5_CTS	J2.107	Clear to send	
UART5_RTS	J2.105	Request to send	
UART5_RX_DATA	J2.95	Serial/infrared data receive	
UART5_TX_DATA	J2.93	Serial/infrared data transmit	

7.7 SPI

AXEL LITE provides up to five SPI ports connected to the I.MX6 integrated Enhanced Configurable SPI (ECSPI) controller, featuring:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Up to four Chip Select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Configurable Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK)
- Direct Memory Access (DMA) support

7.7.1 ECSPI1

AXEL LITE on-board bootable SPI Flash is interfaced with the i.MX6 SoC through the eCSPI1 port on chip select 0. For further details, please refer to Section 3.3.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ECSPI1_MISO	J2.93 J2.70 J2.182	Master data in; slave data out	
ECSPI1_MOSI	J2.91 J2.68 J2.180	Master data out; slave data in	
ECSPI1_RDY	J2.54	Data ready signal	
ECSPI1_SCLK	J2.89 J2.66 J2.178	Clock signal	
ECSPI1_SS0	J2.95 J2.72 J2.184	Chip select 0 signal	
ECSPI1_SS1	J2.97	Chip select 1 signal	

Pin name	Conn. Pin	Function	Notes
	J2.168 J2.177		
ECSPI1_SS2	J2.99 J2.187	Chip select 2 signal	
ECSPI1_SS3	J2.101 J2.189	Chip select 3 signal	

7.7.2 ECSPI2

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ECSPI2_MISO	J2.78 J2.172	Master data in; slave data out	
ECSPI2_MOSI	J2.76 J2.170	Master data out; slave data in	
ECSPI2_SCLK	J2.74 J2.176	Clock signal	
ECSPI2_SS0	J2.80 J2.174	Chip select 0 signal	
ECSPI2_SS1	J2.168	Chip select 1 signal	
ECSPI2_SS2	J2.187	Chip select 2 signal	
ECSPI2_SS3	J2.189	Chip select 3 signal	

7.7.3 ECSPI3

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ECSPI3_MISO	J2.138	Master data in; slave data out	
ECSPI3_MOSI	J2.136	Master data out; slave data in	
ECSPI3_RDY	J2.150	Data ready signal	
ECSPI3_SCLK	J2.134	Clock signal	
ECSPI3_SS0	J2.140	Chip select 0 signal	

Pin name	Conn. Pin	Function	Notes
	J2.63		
ECSPI5_SS1	J2.79 J2.65	Chip select 1 signal	
ECSPI5_SS2	J2.81	Chip select 2 signal	
ECSPI5_SS3	J2.67	Chip select 3 signal	

7.8 I²C

Three I²C channels are available on **AXEL LITE** to provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus™) specification version 2.1. The I²C ports support standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s).

7.8.1 I²C1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
I2C1_SCL	J2.76 J2.181	I2C clock	
I2C1_SDA	J2.74 J2.195	I2C data	

7.8.2 I²C2

The I²C2 bus is used for connecting the i.MX6 SOC to the PMIC. The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
I2C2_SCL	J2.101	I2C clock	
I2C2_SDA	J2.103	I2C data	

7.8.3 I²C3

The following table describes the interface signals:

7.9.2 FLEXCAN2

When required, FLEXCAN2 must be connected to an external PHY on the carrier board.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
FLEXCAN2_RX	J2.107 J2.41	Receive data pin	
FLEXCAN2_TX	J2.105 J2.39	Transmit data pin	

7.10 JTAG

The i.MX6 provides debug access via a standard JTAG (IEEE 1149.1) debug interface. The signals are routed to the on-board J7 connector. The connector is placed on the top side of the PCB, at the upper-right corner (please see the picture below).

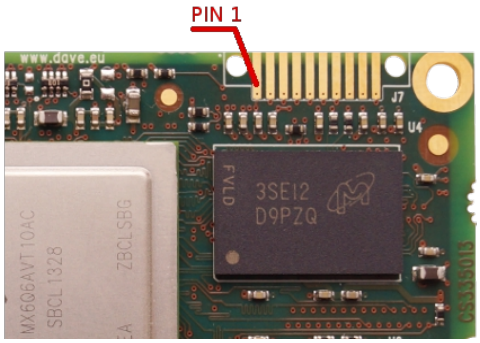


Fig. 6: On board JTAG connector J7

J7 footprint mates with Samtec FSI-110-03-G-S connector. The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
JTAG_TDO	J7.4	JTAG TDO	On board connector
JTAG_TDI	J7.5	JTAG TDI	On board connector

Pin name	Conn. Pin	Function	Notes
JTAG_TMS	J7.3	JTAG TMS	On board connector
JTAG_TCK	J7.2	JTAG clock	On board connector
JTAG_VREF	J7.10	JTAG VREF	On board connector
JTAG_nTRST	J7.6	JTAG TRST	On board connector
DGND	J7.1	Ground	On board connector
CPU_PORn	J7.7	Please refer to Section 5.2.1.	

J7.8 and J7.9 pin are not connected.

7.11 SD/SDIO/MMC

The processor provides 4 MMC/SD/SDIO ports through the Ultra Secured Digital Host Controller (USDHC), compliant with MMC V4.41, Secure Digital Memory Card Specification V3.00 and Secure Digital Input Output (SDIO) V3.00 specifications. The controller supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes. High capacity SD cards (SDHC) are supported.

Three MMC/SD/SDIO interfaces are available on **AXEL LITE** SOM.

7.11.1 MMC/SD/SDIO1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
SD1_CD	J2.28	Card detection pin	If not used(for the embedded memory),tie low to indicate there is a card attached.
SD1_CLK	J2.85	Clock for MMC/SD/SDIO card	
SD1_CMD	J2.83	CMD line	
SD1_DATA0	J2.75	DATA0 line in all modes	Also used to detect busy state
SD1_DATA1	J2.77	DATA1 line in 4/8-bit mode	Also used to detect interrupt in 1/4-bit mode