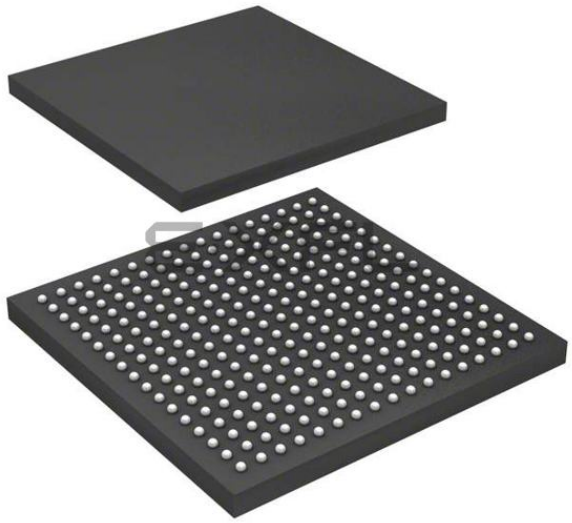

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	454MHz
Co-Processors/DSP	Data; DCP
RAM Controllers	LVDDR, LVDDR2, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Hardware ID
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx283dvm4br2

such as memories and SD cards, as well as provide battery charging capability for Li-Ion batteries.

The i.MX28 processor includes an additional 128-Kbyte on-chip SRAM to make the device ideal for eliminating external RAM in applications with small footprint RTOS.

The i.MX28 supports connections to various types of external memories, such as mobile DDR, DDR2 and LV-DDR2, SLC and MLC NAND Flash.

The i.MX28 can be connected to a variety of external devices such as high-speed USB2.0 OTG, CAN, 10/100 Ethernet, and SD/SDIO/MMC.

1.1 Device Features

The following lists the features of the i.MX28:

- ARM926EJ-S CPU running at 454 MHz:
  - 16-Kbyte instruction cache and 32-Kbyte data cache
  - ARM embedded trace macrocell (CoreSight™ ETM9™)
  - Parallel JTAG interface
- 128 KBytes of integrated low-power on-chip SRAM
- 128 KBytes of integrated mask-programmable on-chip ROM
- 1280 bits of on-chip one-time-programmable (OCOTP) ROM
- 16-bit mobile DDR (mDDR) (1.8 V), DDR2 (1.8 V) and LV-DDR2 (1.5 V), up to 205 MHz DDR clock frequency with voltage overdrive
- Support for up to eight NAND Flash memory devices with up to 20-bit BCH ECC
- Four synchronous serial ports (SSP) for SDIO/MMC/MS/SPI: SSP0, SSP1, SSP2, and SSP3. SSP0 and SSP1 can support three modes,1-bit, 4-bit, and 8-bit, whereas SSP2 and SSP3 can support only 1-bit and 4-bit modes.
- 10/100-Mbps Ethernet MAC compatible with IEEE Std 802.3™:
  - Single 10/100 Ethernet with GMII/RMII or Dual 10/100 Ethernet with RMII interface
  - Supporting IEEE Std 1588™-compatible hardware timestamp
  - Supporting 50-MHz/25-MHz clock output for external Ethernet PHY
- Two 2.0B protocol-compatible Controller Area Network (CAN) interfaces
- One USB2.0 OTG device/host controller and PHY
- One USB2.0 host controller and PHY
- LCD controller, up to 24-bit RGB (DOTCK) modes and 24-bit system-mode
- Pixel-processing pipeline (PXP) supports full path from color-space conversion, scaling, alpha-blending to rotation without intermediate memory access.
- SPDIF transmitter
- Dual serial audio interface (SAIF) to support full-duplex transmit and receive operations; each SAIF supports three stereo pairs
- Five application Universal Asynchronous Receiver-Transmitters (UARTs), up to 3.25 Mbps with hardware flow control

- One debug UART operating at up to 115 Kb/s using programmed I/O
- Two I^2C master/slave interfaces, up to 400 kbps
- Four 32-bit timers and a rotary decoder
- Eight Pulse Width Modulators (PWMs)
- Real-time clock (RTC)
- GPIO with interrupt capability
- Power Management Unit (PMU) supports a triple output DC-DC switching converter, multiple linear regulators, battery charger, and detector.
- 16-channel Low-Resolution A/D Converter (LRADC). There are 16 physical channels but they can only be mapped to 8 virtual channels at a time.
- Single channel High Speed A/D Converter (HSADC), up to 2 Msps data rate
- 4/5-wire touchscreen controller
- Up to 8X8 keypad matrix with button-detect circuit
- Security features:
  - Read-only unique ID for Digital Rights Management (DRM) algorithms
  - Secure boot using 128-bit AES hardware decryption
  - SHA-1 and SHA256 hashing hardware
  - High assurance boot (HAB4)
- Offered in 289-pin Ball Grid Array (BGA)

1.2 Ordering Information and Functional Part Differences

Table 1 provides the ordering information for the i.MX28.

Table 1. Ordering Information

Part Number	Projected Temperature Range (°C)	Package
MCIMX280DVM4B	–20 to +70	14 x 14 mm, 0.8mm pitch, MAPBGA-289
MCIMX280CVM4B	–40 to +85	14 x 14 mm, 0.8mm pitch, MAPBGA-289
MCIMX283DVM4B	–20 to +70	14 x 14 mm, 0.8 mm pitch, MAPBGA-289
MCIMX283CVM4B	–40 to +85	14 x 14 mm, 0.8 mm pitch, MAPBGA-289
MCIMX286DVM4B	–20 to +70	14 x 14 mm, 0.8 mm pitch, MAPBGA-289
MCIMX286CVM4B	–40 to +85	14 x 14 mm, 0.8 mm pitch, MAPBGA-289
MCIMX287CVM4B	–40 to +85	14 x 14 mm, 0.8 mm pitch, MAPBGA-289

2.1 Special Signal Considerations

Special signal considerations are listed in Table 5. The package contact assignment is found in Section 4, “Package Information and Contact Assignments.” Signal descriptions are provided in the reference manual.

Table 5. Signal Considerations

Signal	Descriptions
PSWITCH	The pin is used for chip power on or recovery. VDDIO can be applied to PSWITCH through a 10 kΩ resistor. This is necessary in order to enter the chip’s firmware recovery. The on-chip circuitry prevents the actual voltage on the pin from exceeding acceptable levels.
VDDXTAL	This pin is an output of i.MX28. Should be coupled to ground with a 0.1 uF capacitor. User should not supply external power to this pin.
BATTERY	This pin should be connected to the battery with minimal resistance. It provides charging current to the battery. See the “Power Supply” section of the reference manual for details.
DCDC_BATTERY	This pin is an input of i.MX28 that provides supply to the DCDC converter. It should be connected to the battery with minimal resistance. See the “Power Supply” section of the reference manual for details.
XTALI XTALO	These analog pins are connected to an external 24 MHz crystal circuit. This crystal provides the clock source for on-chip PLLs.
RTC_XTALO RTC_XTALI	These analog pins are connected to an external 32.768/32.0 kHz crystal circuit. This crystal provides clock source to the on-chip real-time counter circuits.
RESETN	This pin resets the chip if it is low. This pin is pulled up to VDDIO33 with an internal 10 kΩ resistor. No external pull up resistors are needed.
DEBUG	This pin is used for JTAG interface. DEBUG=0: JTAG interface works for boundary scan. DEBUG=1: JTAG interface works for ARM debugging.
TESTMODE	For Freescale factory use only. Must be externally connected to GND for normal operation.

3 Electrical Characteristics

This section provides the device-level and module-level electrical characteristics for the i.MX28.

3.1 i.MX28 Device-Level Conditions

This section provides the device-level electrical characteristics for the IC.

3.1.1 DC Absolute Maximum Ratings

Table 6 provides the DC absolute maximum operating conditions.

- Stresses beyond those listed under Table 6 may cause permanent damage to the device.

Table 13 illustrates the power supply characteristics.

Table 13. Power Supply Characteristics

Parameter	Min	Typ	Max	Unit
Linear Regulators				
Output Voltage Accuracy (V_{DDIO}, V_{DDA}, V_{DDM}, V_{DDD})[1]	–3	—	+3	%
V_{DDIO} Maximum Output Current (V_{DDIO} = 3.30 V, V_{DD5V} = 4.75 V)[2, 3]	270	—	—	mA
V_{DDM} Maximum Output Current (V_{DDM} = 1.5 V)[2]	160	—	—	mA
V_{DDA} Maximum Output Current (V_{DDA} = 1.8 V)[2, 3]	225	—	—	mA
V_{DDD} Maximum Output Current (V_{DDD} = 1.2 V)[2, 3]	200	—	—	mA
DCDC Converters				
Output Voltage Accuracy (DCDC_VDDIO, DCDC_VDDA, DCDC_VDDD)[1]	–3	—	+3	%
DCDC_VDDD Maximum Output Current (V_{DDD} = 1.55 V)[4, 5]	250	—	—	mA
DCDC_VDDA Maximum Output Current (V_{DDA} = 1.8 V)[4, 5]	200	—	—	mA
DCDC_VDDIO Maximum Output Current (V_{DDIO} = 3.15 V, 3.3 V < BATT < 4.242 V)[4, 5, 6]	250	—	—	mA
VDD4P2 Regulated Output				
VDD4P2 Output Voltage Accuracy (TARGET=4.2V)[1]	–3	—	+3	%
VDD4P2 Output Current Limit Accuracy (VDD5V = 4.75 V, ILIMIT=480 mA)[7]	480	500	520	mA
VDD4P2 Output Current Limit Accuracy (VDD5V=4.75 V, ILIMIT=100 mA)[7]	100	120	140	mA
Battery Charger				
Final Charge Voltage Accuracy (TARGET=4.2 V)	-2	—	+1	%

1 No load.

2 Maximum output current measured when output voltage droops 100 mV from the programmed target voltage with no load present.

3 Because the internal linear regulators are cascaded, it is not possible to simultaneously operate the V_{DDIO}, V_{DDA}, V_{DDM}, and V_{DDD} linear regulators at the maximum specified load current. For example, the V_{DDIO} linear regulator provides current to both the V_{DDIO} 3.3 V supply rail as well as the V_{DDM} and V_{DDA} linear regulator inputs. Likewise, the V_{DDA} linear regulator provides current to both the 1.8 V supply rail as well as the V_{DDD} linear regulator input. The application designer should ensure the following two conditions are met:

(V_{DDIO} Load Current + V_{DDM} Load Current + V_{DDA} Load Current) < V_{DDIO} Maximum Output Current
(V_{DDA} Load Current + V_{DDD} Load Current) < V_{DDA} Maximum Output Current

4 DCDC Double FETs Enabled, Inductor Value = 15 µH.

5 The DCDC Converter is a triple output buck converter. The maximum output current capability of each output of the converter is dependent on the loads on the other two outputs. For a given output, it may be possible to achieve a maximum output current higher than that specified by ensuring the load on the other outputs is well below the maximum.

6 Assumes simultaneous load of IDDD = 250 mA@ 1.55 V and IDDA = 200 mA@1.8 V.

7 Untuned.

Table 25. Digital Pin DC Characteristics for GPIO in 3.3-V Mode (continued)

Parameter	Symbol	Min	Max	Unit
10-K pull-up resistance[2]	Rpu10k	8	12	kΩ
47-K pull-up resistance	Rpu47k	39	56	kΩ

1 The conditions of the current measurements for all different drives are as follows:
IOL: at 0.4 V
IOH: at VDDIO * 0.8 V
Maximum corner for 3.3 V mode: 3.6 V, -40°C, fast process.
Minimum corner for 3.3 V mode: 3.0 V, 105°C, slow process.
8 gpio pins (LCD_D0-D7) and 2 gpio_clk pins (LCD_DOTCLK and LCD_WR_RWN) simultaneously loaded.

2 See the i.MX28 reference manual for detailed pull-up configuration of each I/O.

Table 26 shows the digital pin DC characteristics for GPIO in 1.8 V mode.

Table 26. Digital Pin DC Characteristics for GPIO in 1.8 V Mode

	Symbol	Min	Max	Unit
Input voltage high (DC)	VIH	0.7 × VDDIO18	VDDIO18	V
Input voltage low (DC)	VIL	—	0.3 × VDDIO18	V
Output voltage high (DC)	VOH	0.8 * VDDIO18	—	V
Output voltage low (DC)	VOL	—	0.2 × VDDIO18	V
Output source current[1] (DC) *gpio*	IOH – low	-2.2	—	mA
	IOH – medium	-3.5	—	mA
	IOH – high	-4.0	—	mA
Output sink current (DC) *gpio*	IOL – low	3.3	—	mA
	IOL – medium	7.0	—	mA
	IOL – high	7.5	—	mA
Output source current (DC) *gpio_clk*	IOH – low	-4.2	—	mA
	IOH – high	-6.0	—	mA
Output sink current (DC) *gpio_clk*	IOL – low	6.8	—	mA
	IOL – high	11.5	—	mA
10-K pull-up resistance[2]	Rpu10k	8	12	kΩ
47-K pull-up resistance	Rpu47k	39	56	kΩ

1 The condition of the current measurements for all different drives are as follows:
Maximum corner for 1.8 V mode: 1.9 V, -40°C, Fast process.
Minimum corner for 1.8 V mode: 1.7 V, 105°C, Slow process.
1 gpio pin (GPMI_D0) and 1 gpio_clk pin (GPMI_WRN) simultaneously loaded.

2 See the i.MX28 reference manual for detailed pull-up configuration of each I/O.

3.5.3 EMI AC Timing

This section includes descriptions of the electrical specifications of EMI module which interfaces external DDR2 and Mobile-DDR1 (LP-DDR1) memory devices.

3.5.3.1 EMI Command and Address AC Timing

Figure 5 and Table 34 specify the timing related to the address and command pins that interfaces DDR2 and Mobile-DDR1 memory devices.

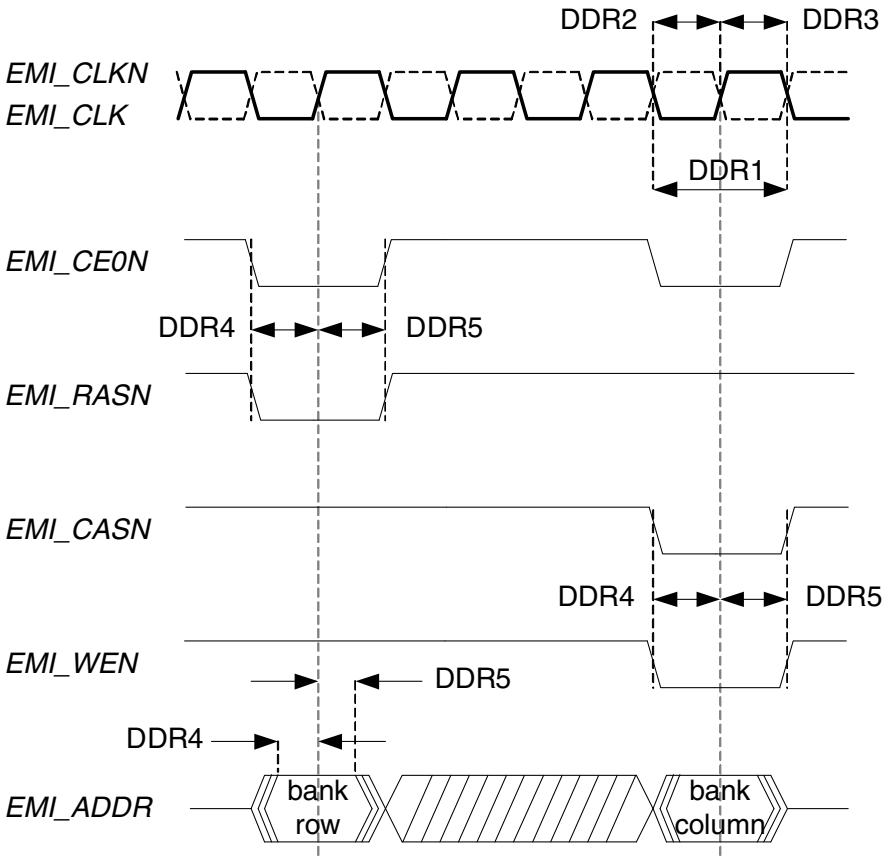


Figure 5. EMI Command/Address AC Timing

Table 34. EMI Command/Address AC Timing

ID	Description	Symbol	Min.	Max.	Unit
DDR1	CK cycle time	tCK	4.86	—	ns
DDR2	CK high level width	tCH	0.5 tCK –0.5	0.5 tCK + 0.5	ns
DDR3	CK low level width	tCL	0.5 tCK –0.5	0.5 tCK + 0.5	ns

Table 35. DDR Output AC Timing (continued)

ID	Description	Symbol	Min	Max	Unit
DDR15	DQ & DQM output setup time relative to DQS	tDS	1/4 tCK –0.8	1/4 tCK –0.5	ns
DDR16	DQ & DQM output hold time relative to DQS	tDH	1/4 tCK –0.8	1/4 tCK –0.5	ns

3.5.3.3 DDR2 Input AC Timing

Figure 7 and Table 36 show input AC timing for standard DDR2 and LVDDR2.

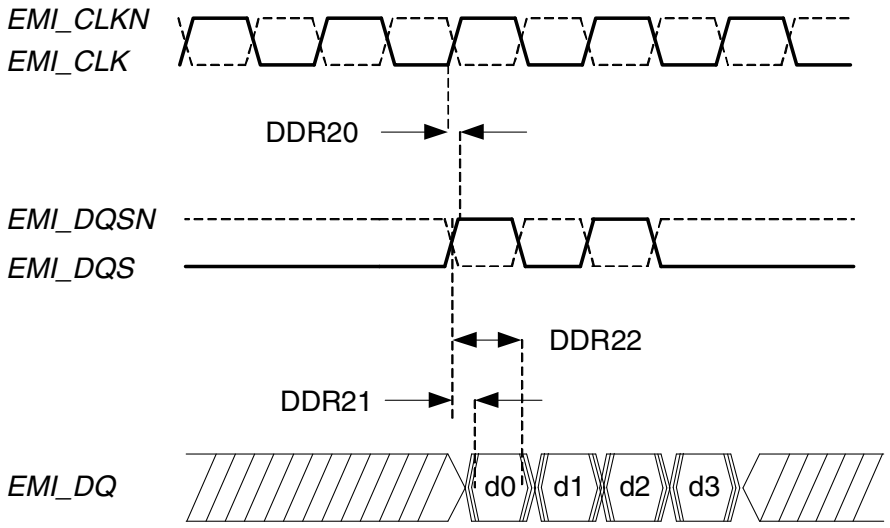


Figure 7. DDR2 Input AC Timing

Table 36. DDR2 Input AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR20	Positive DQS latching edge to associated CK edge	tDQSCK	–0.5	0.5	ns
DDR21	DQS to DQ input skew	tDQSQ	0.25 tCK –0.85	0.25 tCK –0.5	ns
DDR22	DQS to DQ input hold time	tQH	0.25 tCK +0.75	0.25 tCK + 1	ns

Figure 10 shows MII transmit signal timings. Table 39 describes the timing parameters (M5–M8) shown in the figure.

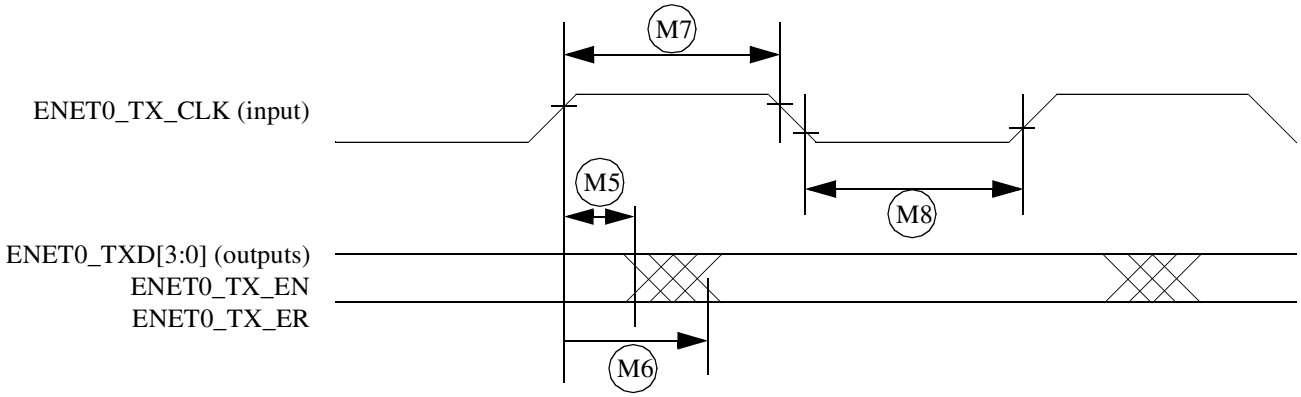


Figure 10. MII Transmit Signal Timing Diagram

Table 39. MII Transmit Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M5	ENET0_TX_CLK to ENET0_TXD[3:0], ENET0_TX_EN, ENET0_TX_ER invalid	5	—	ns
M6	ENET0_TX_CLK to ENET0_TXD[3:0], ENET0_TX_EN, ENET0_TX_ER valid	—	20	ns
M7	ENET0_TX_CLK pulse width high	35%	65%	ENET0_TX_CLK period
M8	ENET0_TX_CLK pulse width low	35%	65%	ENET0_TX_CLK period

[1] ENET0_TX_EN, ENET0_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

3.5.4.1.3 MII Asynchronous Inputs Signal Timing (ENET0_CRS and ENET0_COL)

Figure 11 shows MII asynchronous input timings. Table 40 describes the timing parameter (M9) shown in the figure.

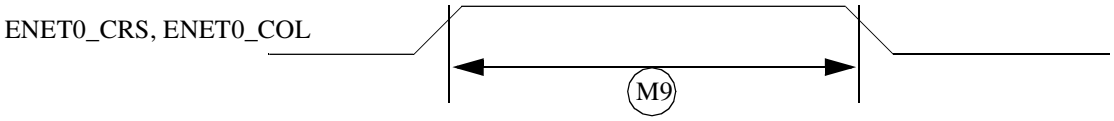


Figure 11. MII Async Inputs Timing Diagram

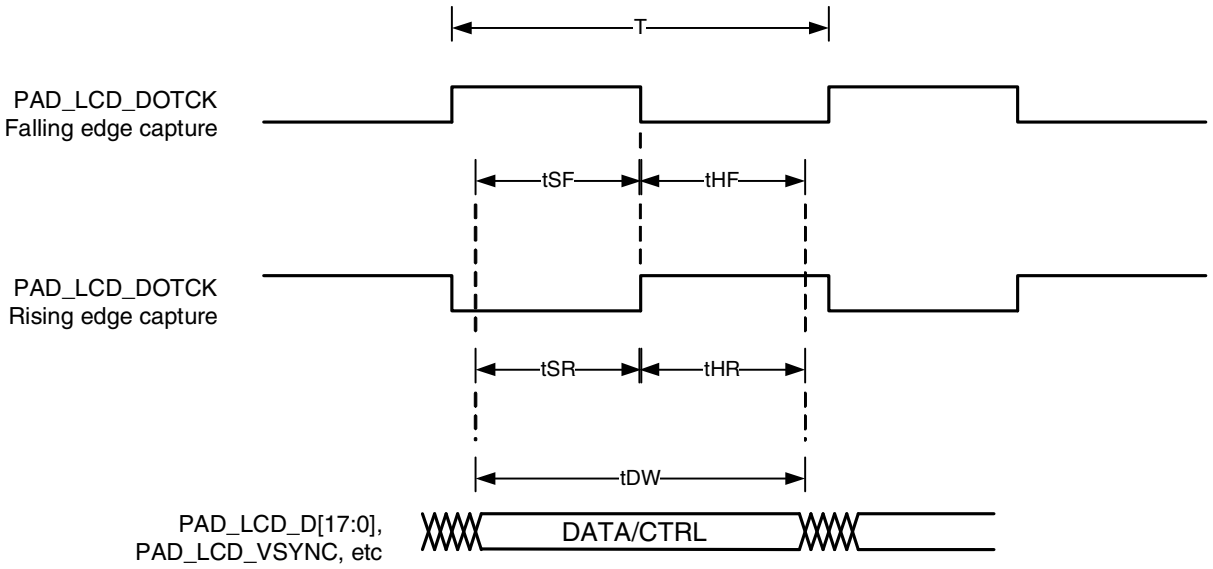
Table 40. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	ENET0_CRS to ENET0_COL minimum pulse width	1.5	—	ENET0_TX_CLK period

[1] ENET0_COL has the same timing in 10-Mbit 7-wire interface mode.

3.5.8 LCD AC Output Electrical Specifications

Figure 24 depicts the AC output timing for the LCD module. Table 48 lists the LCD module timing parameters.



Notes:
T = LCD interface clock period
I/O Drive Strength = 4mA
I/O Voltage = 3.3V
Cck = Capacitance load on DOTCK pad
Cd = Capacitance load on DATA/CTRL pad

Figure 24. LCD AC Output Timing Diagram

Table 48. LCD AC Output Timing Parameters

ID	Parameter	Description
tSF	Data setup for falling edge	DOTCK = T/2 – 1.97ns + 0.15*Cck – 0.19*Cd
tHF	Data hold for falling edge	DOTCK = T/2 + 0.29ns + 0.09*Cd – 0.10*Cck
tSR	Data setup for rising edge	DOTCK = T/2 – 2.09ns + 0.18*Cck – 0.19*Cd
tHR	Data hold for rising edge	DOTCK = T/2 + 0.40ns + 0.09*Cd – 0.10*Cck
tDW	Data valid window	tDW = T – 1.45ns

3.5.9 Inter IC (I^2C) Timing

The I^2C module is designed to support up to 400-Kbps I^2C connection compliant with I^2C bus protocol. The following section describes I^2C SDA and SCL signal timings.

Figure 25 shows the timing of the I^2C module. Table 49 describes the I^2C module timing parameters (IC1–IC11) shown in the figure.

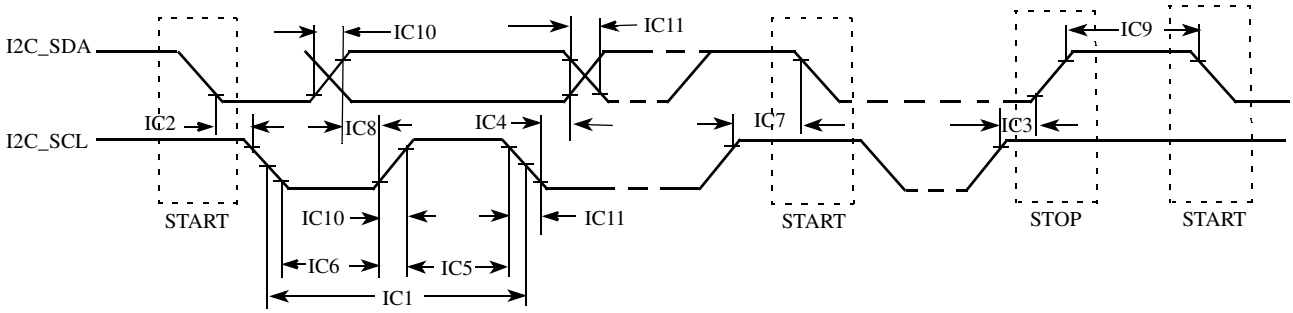


Figure 25. I^2C Module Timing Diagram

Table 49. I^2C Module Timing Parameters: 1.8 V – 3.6 V

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
IC1	I2C_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2C_SCL clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2C_SCL clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2C_SDA and I2C_SCL signals	—	1000	$20+0.1C_b$[4]	300	ns
IC11	Fall time of both I2C_SDA and I2C_SCL signals	—	300	$20+0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for the I2C_SDA signal in order to bridge the undefined region of the falling edge of I2C_SCL.

2 The maximum IC4 has to be met only if the device does not stretch the LOW period (ID no IC5) of the I2C_SCL signal.

3 A fast-mode I2C bus device can be used in a standard-mode I^2C bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the I2C_SCL signal. If such a device does stretch the LOW period of the I2C_SCL signal, it must output the next data bit to the I2C_SDA line max_rise_time (ID No IC9) + data_setup_time (ID No IC7) = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the I2C_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

Table 53. PWM Output Timing Parameter: MATT Mode 24 MHz Crystal Clock

Ref No.	Parameter	Minimum	Maximum	Unit
1	System CLK frequency[1]	24	24	MHz
2a	Clock high time	20.99	—	ns
2b	Clock low time	21.01	—	ns
3a	Clock fall time	—	0.3	ns
3b	Clock rise time	—	0.3	ns
4a	Output delay time	—	15.23	ns
4b	Output setup time	15.92	—	ns

[1] CL of PWMO = 30 pF

3.5.12 Serial Audio Interface (SAIF) AC Timing

The following subsections describe SAIF timing in two cases:

- Transmitter
- Receiver

3.5.12.1 SAIF Transmitter Timing

Figure 33 shows the timing for SAIF transmitter with internal clock, and Table 54 describes the timing parameters (SS1–SS13).

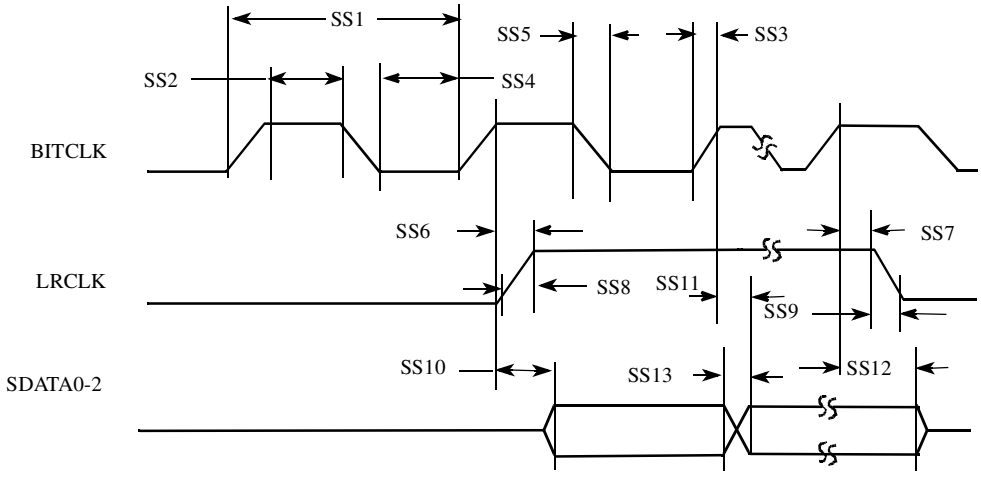


Figure 33. SAIF Transmitter Timing Diagram

Table 54. SAIF Transmitter Timing

ID	Parameter	Min.	Max.	Unit
SS1	BITCLK period	81.4	—	ns
SS2	BITCLK high period	36.0	—	ns
SS3	BITCLK rise time	—	6.0	ns
SS4	BITCLK low period	36.0	—	ns
SS5	BITCLK fall time	—	6.0	ns
SS6	BITCLK high to LRCLK high	—	15.0	ns
SS7	BITCLK high to LRCLK low	—	15.0	ns
SS8	LRCLK rise time	—	6.0	ns
SS9	LRCLK fall time	—	6.0	ns
SS10	BITCLK high to SDATA valid from high impedance	—	15.0	ns
SS11	BITCLK high to SDATA high/low	—	15.0	ns
SS12	BITCLK high to SDATA high impedance	—	15.0	ns
SS13	SDATA rise/fall time	—	6.0	ns

3.5.12.2 SAIF Receiver Timing

Figure 34 shows the timing for the SAIF receiver with internal clock. Table 55 describes the timing parameters (SS1–SS17) shown in the figure.

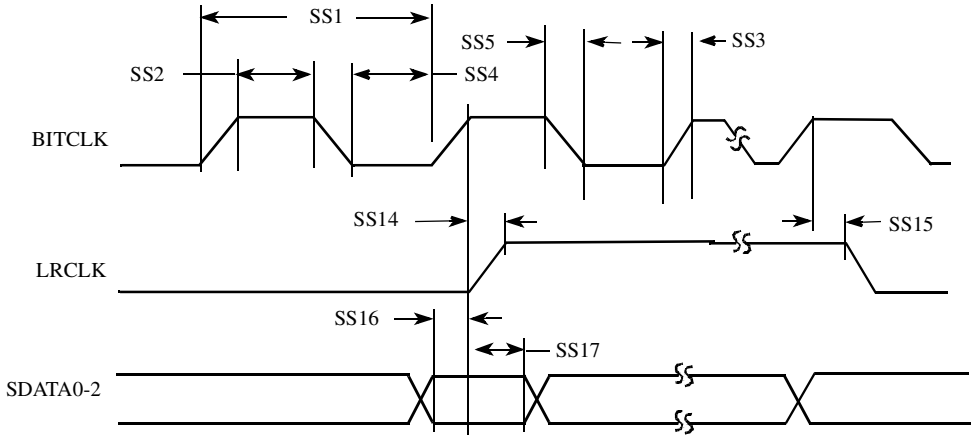


Figure 34. SAIF Receiver Timing Diagram

Table 55. SAIF Receiver Timing with Internal Clock

ID	Parameter	Min.	Max.	Unit
SS1	BITCLK period	81.4	—	ns
SS2	BITCLK high period	36.0	—	ns
SS3	BITCLK rise time	—	6.0	ns
SS4	BITCLK low period	36.0	—	ns
SS5	BITCLK fall time	—	6.0	ns
SS14	BITCLK high to LRCLK high	—	15.0	ns
SS15	BITCLK high to LRCLK low	—	15.0	ns
SS16	SDATA setup time before BITCLK high	10.0	—	ns
SS17	SDATA hold time after BITCLK high	0.0	—	ns

3.5.13 SPDIF AC Timing

SPDIF data is sent using bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

The following Table 56 shows SPDIF timing parameters, including the timing of the modulating Tx clock (spdif_clk) in SPDIF transmitter as shown in the Figure 35.

Table 56. SPDIF Timing

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFOUT output (Load = 30pf) • Skew • Transition Rising • Transition Falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Tx clock (spdif_clk) period	spclkp	81.4	—	ns
spdif_clk high period	spclkph	65.1	—	ns
spdif_clk low period	spclkpl	65.1	—	ns

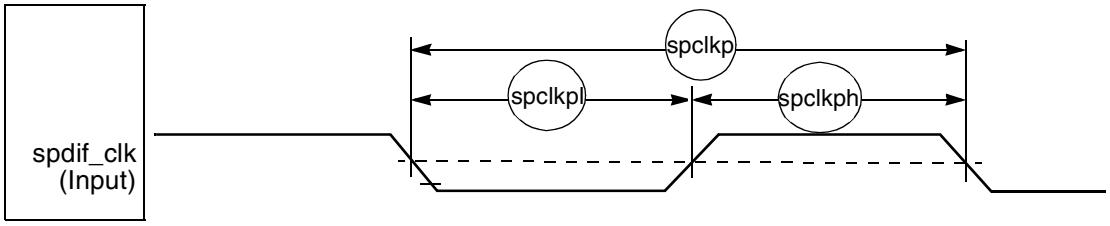


Figure 35. spdif_clk Timing

Table 60. MS Parallel Transfer Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
MS5	SCK Fall Time	tCLKf	—	10	ns
MS11	BS Setup Time	tBSsu	8	—	ns
MS12	BS Hold Time	tBSh	1	—	ns
MS13	DATA Setup Time	tDsu	8	—	ns
MS14	DATA Hold Time	tDh	1	—	ns
MS15	DATA Input Delay Time	tDd	—	15	ns

3.5.14.4 SPI AC Timing

Figure 41 depicts the master mode and slave mode timings of the SPI, and Table 61 lists the timing parameters.

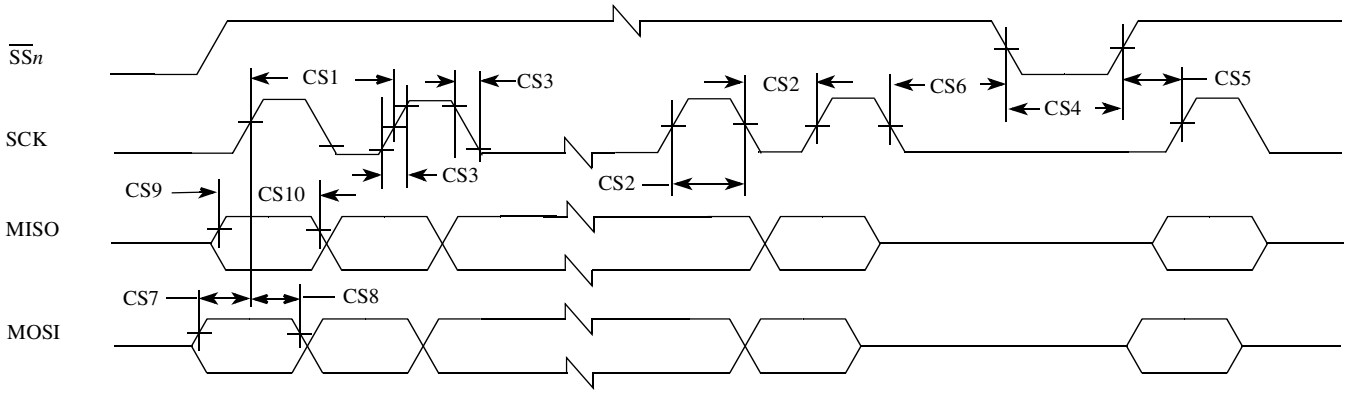


Figure 41. SPI Interface Timing Diagram

Table 61. SPI Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
CS1	SCK cycle time	t_{clk}	50	—	ns
CS2	SCK high or low time	t_{SW}	25	—	ns
CS3	SCK rise or fall	$t_{RISE/FALL}$	—	7.6	ns
CS4	$\overline{SS}n$ pulse width	t_{CSLH}	25	—	ns
CS5	$\overline{SS}n$ lead time (CS setup time)	t_{SCS}	25	—	ns
CS6	$\overline{SS}n$ lag time (CS hold time)	t_{HCS}	25	—	ns
CS7	MOSI setup time	t_{Smosi}	5	—	ns
CS8	MOSI hold time	t_{Hmosi}	5	—	ns
CS9	MISO setup time	t_{Smiso}	5	—	ns
CS10	MISO hold time	t_{Hmiso}	5	—	ns

3.5.15 UART (UARTAPP and DebugUART) AC Timing

This section describes the UART module AC timing which is applicable to both UARTAPP and DebugUART.

3.5.15.1 UART Transmit Timing

Figure 39 shows the UART transmit timing, showing only eight data bits and one stop bit. Table 62 describes the timing parameter (UA1) shown in the figure.

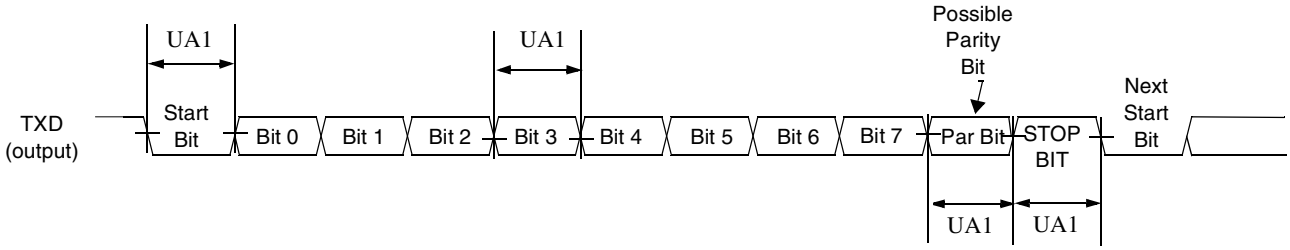


Figure 42. UART Transmit Timing Diagram

Table 62. UART Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UARTAPP can support is 3.25 Mbps. The maximum baud rate of DebugUART is 115.2 kbps.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (which is APBX clock = 24 MHz).

3.5.15.2 UART Receive Timing

Figure 43 shows the UART receive timing, showing only eight data bits and one stop bit. Table 63 describes the timing parameter (UA2) shown in the figure.

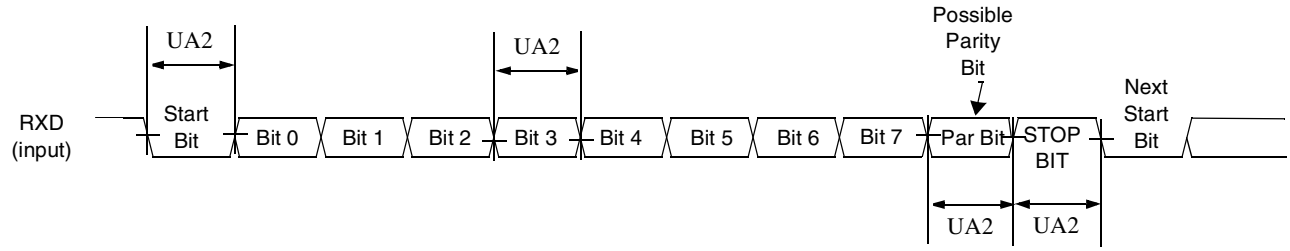


Figure 43. UART Receive Timing Diagram

Table 63. UART Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
UA2	Receive bit time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] $- 1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UARTAPP can support is 3.25 Mbps. The maximum baud rate of DebugUART is 115 kbps.

4 Package Information and Contact Assignments

4.1 Case MAPBGA-289, 14 x 14 mm, 0.8 mm Pitch

The following notes apply to Figure 44:

- All dimensions are in millimeters.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Maximum solder bump diameter measured parallel to datum A.
- Datum A, the seating plane, is determined by the spherical crowns of the solder bumps.
- Parallelism measurement excludes any effect of mark on top surface of package.

Table 65. i.MX287 MAPBGA Contact Assignments (continued)

Signal Name	Contact Assignment
DCDC_VDDA	B16
DCDC_VDDD	D17
DCDC_VDDIO	C17
DEBUG	B9
EMI_A00	U15
EMI_A01	U12
EMI_A02	U14
EMI_A03	T11
EMI_A04	U10
EMI_A05	R11
EMI_A06	R9
EMI_A07	N11
EMI_A08	U9
EMI_A09	P10
EMI_A10	U13
EMI_A11	T10
EMI_A12	U11
EMI_A13	T9
EMI_A14	N10
EMI_BA0	T16
EMI_BA1	T12
EMI_BA2	N12
EMI_CASN	U16
EMI_CE0N	P12
EMI_CE1N	P9
EMI_CKE	T13
EMI_CLK	L17
EMI_CLKN	L16
EMI_D00	N16
EMI_D01	M13
EMI_D02	P15
EMI_D03	N14

Signal Name	Contact Assignment
ENET0_TX_CLK	E3
ENET0_TX_EN	F4
ENET_CLK	E2
GPMI_ALE	P6
GPMI_CE0N	N7
GPMI_CE1N	N9
GPMI_CE2N	M7
GPMI_CE3N	M9
GPMI_CLE	P7
GPMI_D00	U8
GPMI_D01	T8
GPMI_D02	R8
GPMI_D03	U7
GPMI_D04	T7
GPMI_D05	R7
GPMI_D06	U6
GPMI_D07	T6
GPMI_RDN	R6
GPMI_RDY0	N6
GPMI_RDY1	N8
GPMI_RDY2	M8
GPMI_RDY3	L8
GPMI_RESETN	L9
GPMI_WRN	P8
HSADC0	B14
I2C0_SCL	C7
I2C0_SDA	D8
JTAG_RTCK	E14
JTAG_TCK	E11
JTAG_TDI	E12
JTAG_TDO	E13
JTAG_TMS	D12

Signal Name	Contact Assignment
LRADC6	C14
PSWITCH	A11
PWM0	K7
PWM1	L7
PWM2	K8
PWM3	E9
PWM4	E10
RESETN	A14
RTC_XTALI	D11
RTC_XTALO	C11
SAIF0_BITCLK	F7
SAIF0_LRCLK	G6
SAIF0_MCLK	G7
SAIF0_SDATA0	E7
SAIF1_SDATA0	E8
SPDIF	D7
SSP0_CMD	A4
SSP0_DATA0	B6
SSP0_DATA1	C6
SSP0_DATA2	D6
SSP0_DATA3	A5
SSP0_DATA4	B5
SSP0_DATA5	C5
SSP0_DATA6	D5
SSP0_DATA7	B4
SSP0_DETECT	D10
SSP0_SCK	A6
SSP1_CMD	C1
SSP1_DATA0	D1
SSP1_DATA3	E1
SSP1_SCK	B1
SSP2_MISO	B3

Table 68. 289-Pin i.MX286 MAPBGA Ball Map (continued)

	U	T	R	P	N	M	L
1	VSS	LCD_D12	LCD_D10	LCD_D07	NC	NC	NC
2	LCD_D14	LCD_D13	LCD_D11	LCD_D08	LCD_D06	LCD_D04	LCD_D02
3	LCD_D15	LCD_D16	LCD_D17	LCD_D09	VDDIO33	LCD_D05	LCD_D03
4	LCD_D18	LCD_D19	LCD_D20	LCD_RD_E	VSS	LCD_RS	AUART1_RX
5	LCD_D21	LCD_D22	LCD_D23	LCD_CS	NC	NC	NC
6	GPMI_D06	GPMI_D07	GPMI_RDN	GPMI_ALE	GPMI_RDY0	LCD_RESET	NC
7	GPMI_D03	GPMI_D04	GPMI_D05	GPMI_CLE	GPMI_CE0N	GPMI_CE2N	PWM1
8	GPMI_D00	GPMI_D01	GPMI_D02	GPMI_WRN	GPMI_RDY1	GPMI_RDY2	GPMI_RDY3
9	EMI_A08	EMI_A13	EMI_A06	EMI_CE1N	GPMI_CE1N	GPMI_CE3N	GPMI_RESETN
10	EMI_A04	EMI_A11	VSSIO_EMI	EMI_A09	EMI_A14	VDDIO_EMI	VSS
11	EMI_A12	EMI_A03	EMI_A05	VDDIO_EMI	EMI_A07	VDDIO_EMI	VSS
12	EMI_A01	EMI_BA1	VSSIO_EMI	EMI_CE0N	EMI_BA2	VDDIO_EMI	VSSIO_EMI
13	EMI_A10	EMI_CKE	VDDIO_EMI	EMI_D04	VDDIO_EMI	EMI_D01	VDDIO_EMI
14	EMI_A02	VSSIO_EMI	EMI_VREF0	VSSIO_EMI	EMI_D03	VSS	EMI_D06
15	EMI_A00	EMI_WEN	VDDIO_EMIQ	EMI_D02	VDDIO_EMI	EMI_DQM0	EMI_DDR_OPEN_FB
16	EMI_CASN	EMI_BA0	EMI_RASN	VSSIO_EMI	EMI_D00	VSSIO_EMI	EMI_CLKN
17	VSSIO_EMI	EMI_ODT1	EMI_ODT0	EMI_D05	VDDIO33_EMI	EMI_D07	EMI_CLK
	U	T	R	P	N	M	L

4.7 i.MX287 Ball Map

Table 69 shows the i.MX287 MAPBGA Ball Map.

Table 69. 289-Pin i.MX287 MAPBGA Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VSS	SSP3_SCK	SSP2_SCK	SSP0_CMD	SSP0_DATA3	SSP0_SCK	VDDIO33	USB1DP	VSS	USB0DM	PSWITCH	XTALI	VDD4P2	RESETN	BATTERY	DCDC_LP	DCDC_GND	A

Table 69. 289-Pin i.MX287 MAPBGA Ball Map (continued)

K	J	H	G	F	E	D	C	B
LCD_WR_RWN	ENET0_RXD2	ENET0_RXD0	ENET0_TXD2	ENET0_TXD0	SSP1_DATA3	SSP1_DATA0	SSP1_CMD	SSP1_SCK
LCD_D00	ENET0_RXD3	ENET0_RXD1	ENET0_TXD3	ENET0_TXD1	ENET_CLK	SSP3_SS0	SSP3_MOSI	SSP3_MISO
LCD_D01	ENET0_CRS	VSS	VDDIO33	ENET0_RX_CLK	ENET0_TX_CLK	SSP2_SS1	SSP2_MOSI	SSP2_MISO
AUART1_TX	ENET0_COL	ENET0_MDIO	ENET0_MDC	ENET0_TX_EN	ENET0_RX_EN	SSP2_SS2	SSP2_SS0	SSP0_DATA7
AUART1_CTS	AUART1_RTS	AUART0_TX	AUART0_RX	AUART2_TX	VSS	SSP0_DATA6	SSP0_DATA5	SSP0_DATA4
AUART3_RTS	AUART0_CTS	AUART2_CTS	SAIF0_LRCLK	AUART2_RX	VDDIO33	SSP0_DATA2	SSP0_DATA1	SSP0_DATA0
PWM0	AUART0_RTS	AUART2_RTS	SAIF0_MCLK	SAIF0_BITCLK	SAIF0_SDATA0	SPDIF	I2C0_SCL	VSS
PWM2	VDDIO33	VDDIO33	VDDIO18	VDDIO18	SAIF1_SDATA0	I2C0_SDA	LRADC2	USB1DM
VSS	VDDIO33	VSS	VDDIO18	VDDIO18	PWM3	LRADC3	LRADC1	DEBUG
VSS	VDDIO33	VSS	VDDD	VDDD	PWM4	SSP0_DETECT	TESTMODE	USB0DP
VSS	VSS	VSS	VDDD	VDDD	JTAG_TCK	RTC_XTALI	RTC_XTALO	VSSA2
VDDD	VSS	VSS	VDDD	VDDD	JTAG_TDI	JTAG_TMS	VDDXTAL	XTALO
EMI_VREF1	VDDIO_EMIQ	EMI_D12	VDDIO_EMI	EMI_D14	JTAG_TDO	LRADC4	VDDA1	VSSA1
EMI_DDR_OPEN	EMI_D11	VSSIO_EMI	EMI_D10	VSSIO_EMI	JTAG_RTCK	JTAG_TRST	LRADC6	HSADC0
VDDIO_EMIQ	VSS	EMI_D09	VDDIO_EMI	EMI_DQM1	VSS	LRADC5	LRADC0	DCDC_BATT
EMI_DQS0N	EMI_DQS1N	VSS	EMI_D08	VSSIO_EMI	VDDIO33	VDD1P5	VSS	DCDC_VDDA
EMI_DQS0	EMI_DQS1	EMI_D13	VDDIO_EMI	EMI_D15	VDD5V	DCDC_VDDD	DCDC_VDDIO	DCDC_LN1
K	J	H	G	F	E	D	C	B

Table 70. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 0	09/2010	Initial release.