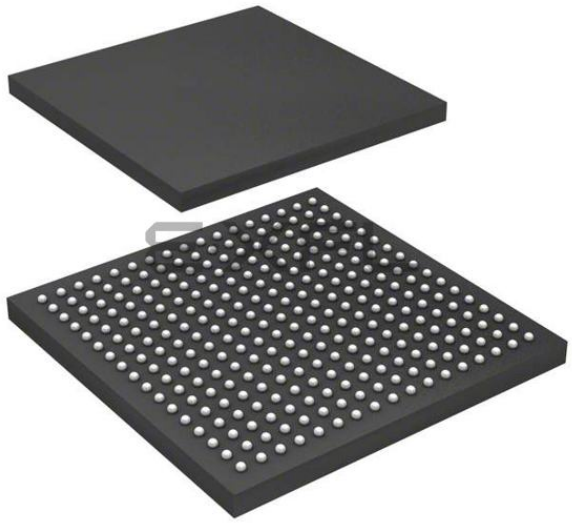

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	454MHz
Co-Processors/DSP	Data; DCP
RAM Controllers	LVDDR, LVDDR2, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Boot Security, Cryptography, Hardware ID
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx286cvm4br2

such as memories and SD cards, as well as provide battery charging capability for Li-Ion batteries.

The i.MX28 processor includes an additional 128-Kbyte on-chip SRAM to make the device ideal for eliminating external RAM in applications with small footprint RTOS.

The i.MX28 supports connections to various types of external memories, such as mobile DDR, DDR2 and LV-DDR2, SLC and MLC NAND Flash.

The i.MX28 can be connected to a variety of external devices such as high-speed USB2.0 OTG, CAN, 10/100 Ethernet, and SD/SDIO/MMC.

1.1 Device Features

The following lists the features of the i.MX28:

- ARM926EJ-S CPU running at 454 MHz:
  - 16-Kbyte instruction cache and 32-Kbyte data cache
  - ARM embedded trace macrocell (CoreSight™ ETM9™)
  - Parallel JTAG interface
- 128 KBytes of integrated low-power on-chip SRAM
- 128 KBytes of integrated mask-programmable on-chip ROM
- 1280 bits of on-chip one-time-programmable (OCOTP) ROM
- 16-bit mobile DDR (mDDR) (1.8 V), DDR2 (1.8 V) and LV-DDR2 (1.5 V), up to 205 MHz DDR clock frequency with voltage overdrive
- Support for up to eight NAND Flash memory devices with up to 20-bit BCH ECC
- Four synchronous serial ports (SSP) for SDIO/MMC/MS/SPI: SSP0, SSP1, SSP2, and SSP3. SSP0 and SSP1 can support three modes,1-bit, 4-bit, and 8-bit, whereas SSP2 and SSP3 can support only 1-bit and 4-bit modes.
- 10/100-Mbps Ethernet MAC compatible with IEEE Std 802.3™:
  - Single 10/100 Ethernet with GMII/RMII or Dual 10/100 Ethernet with RMII interface
  - Supporting IEEE Std 1588™-compatible hardware timestamp
  - Supporting 50-MHz/25-MHz clock output for external Ethernet PHY
- Two 2.0B protocol-compatible Controller Area Network (CAN) interfaces
- One USB2.0 OTG device/host controller and PHY
- One USB2.0 host controller and PHY
- LCD controller, up to 24-bit RGB (DOTCK) modes and 24-bit system-mode
- Pixel-processing pipeline (PXP) supports full path from color-space conversion, scaling, alpha-blending to rotation without intermediate memory access.
- SPDIF transmitter
- Dual serial audio interface (SAIF) to support full-duplex transmit and receive operations; each SAIF supports three stereo pairs
- Five application Universal Asynchronous Receiver-Transmitters (UARTs), up to 3.25 Mbps with hardware flow control

- One debug UART operating at up to 115 Kb/s using programmed I/O
- Two I^2C master/slave interfaces, up to 400 kbps
- Four 32-bit timers and a rotary decoder
- Eight Pulse Width Modulators (PWMs)
- Real-time clock (RTC)
- GPIO with interrupt capability
- Power Management Unit (PMU) supports a triple output DC-DC switching converter, multiple linear regulators, battery charger, and detector.
- 16-channel Low-Resolution A/D Converter (LRADC). There are 16 physical channels but they can only be mapped to 8 virtual channels at a time.
- Single channel High Speed A/D Converter (HSADC), up to 2 Msps data rate
- 4/5-wire touchscreen controller
- Up to 8X8 keypad matrix with button-detect circuit
- Security features:
  - Read-only unique ID for Digital Rights Management (DRM) algorithms
  - Secure boot using 128-bit AES hardware decryption
  - SHA-1 and SHA256 hashing hardware
  - High assurance boot (HAB4)
- Offered in 289-pin Ball Grid Array (BGA)

1.2 Ordering Information and Functional Part Differences

Table 1 provides the ordering information for the i.MX28.

Table 1. Ordering Information

Part Number	Projected Temperature Range (°C)	Package
MCIMX280DVM4B	–20 to +70	14 x 14 mm, 0.8mm pitch, MAPBGA-289
MCIMX280CVM4B	–40 to +85	14 x 14 mm, 0.8mm pitch, MAPBGA-289
MCIMX283DVM4B	–20 to +70	14 x 14 mm, 0.8 mm pitch, MAPBGA-289
MCIMX283CVM4B	–40 to +85	14 x 14 mm, 0.8 mm pitch, MAPBGA-289
MCIMX286DVM4B	–20 to +70	14 x 14 mm, 0.8 mm pitch, MAPBGA-289
MCIMX286CVM4B	–40 to +85	14 x 14 mm, 0.8 mm pitch, MAPBGA-289
MCIMX287CVM4B	–40 to +85	14 x 14 mm, 0.8 mm pitch, MAPBGA-289

Table 2 provides the functional differences between the i.MX280, i.MX283, i.MX286, and i.MX287.

Table 2. i.MX28 Functional Differences

Function	i.MX280	i.MX283	i.MX286	i.MX287
Application UART	x5	x5	x5	x5
Debug UART	x1	x1	x1	x1
CAN	—	—	x2	x2
Ethernet	x1	x1	x1	x2
High-speed ADC	x1	x1	x1	x1
L2 Switch	—	—	—	Yes
LCD Interface	—	Yes	Yes	Yes
LRADC[1]	x8	x8	x8	x8
PWM	x8	x8	x8	x8
S/PDIF Tx	—	—	Yes	Yes
SD/SDIO/MMC[2]	x4	x4	x4	x4
Security	Yes	Yes	Yes	Yes
SPI	x4	x4	x4	x4
Touch Screen	—	Yes	Yes	Yes
USB 2.0	OTG HS with HS PHY x1	OTG HS with HS PHY x1	OTG HS with HS PHY x1	OTG HS with HS PHY x1
	HS Host with HS PHY x1	HS Host with HS PHY x1	HS Host with HS PHY x1	HS Host with HS PHY x1

1 There are 16 physical channels but they can only be mapped to 8 virtual channels at a time.

2 For SD/SDIO/MMC, four synchronous serial ports (SSP) are available: SSP0, SSP1, SSP2, and SSP3. SSP0 and SSP1 can support three modes,1-bit, 4-bit, and 8-bit, whereas SSP2 and SSP3 can support only 1-bit and 4-bit modes.

Table 4. i.MX28 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DFLPT	Default first-level page table	System control	The DFLPT provides a unique method of implementing the ARM MMU first-level page table (L1PT) using a hardware-based approach.
DIGCTL	Digital control and on-chip RAM	System control	The digital control module includes sections for controlling the SRAM, the performance monitors, high-entropy pseudo-random number seed, free-running microseconds counter, and other chip control functions.
DUART	Debug UART	Connectivity peripherals	The Debug UART performs the following data conversions: • Serial-to-parallel conversion on data received from a peripheral device • Parallel-to-serial conversion on data transmitted to the peripheral device
EMI	External memory interface	Connectivity peripherals	The i.MX28 supports off-chip DRAM storage through the EMI controller, which is connected to the four internal AHB/AXI busses. The EMI supports multiple external memory types, including: • 1.8-V Mobile DDR1 (LP-DDR1) • Standard 1.8-V DDR2 • Low Voltage 1.5-V DDR2 (LV-DDR2)
ENET	Ethernet MAC Controller	Connectivity peripherals	Ethernet MAC controller connected to the uDMA (unified DMA). Supports 10/100 Mbps with TCP/UDP/IP Acceleration and IEEE 1588 Functions; also supports RMII or MII connectivity.
FlexCAN(2)	Controller area network module	Connectivity peripherals	The Controller Area Network (CAN) protocol is a message based protocol used for serial data. It was designed specifically for automotive but is also used in industrial control and medical applications. The serial data bus runs at 1 Mbps.
GPMI	General-purpose media interface	Connectivity peripherals	The General-Purpose Media Interface (GPMI) controller is a flexible NAND Flash controller with 8-bit data width, up to 50-MBps I/O speed and individual chip select and DMA channels for up to 8 NAND devices. It also provides a interface to 20-bit BCH for ECC.
HSADC	High-speed ADC	Connectivity peripherals	The high-speed ADC block is designed to sample an analog input with 12-bit resolution and a sample rate of up to 2 Msps. The output of the HSADC block can be moved to the external memory through APBH-DMA. A typical user case of the HSADC is to work with the PWM block to drive an external linear image scanner sensor.
I^2C(2)	I^2C module	Connectivity peripherals	The I^2C is a standard two-wire serial interface used to connect the chip with peripherals or host controllers. The I^2C operates up to 400 kbps in either I^2C master or I^2C slave mode. Each I^2C has a dedicated DMA channel and can also controlled by CPU in PIO or PIO queue modes. It supports both 7-bit and 10-bit device address in master mode, and has programmable 7-bit address in slave mode.
ICOLL	Interrupt Collector	System control	The ARM9 CPU core has two interrupt input lines, IRQ and FIQ. The interrupt collector (ICOLL) can steer any of 128 interrupt sources to either the FIQ or IRQ line of the ARM9 CPU.
L2 Switch	3-Port L2 Switch	Network Control	Programmable 3-Port Ethernet Switch with QOS

Table 4. i.MX28 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
RTC	Real-time clock, alarm, watchdog	Clocks	The real-time clock (RTC) and alarm share a one-second pulse time domain. The watchdog reset and millisecond counter run on a one-millisecond time domain. The RTC, alarm, and persistent bits reside in a special power domain (crystal domain) that remains powered up even when the rest of the chip is in its powered-down state.
SAIF(2)	Serial audio interface	Connectivity peripherals	SAIF provides a half-duplex serial port for communication with a variety of serial devices, including industry-standard codecs and DSPs. It supports a continuous range of sample rates from 8 kHz–192 kHz using a high-resolution fractional divider driven by the PLL. Samples are transferred to/from the FIFO through the APBX DMA interface, a FIFO service interrupt, or software polling.
SPDIF	SPDIF	Connectivity peripherals	The Sony-Philips Digital Interface Format (SPDIF) transmitter module transmits data according to the SPDIF digital audio interface standard (IEC-60958).
SSP(4)	Synchronous serial port	Connectivity peripherals	The synchronous serial port is a flexible interface for inter-IC and removable media control and communication. The SSP supports master operation of SPI, Texas Instruments SSI; 1-bit, 4-bit, and 8-bit SD/SDIO/MMC and 1-bit and 4-bit MS modes. The SPI mode has enhancements to support 1-bit legacy MMC cards. SPI master dual (2-bit) and quad (4-bit) mode reads are also supported. The SSP also supports slave operation for the SPI and SSI modes. The SSP has a dedicated DMA channel in the bridge and can also be controlled directly by the CPU through PIO registers. Each of the four SSP modules is independent of the other and can have separate SSPCLK frequencies.
TIMROT	Timers and Rotary Decoder	Timer peripherals	This module implements four timers and a rotary decoder. The timers and decoder can take their inputs from any of the pins defined for PWM, rotary encoders, or certain divisions from the 32-kHz clock input. Thus, the PWM pins can be inputs or outputs, depending on the application.
USBOTG USBHOST	High-speed USB on-the-go	Connectivity peripherals	The USB module provides high-performance USB On-The-Go (OTG) and host functionality (up to 480 Mbps), compliant with the USB 2.0 specification and the OTG supplement. The module has DMA capabilities for handling data transfer between internal buffers and system memory. When the OTG controller works in device mode, it can only work in FS or HS mode. Two USB2.0 PHYs are also integrated (one for the OTG port, another for the host port.)
USBPHY	Integrated USB PHY	Connectivity peripherals	The integrated USB 2.0 PHY macrocells are capable of connecting to USB host/device systems at the USB low-speed (LS) rate of 1.5 Mbps, full-speed (FS) rate of 12 Mbps or at the USB 2.0 high-speed (HS) rate of 480 Mbps. The integrated PHYs provide a standard UTM interface. The USB_DP and USB_DN pins connect directly to a USB connector.

Table 20. Power Mode Settings (continued)

Core/Clock/Module	Offstate	Standby	Run
OSC32K	On	On	On
DCDC	Off	On	On
RTC	On	On	On
Other Modules	Off	On/Off	On/Off

3.1.6 Supply Power-Up/Power-Down Requirements

There is no special power-up sequence. After applying 5 V or battery in any order, the rest of the power supplies are internally generated and automatically come up in a safe way.

There is no special power-down sequence. 5 V or the battery can be removed at any time.

3.1.7 Reset Timing

Because the i.MX28 is a PMU and an SoC, power-on reset is generated internally and there is no timing requirement on external pins.

The i.MX28 can be reset by asserting the external pin RESETN for at least 100 mS and later deasserting RESETN.

If the reset occurs while the device is only powered by the battery, then the reset kills all of the power supplies and the system reboots on the assertion of PSWITCH. If auto-restart is set up ahead of time, the system reboots immediately.

If the chip is powered by 5 V, then the reset serves to reset the digital sections of the chip. If the DCDC is operating at the time of the reset, then power switches back to the default linear regulators powered by 5 V.

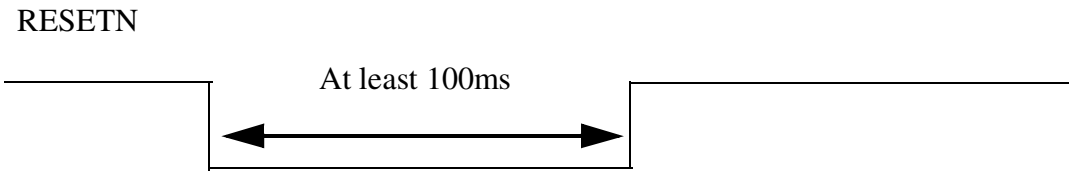

Figure 2. RESETN Timing

3.2 Thermal Characteristics

The thermal resistance characteristics for the device are given in Table 21. These values are measured under the following conditions:

- Two layer Substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.160 mm

- Core via I.D: 0.068 mm, Core via plating 0.016 mm
- Flag: trace style with ground balls under the die connected to the flag
- Die Attach: 0.033 mm non-conductive die attach, k = 0.3 W/m K
- Mold Compound: generic mold compound, k = 0.9 W/m K

Table 21. Thermal Resistance Data

Rating			Value	Unit
Junction to ambient[1] natural convection	Single layer board (1s)	$R_{\theta JA}$	62	°C/W
Junction to ambient[1] natural convection	Four layer board (2s2p)	$R_{\theta JA}$	36	°C/W
Junction to ambient[1] (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	53	°C/W
Junction to ambient[1] (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	33	°C/W
Junction to boards[2]		$R_{\theta JB}$	24	°C/W
Junction to case (top)[3]		$R_{\theta JCtop}$	15	°C/W
Junction to package top[4]	Natural Convection	Ψ_{JT}	3	°C/W

1 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-2 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- DDR I/O: Mobile DDR (LPDDR1), standard 1.8 V DDR2, and low-voltage 1.5 V DDR2 (LVDDR2)
- General purpose I/O (GPIO)

3.3.1 DDR I/O DC Parameters

Table 22 shows the EMI digital pin DC characteristics.

NOTE

The current values and the I-V curves of the I/O DC characteristics are estimated based on an overly conservative device model. They are updated upon the measurement results of the first silicon.

Table 24 shows the external devices supported by the EMI.

Table 24. External Devices Supported by the EMI

DRAM Device	Max Load[1, 2]	Pad Voltage
DDR2	15 pF	1.8 V
mDDR	15 pF	1.8 V
LVDDR2	15 pF	1.5 V

1 Max load includes capacitive load due to PCB traces, pad capacitance and driver self-loading.

2 Setting is for worst case. Freescale's EMI interface uses less powerful drivers than those typically used in mDDR devices. A possible transmission-line effect on the PC board must be suppressed by minimizing the trace length combined with Freescale's slower edge-rate drivers. The i.MX28 provides up to 16 mA programmable drive strength. However, the 16-mA mode is an experimental mode. With the 16-mA mode, the EMI function may be impaired by Simultaneous Switching Output (SSO) noise. In general, the stronger the driver mode, the noisier the on-chip power supply. Freescale recommends not using a stronger driver mode than is required. Because on-chip power and ground noise is proportional to the inductance of its return path, users should make their best effort to reduce inductance between the EMI power and ground balls and the PC board power and ground planes.

3.3.2 GPIO I/O DC Parameters

Max load includes capacitive load due to PCB traces, pad capacitance and driver self-loading. For the internal pull up setting of each pad, see the "Pin Control and GPIO" section of the reference manual.

Table 25 shows the digital pin DC characteristics for GPIO in 3.3-V mode. Measurements are valid for eight pins loaded using the 4mA driver, four pins loaded using the 8mA driver, and two pins loaded using either the 12mA or 16mA driver.

Table 25. Digital Pin DC Characteristics for GPIO in 3.3-V Mode

Parameter	Symbol	Min	Max	Unit
Input voltage high (dc)	VIH	2	VDDIO	V
Input voltage low (dc)	VIL	—	0.8	V
Output voltage high (dc)	VOH	0.8 × VDDIO	—	V
Output voltage low (dc)	VOL	—	0.4	V
Output source current[1] (dc) *gpio*	IOH – Low	-5.0	—	mA
	IOH – Medium	-9.5	—	mA
	IOH – High	-11.4	—	mA
Output sink current (dc) *gpio*	IOL – Low	3.8	—	mA
	IOL – Medium	7.7	—	mA
	IOL – High	9.0	—	mA
Output source current (dc) *gpio_clk*	IOH – Low	-9.2	—	mA
	IOH – High	-15.2	—	mA
Output sink current (dc) *gpio_clk*	IOL – Low	7.6	—	mA
	IOL – High	12.0	—	mA

3.5.3 EMI AC Timing

This section includes descriptions of the electrical specifications of EMI module which interfaces external DDR2 and Mobile-DDR1 (LP-DDR1) memory devices.

3.5.3.1 EMI Command and Address AC Timing

Figure 5 and Table 34 specify the timing related to the address and command pins that interfaces DDR2 and Mobile-DDR1 memory devices.

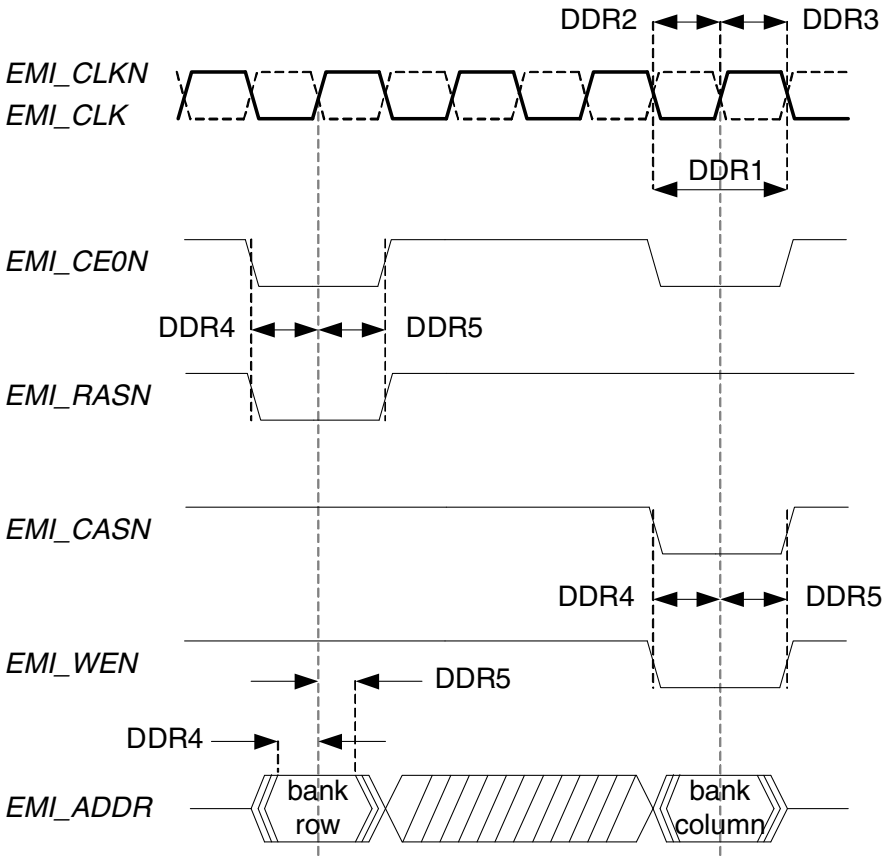

Figure 5. EMI Command/Address AC Timing

Table 34. EMI Command/Address AC Timing

ID	Description	Symbol	Min.	Max.	Unit
DDR1	CK cycle time	tCK	4.86	—	ns
DDR2	CK high level width	tCH	0.5 tCK –0.5	0.5 tCK + 0.5	ns
DDR3	CK low level width	tCL	0.5 tCK –0.5	0.5 tCK + 0.5	ns

3.5.3.4 LPDDR1 Input AC Timing

Figure 8 and Table 37 show input AC timing for LPDDR1.

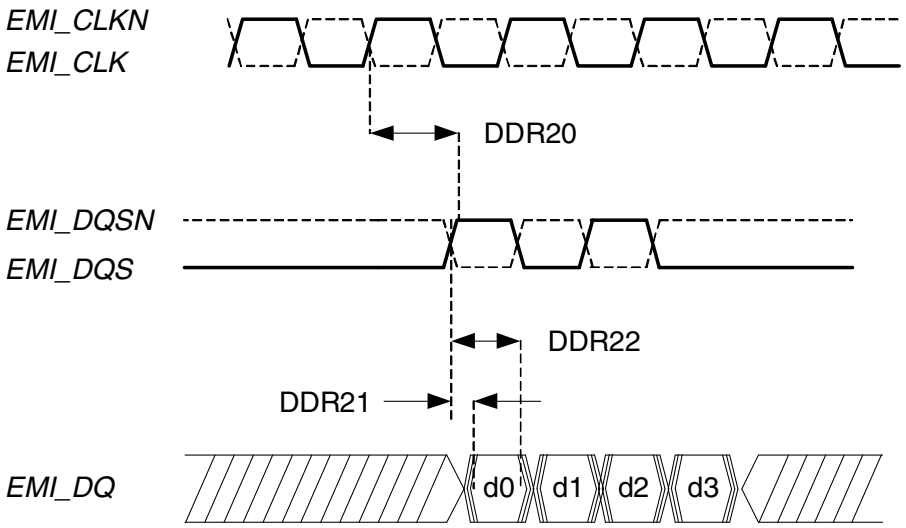

Figure 8. LPDDR1 Input AC Timing

Table 37. DDR2 Input AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR20	Positive DQS latching edge to associated CK edge	tDQSCK	2	6	ns
DDR21	DQS to DQ input skew	tDQSQ	0.25 tCK –0.85	0.25 tCK –0.5	ns
DDR22	DQS to DQ input hold time	tQH	0.25 tCK +0.75	0.25 tCK + 1	ns

3.5.4 Ethernet MAC Controller (ENET) Timing

The ENET is designed to support both 10- and 100-Mbps Ethernet networks compliant with IEEE 802.3. An external transceiver interface and transceiver function are required to complete the interface to the media. The ENET supports 10/100-Mbps MII (18 pins altogether), 10/100-Mbps RMII (10 pins, including serial management interface), for connection to an external Ethernet transceiver. All signals are compatible with transceivers operating at a voltage of 3.3 V.

The following subsections describe the timing for MII and RMII modes.

Figure 10 shows MII transmit signal timings. Table 39 describes the timing parameters (M5–M8) shown in the figure.

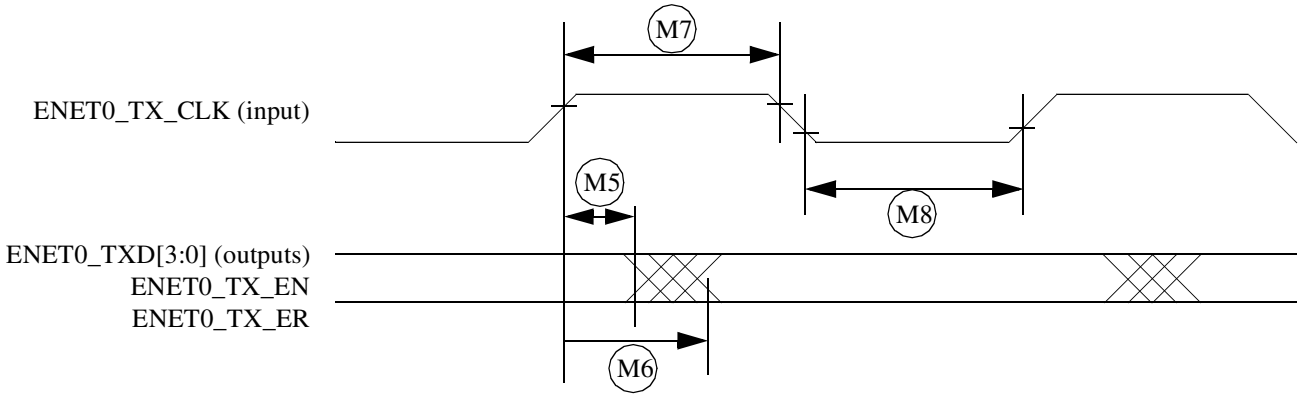

Figure 10. MII Transmit Signal Timing Diagram

Table 39. MII Transmit Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M5	ENET0_TX_CLK to ENET0_TXD[3:0], ENET0_TX_EN, ENET0_TX_ER invalid	5	—	ns
M6	ENET0_TX_CLK to ENET0_TXD[3:0], ENET0_TX_EN, ENET0_TX_ER valid	—	20	ns
M7	ENET0_TX_CLK pulse width high	35%	65%	ENET0_TX_CLK period
M8	ENET0_TX_CLK pulse width low	35%	65%	ENET0_TX_CLK period

[1] ENET0_TX_EN, ENET0_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

3.5.4.1.3 MII Asynchronous Inputs Signal Timing (ENET0_CRS and ENET0_COL)

Figure 11 shows MII asynchronous input timings. Table 40 describes the timing parameter (M9) shown in the figure.

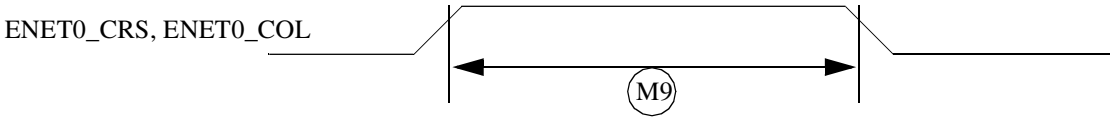

Figure 11. MII Async Inputs Timing Diagram

Table 40. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	ENET0_CRS to ENET0_COL minimum pulse width	1.5	—	ENET0_TX_CLK period

[1] ENET0_COL has the same timing in 10-Mbit 7-wire interface mode.

Table 47. NFC Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Example Timing for GPMI Clock ≈ 100MHz T = 10ns		Unit
			Min.	Max.	Min.	Max.	
NF1	CLE setup time	tCLS	(AS+1)*T	—	10	—	ns
NF2	CLE hold time	tCLH	(DH+1)*T	—	20	—	ns
NF3	$\overline{CEn}$ setup time	tCS	(AS+1)*T	—	10	—	ns
NF4	$\overline{CE}$ hold time	tCH	(DH+1)*T	—	20	—	ns
NF5	$\overline{WE}$ pulse width	tWP	DS*T		10		ns
NF6	ALE setup time	tALS	(AS+1)*T	—	10	—	ns
NF7	ALE hold time	tALH	(DH+1)*T	—	20	—	ns
NF8	Data setup time	tDS	DS*T	—	10	—	ns
NF9	Data hold time	tDH	DH*T	—	10	—	ns
NF10	Write cycle time	tWC	(DS+DH)*T		20		ns
NF11	$\overline{WE}$ hold time	tWH	DH*T		10		ns
NF12	Ready to $\overline{RE}$ low	tRR	(AS+1)*T	—	10	—	ns
NF13	$\overline{RE}$ pulse width	tRP	DS*T	—	10	—	ns
NF14	READ cycle time	tRC	(DS+DH)*T	—	20	—	ns
NF15	$\overline{RE}$ high hold time	tREH	DH*T		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

[1] The Flash clock maximum frequency is 100 MHz.

2)GPMI's output timing could be controlled by module's internal register, say HW_GPMI_TIMING0_ADDRESS_SETUP,HW_GPMI_TIMING0_DATA_SETUP,HW_GPMI_TIMING0_DATA_HOLD, this AC timing depends on these registers' setting. In the above table we use AS/DS/DH representing these settings each.

3)AS minimum value could be 0, while DS/DH minimum value is 1.

Table 53. PWM Output Timing Parameter: MATT Mode 24 MHz Crystal Clock

Ref No.	Parameter	Minimum	Maximum	Unit
1	System CLK frequency[1]	24	24	MHz
2a	Clock high time	20.99	—	ns
2b	Clock low time	21.01	—	ns
3a	Clock fall time	—	0.3	ns
3b	Clock rise time	—	0.3	ns
4a	Output delay time	—	15.23	ns
4b	Output setup time	15.92	—	ns

[1] CL of PWMO = 30 pF

3.5.12 Serial Audio Interface (SAIF) AC Timing

The following subsections describe SAIF timing in two cases:

- Transmitter
- Receiver

3.5.12.1 SAIF Transmitter Timing

Figure 33 shows the timing for SAIF transmitter with internal clock, and Table 54 describes the timing parameters (SS1–SS13).

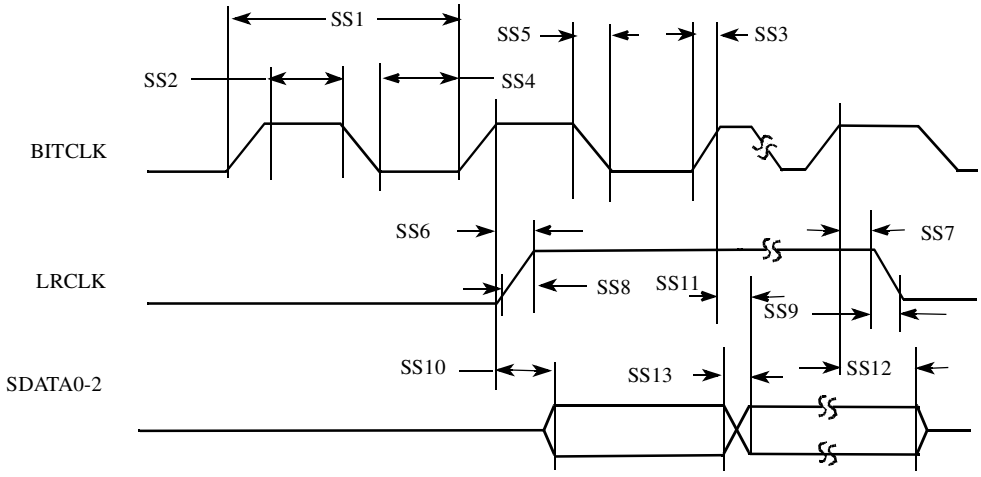

Figure 33. SAIF Transmitter Timing Diagram

3.5.14 Synchronous Serial Port (SSP) AC Timing

This section describes the electrical information of the SSP, which includes SD/MMC4.3 (Single Data Rate) timing, MMC4.4 (Dual Date Rate) timing, MS (Memory Stick) timing, and SPI timing.

3.5.14.1 SD/MMC4.3 (Single Data Rate) AC Timing

Figure 36 depicts the timing of SD/MMC4.3, and Table 57 lists the SD/MMC4.3 timing characteristics.

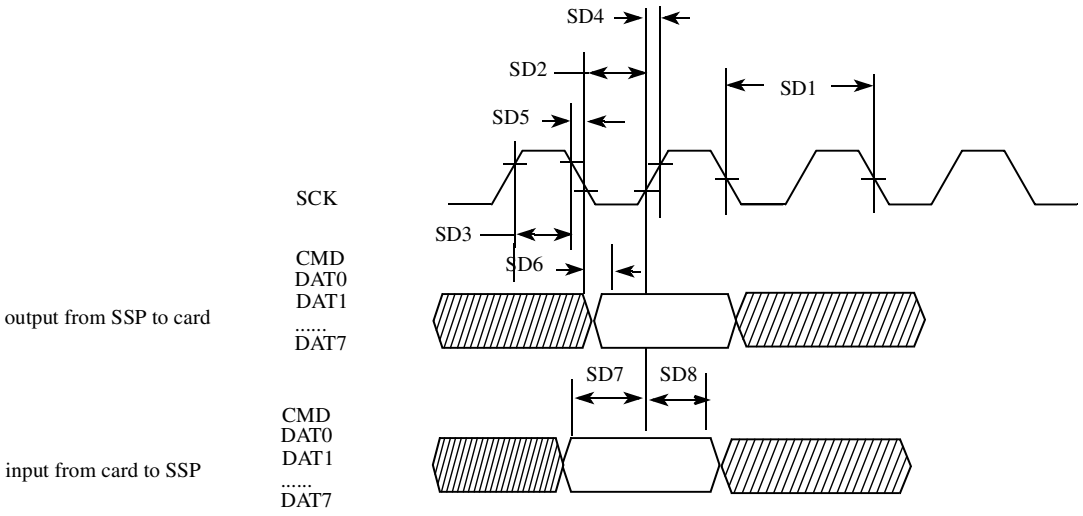

Figure 36. SD/MMC4.3 Timing

Table 57. SD/MMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
SSP Output / Card Inputs CMD, DAT (Reference to CLK)					
SD6	SSP Output Delay	t_{OD}	-5	5	ns
SSP Input / Card Outputs CMD, DAT (Reference to CLK)					

3.5.14.3 MS (Memory Stick) AC Timing

The SSP module, which also has the function of a memory stick host controller, is compatible with the Sony Memory Stick version 1.x and Memory Stick PRO.

Figure 38, Figure 39 and Table 40 show the timing of the Memory Stick. Table 59 and Table 60 list the Memory Stick timing characteristics.

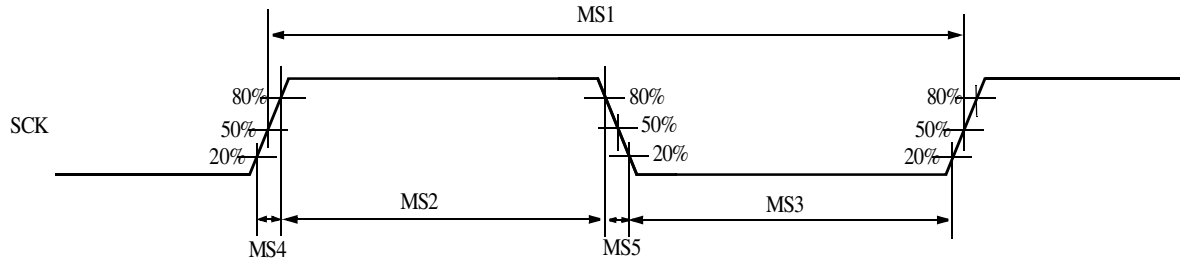

Figure 38. MS Clock Time Waveforms

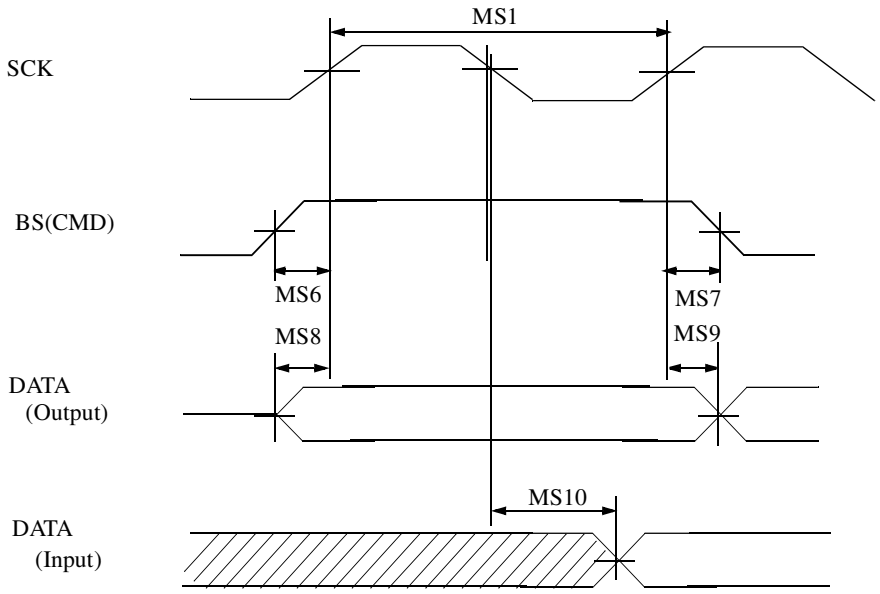

Figure 39. MS Serial Transfer Mode Timing Diagram

Table 60. MS Parallel Transfer Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
MS5	SCK Fall Time	tCLKf	—	10	ns
MS11	BS Setup Time	tBSsu	8	—	ns
MS12	BS Hold Time	tBSh	1	—	ns
MS13	DATA Setup Time	tDsu	8	—	ns
MS14	DATA Hold Time	tDh	1	—	ns
MS15	DATA Input Delay Time	tDd	—	15	ns

3.5.14.4 SPI AC Timing

Figure 41 depicts the master mode and slave mode timings of the SPI, and Table 61 lists the timing parameters.

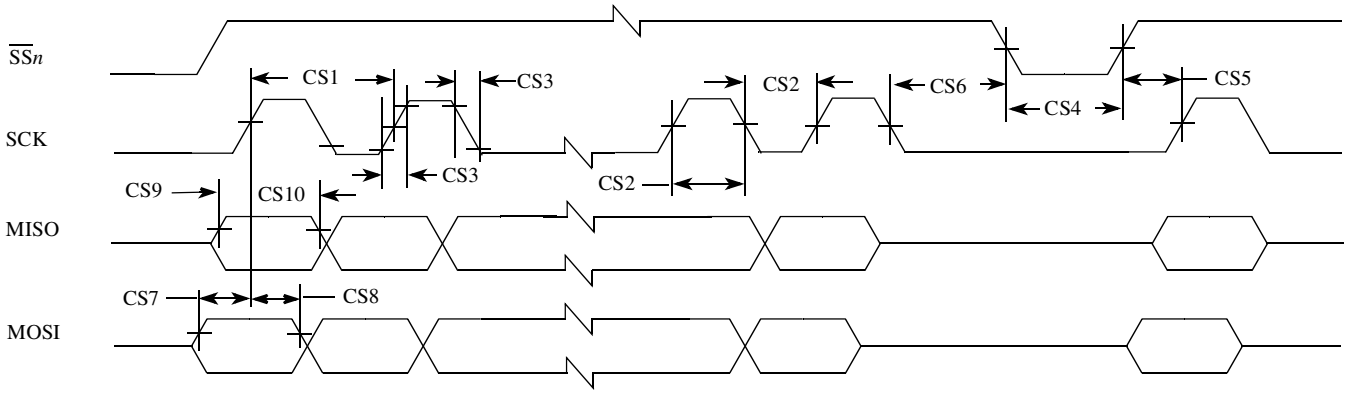

Figure 41. SPI Interface Timing Diagram

Table 61. SPI Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
CS1	SCK cycle time	t_{clk}	50	—	ns
CS2	SCK high or low time	t_{SW}	25	—	ns
CS3	SCK rise or fall	$t_{RISE/FALL}$	—	7.6	ns
CS4	$\overline{SS}n$ pulse width	t_{CSLH}	25	—	ns
CS5	$\overline{SS}n$ lead time (CS setup time)	t_{SCS}	25	—	ns
CS6	$\overline{SS}n$ lag time (CS hold time)	t_{HCS}	25	—	ns
CS7	MOSI setup time	t_{Smosi}	5	—	ns
CS8	MOSI hold time	t_{Hmosi}	5	—	ns
CS9	MISO setup time	t_{Smiso}	5	—	ns
CS10	MISO hold time	t_{Hmiso}	5	—	ns

Table 63. UART Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
UA2	Receive bit time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UARTAPP can support is 3.25 Mbps. The maximum baud rate of DebugUART is 115 kbps.

4 Package Information and Contact Assignments

4.1 Case MAPBGA-289, 14 x 14 mm, 0.8 mm Pitch

The following notes apply to Figure 44:

- All dimensions are in millimeters.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Maximum solder bump diameter measured parallel to datum A.
- Datum A, the seating plane, is determined by the spherical crowns of the solder bumps.
- Parallelism measurement excludes any effect of mark on top surface of package.

Table 68. 289-Pin i.MX286 MAPBGA Ball Map (continued)

K	J	H	G	F	E	D	C	B
LCD_WR_RWN	NC	ENET0_RXD0	NC	ENET0_TXD0	NC	NC	NC	NC
LCD_D00	NC	ENET0_RXD1	NC	ENET0_TXD1	ENET_CLK	NC	NC	NC
LCD_D01	NC	VSS	VDDIO33	NC	NC	SSP2_SS1	SSP2_MOSI	SSP2_MISO
AUART1_TX	NC	ENET0_MDIO	ENET0_MDC	ENET0_TX_EN	ENET0_RX_EN	SSP2_SS2	SSP2_SS0	SSP0_DATA7
NC	NC	AUART0_TX	AUART0_RX	NC	VSS	SSP0_DATA6	SSP0_DATA5	SSP0_DATA4
NC	AUART0_CTS	NC	SAIF0_LRCLK	NC	VDDIO33	SSP0_DATA2	SSP0_DATA1	SSP0_DATA0
PWM0	AUART0_RTS	NC	SAIF0_MCLK	SAIF0_BITCLK	SAIF0_SDATA0	SPDIF	I2C0_SCL	VSS
PWM2	VDDIO33	VDDIO33	VDDIO18	VDDIO18	SAIF1_SDATA0	I2C0_SDA	LRADC2	USB1DM
VSS	VDDIO33	VSS	VDDIO18	VDDIO18	PWM3	LRADC3	LRADC1	DEBUG
VSS	VDDIO33	VSS	VDDD	VDDD	PWM4	SSP0_DETECT	TESTMODE	USB0DP
VSS	VSS	VSS	VDDD	VDDD	JTAG_TCK	RTC_XTALI	RTC_XTALO	VSSA2
VDDD	VSS	VSS	VDDD	VDDD	JTAG_TDI	JTAG_TMS	VDDXTAL	XTALO
EMI_VREF1	VDDIO_EMIQ	EMI_D12	VDDIO_EMI	EMI_D14	JTAG_TDO	LRADC4	VDDA1	VSSA1
EMI_DDR_OPEN	EMI_D11	VSSIO_EMI	EMI_D10	VSSIO_EMI	JTAG_RTCK	JTAG_TRST	LRADC6	HSADC0
VDDIO_EMIQ	VSS	EMI_D09	VDDIO_EMI	EMI_DQM1	VSS	LRADC5	LRADC0	DCDC_BATT
EMI_DQS0N	EMI_DQS1N	VSS	EMI_D08	VSSIO_EMI	VDDIO33	VDD1P5	VSS	DCDC_VDDA
EMI_DQS0	EMI_DQS1	EMI_D13	VDDIO_EMI	EMI_D15	VDD5V	DCDC_VDDD	DCDC_VDDIO	DCDC_LN1
K	J	H	G	F	E	D	C	B

Table 68. 289-Pin i.MX286 MAPBGA Ball Map (continued)

	U	T	R	P	N	M	L
1	VSS	LCD_D12	LCD_D10	LCD_D07	NC	NC	NC
2	LCD_D14	LCD_D13	LCD_D11	LCD_D08	LCD_D06	LCD_D04	LCD_D02
3	LCD_D15	LCD_D16	LCD_D17	LCD_D09	VDDIO33	LCD_D05	LCD_D03
4	LCD_D18	LCD_D19	LCD_D20	LCD_RD_E	VSS	LCD_RS	AUART1_RX
5	LCD_D21	LCD_D22	LCD_D23	LCD_CS	NC	NC	NC
6	GPMI_D06	GPMI_D07	GPMI_RDN	GPMI_ALE	GPMI_RDY0	LCD_RESET	NC
7	GPMI_D03	GPMI_D04	GPMI_D05	GPMI_CLE	GPMI_CE0N	GPMI_CE2N	PWM1
8	GPMI_D00	GPMI_D01	GPMI_D02	GPMI_WRN	GPMI_RDY1	GPMI_RDY2	GPMI_RDY3
9	EMI_A08	EMI_A13	EMI_A06	EMI_CE1N	GPMI_CE1N	GPMI_CE3N	GPMI_RESETN
10	EMI_A04	EMI_A11	VSSIO_EMI	EMI_A09	EMI_A14	VDDIO_EMI	VSS
11	EMI_A12	EMI_A03	EMI_A05	VDDIO_EMI	EMI_A07	VDDIO_EMI	VSS
12	EMI_A01	EMI_BA1	VSSIO_EMI	EMI_CE0N	EMI_BA2	VDDIO_EMI	VSSIO_EMI
13	EMI_A10	EMI_CKE	VDDIO_EMI	EMI_D04	VDDIO_EMI	EMI_D01	VDDIO_EMI
14	EMI_A02	VSSIO_EMI	EMI_VREF0	VSSIO_EMI	EMI_D03	VSS	EMI_D06
15	EMI_A00	EMI_WEN	VDDIO_EMIQ	EMI_D02	VDDIO_EMI	EMI_DQM0	EMI_DDR_OPEN_FB
16	EMI_CASN	EMI_BA0	EMI_RASN	VSSIO_EMI	EMI_D00	VSSIO_EMI	EMI_CLKN
17	VSSIO_EMI	EMI_ODT1	EMI_ODT0	EMI_D05	VDDIO33_EMI	EMI_D07	EMI_CLK
	U	T	R	P	N	M	L

4.7 i.MX287 Ball Map

Table 69 shows the i.MX287 MAPBGA Ball Map.

Table 69. 289-Pin i.MX287 MAPBGA Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VSS	SSP3_SCK	SSP2_SCK	SSP0_CMD	SSP0_DATA3	SSP0_SCK	VDDIO33	USB1DP	VSS	USB0DM	PSWITCH	XTALI	VDD4P2	RESETN	BATTERY	DCDC_LP	DCDC_GND	A

Table 70. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 0	09/2010	Initial release.