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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOIJ
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12c671t-04i-sm

TABLE 4-1: PIC12C67X SPECIAL FUNCTION REGISTER SUMMARY (CONT.)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other Resets[3]
Bank 1											
80h[1]	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h[1]	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h[1]	STATUS	IRP[4]	RP1[4]	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
84h[1]	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRIS	—	—	GPIO Data Direction Register						--11 1111	--11 1111
86h	—	Unimplemented								—	—
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah[1,2]	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the PC					---0 0000	---0 0000
8Bh[1]	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 000x	0000 000u
8Ch	PIE1	—	ADIE	—	—	—	—	—	—	-0-- ----	-0-- ----
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	—	—	—	$\overline{\text{POR}}$	—	---- --0-	---- --u-
8Fh	OSCCAL	CAL3	CAL2	CAL1	CAL0	CALFST	CALSLW	—	—	0111 00--	uuuu uu--
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	—	Unimplemented								—	—
93h	—	Unimplemented								—	—
94h	—	Unimplemented								—	—
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	—	Unimplemented								—	—
99h	—	Unimplemented								—	—
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	—	Unimplemented								—	—
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.
Shaded locations are unimplemented, read as ‘0’.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non power-up) resets include external reset through $\overline{\text{MCLR}}$ and Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC12C67X; always maintain these bits clear.

5: The SCL (GP7) and SDA (GP6) bits are unimplemented on the PIC12C671/672 and read as ’0’.

FIGURE 5-2: BLOCK DIAGRAM OF GP2/T0CKI/AN2/INT PIN

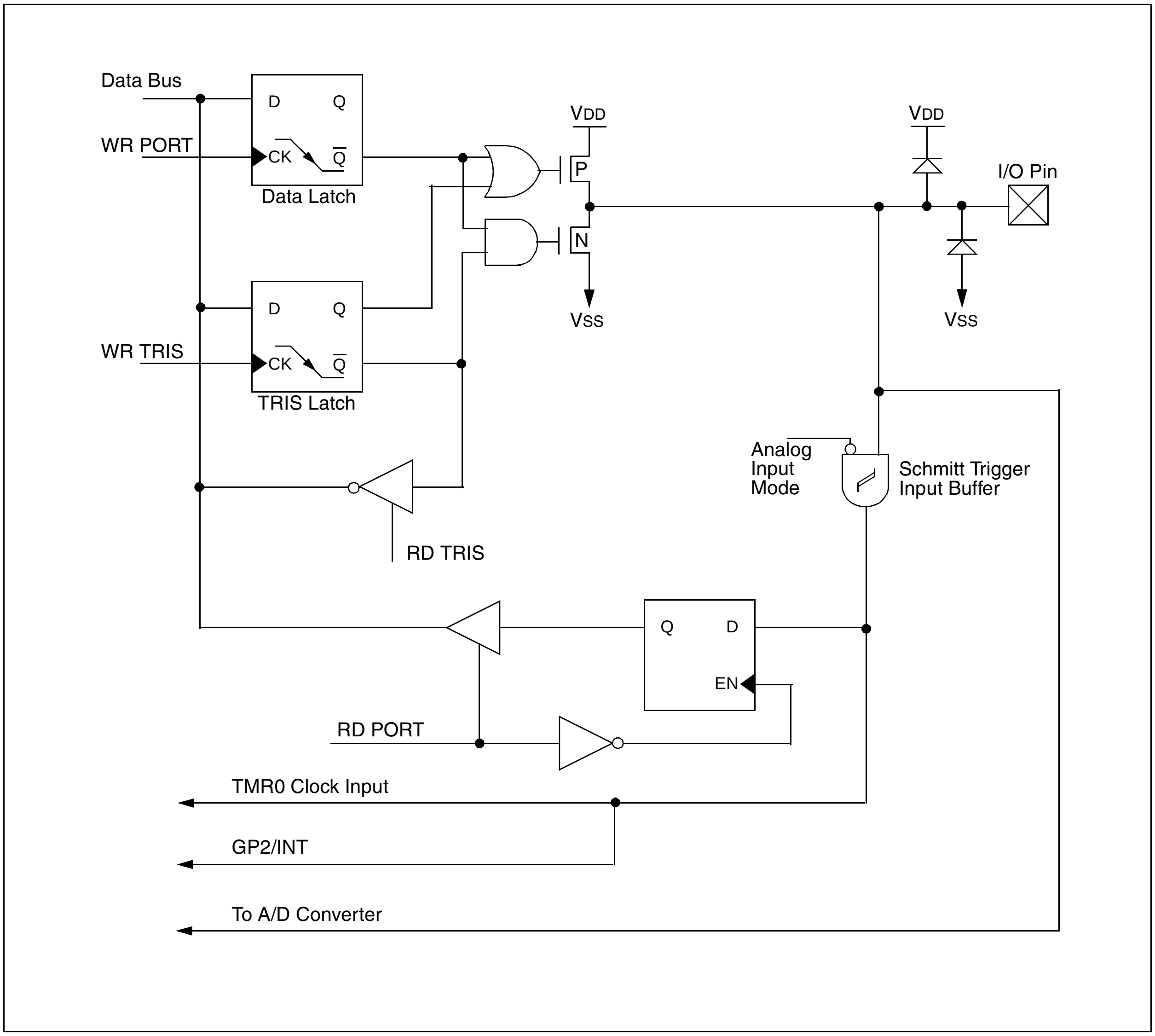
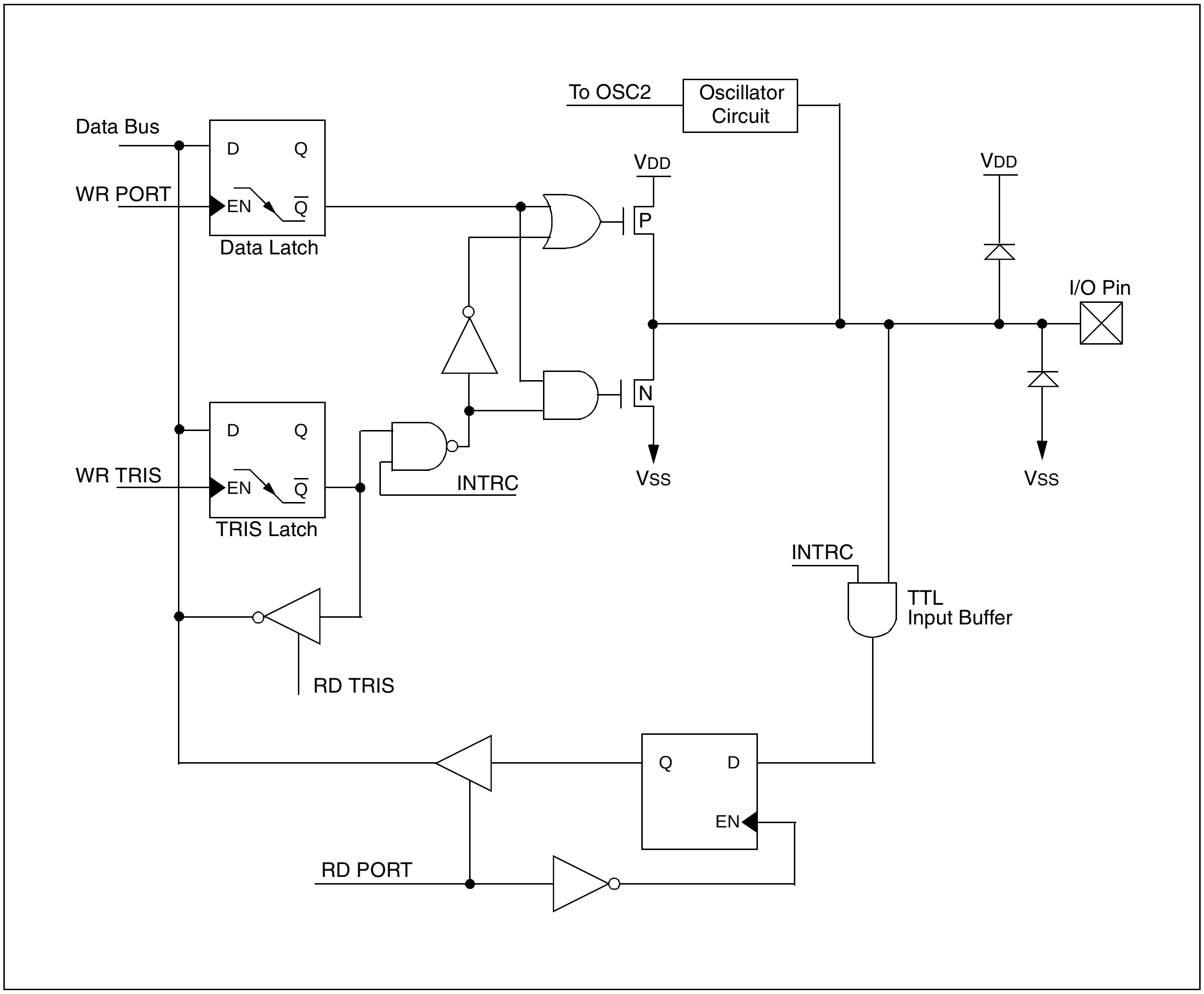


FIGURE 5-5: BLOCK DIAGRAM OF GP5/OSC1/CLKIN PIN



NOTES:

NOTES:

8.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-To-Digital (A/D) converter module has four analog inputs.

The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number (refer to Application Note AN546 for use of A/D Converter). The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (V_{DD}) or the voltage level on the GP1/AN1/V_{REF} pin. The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode.

The A/D module has three registers. These registers are:

- A/D Result Register (ADRES)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 Register, shown in Figure 8-1, controls the operation of the A/D module. The ADCON1 Register, shown in Figure 8-2, configures the functions of the port pins. The port pins can be configured as analog inputs (GP1 can also be a voltage reference) or as digital I/O.

> **Note 1:** If the port pins are configured as analog inputs (reset condition), reading the port (MOVF GPIO,W) results in reading '0's.
>
> **2:** Changing ADCON1 Register can cause the GPIF and INTF flags to be set in the INTCON Register. These interrupts should be disabled prior to modifying ADCON1.

REGISTER 8-1: ADCON0 REGISTER (ADDRESS 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	reserved	CHS1	CHS0	GO/$\overline{\text{DONE}}$	reserved	ADON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **ADCS<1:0>:** A/D Conversion Clock Select bits
`00` = $F_{OSC}/2$
`01` = $F_{OSC}/8$
`10` = $F_{OSC}/32$
`11` = F_{RC} (clock derived from an RC oscillation)

bit 5: **Reserved**

bit 4-3: **CHS<1:0>:** Analog Channel Select bits
`00` = channel 0, (GP0/AN0)
`01` = channel 1, (GP1/AN1)
`10` = channel 2, (GP2/AN2)
`11` = channel 3, (GP4/AN3)

bit 2: **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
If ADON = 1
`1` = A/D conversion in progress (setting this bit starts the A/D conversion)
`0` = A/D conversion not in progress (this bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1: **Reserved**

bit 0: **ADON:** A/D on bit
`1` = A/D converter module is operating
`0` = A/D converter module is shut off and consumes no operating current

8.4 A/D Conversions

Example 8-2 shows how to perform an A/D conversion. The GPIO pins are configured as analog inputs. The analog reference (VREF) is the device VDD. The A/D interrupt is enabled and the A/D conversion clock is FRC. The conversion is performed on the GP0 channel.

Note:	The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The ADRES register will NOT be updated with the partially completed A/D conversion sample. That is, the ADRES register will continue to contain the value of the last completed conversion (or the last value written to the ADRES register). After the A/D conversion is aborted, a 2TAD wait is required before the next acquisition is started. After this 2TAD wait, an acquisition is automatically started on the selected channel.

EXAMPLE 8-2: DOING AN A/D CONVERSION

```
     BSF      STATUS, RP0         ; Select Page 1
     CLRF     ADCON1              ; Configure A/D inputs
     BSF      PIE1,   ADIE        ; Enable A/D interrupts
     BCF      STATUS, RP0         ; Select Page 0
     MOVLW    0xC1                ; RC Clock, A/D is on, Channel 0 is selected
     MOVWF    ADCON0              ;
     BCF      PIR1,   ADIF        ; Clear A/D interrupt flag bit
     BSF      INTCON, PEIE        ; Enable peripheral interrupts
     BSF      INTCON, GIE         ; Enable all interrupts
;
;  Ensure that the required sampling time for the selected input channel has elapsed.
;  Then the conversion may be started.
;
     BSF      ADCON0, GO          ; Start A/D Conversion
       :                          ; The ADIF bit will be set and the GO/DONE bit
       :                          ;  is cleared upon completion of the A/D Conversion.
```

9.7 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip RC oscillator, which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a `SLEEP` instruction. During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The WDT can be permanently disabled by clearing configuration bit WDTE (Section 9.1).

9.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The `CLRWDT` and `SLEEP` instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out early and generating a premature device RESET condition.

The $\overline{\text{TO}}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

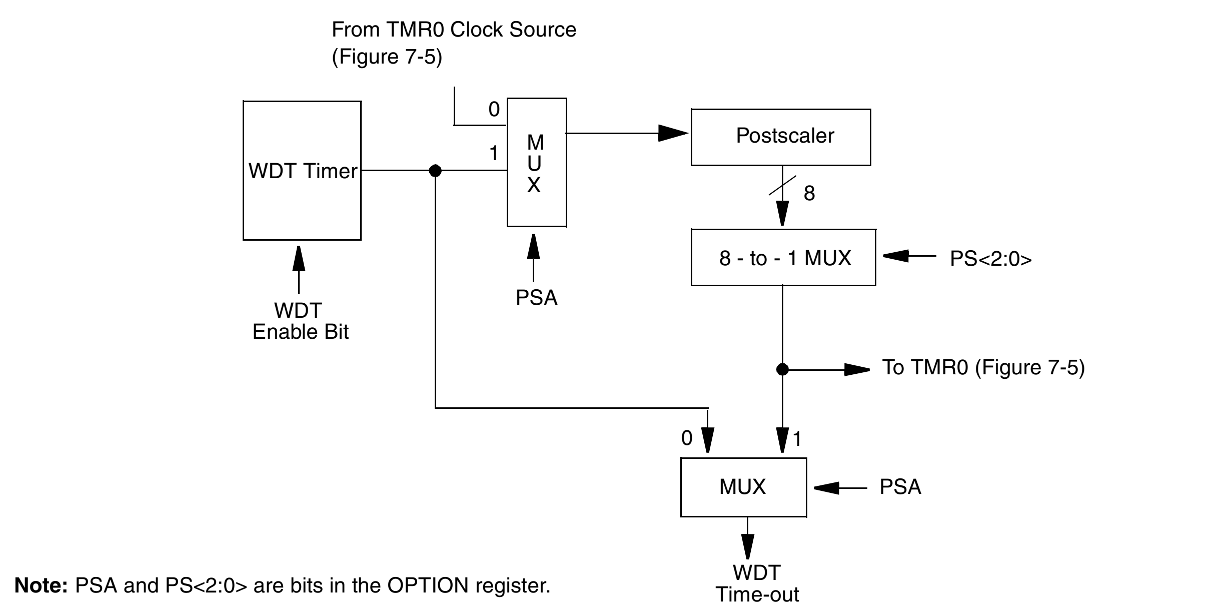
9.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (VDD = Min., Temperature = Max., and max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

> **Note:** When the prescaler is assigned to the WDT, always execute a `CLRWDT` instruction before changing the prescale value, otherwise a WDT reset may occur.

See Example 7-1 and Example 7-2 for changing prescaler between WDT and Timer0.

FIGURE 9-15: WATCHDOG TIMER BLOCK DIAGRAM



Note: PSA and PS<2:0> are bits in the OPTION register.

TABLE 9-8: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits(1)	MCLRE	CP1	CP0	$\overline{\text{PWRTE}}$	$\overline{\text{WDTE}}$	FOSC2	FOSC1	FOSC0
81h	OPTION	$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.
Note 1: See Register 9-1 for operation of these bits. Not all CP0 and CP1 bits are shown.

10.1 Special Function Registers as Source/Destination

The PIC12C67X's orthogonal instruction set allows read and write of all file registers, including special function registers. There are some special situations the user should be aware of:

10.1.1 STATUS AS DESTINATION

If an instruction writes to STATUS, the Z, C and DC bits may be set or cleared as a result of the instruction and overwrite the original data bits written. For example, executing `CLRF STATUS` will clear register STATUS, and then set the Z bit leaving `0000 0100b` in the register.

10.1.2 TRIS AS DESTINATION

Bit 3 of the TRIS register always reads as a '1' since GP3 is an input only pin. This fact can affect some read-modify-write operations on the TRIS register.

10.1.3 PCL AS SOURCE OR DESTINATION

Read, write or read-modify-write on PCL may have the following results:

Read PC:	PCL $\rightarrow$ dest
Write PCL:	PCLATH $\rightarrow$ PCH; 8-bit destination value $\rightarrow$ PCL
Read-Modify-Write:	PCL$\rightarrow$ ALU operand PCLATH $\rightarrow$ PCH; 8-bit result $\rightarrow$ PCL

Where PCH = program counter high byte (not an addressable register), PCLATH = Program counter high holding latch, dest = destination, WREG or f.

10.1.4 BIT MANIPULATION

All bit manipulation instructions are done by first reading the entire register, operating on the selected bit and writing the result back (read-modify-write). The user should keep this in mind when operating on special function registers, such as ports.

GOTO — Unconditional Branch

Syntax: [*label*] GOTO k

Operands: $0 \le k \le 2047$

Operation: k → PC<10:0>
PCLATH<4:3> → PC<12:11>

Status Affected: None

Encoding:

10	1kkk	kkkk	kkkk

Description: `GOTO` is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. `GOTO` is a two cycle instruction.

Words: 1

Cycles: 2

Example

```
GOTO THERE
```

After Instruction
PC = Address `THERE`

INCF — Increment f

Syntax: [*label*] INCF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) + 1 → (dest)

Status Affected: Z

Encoding:

00	1010	dfff	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example

```
INCF    CNT, 1
```

Before Instruction
CNT = 0xFF
Z = 0
After Instruction
CNT = 0x00
Z = 1

INCFSZ — Increment f, Skip if 0

Syntax: [*label*] INCFSZ f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) + 1 → (dest), skip if result = 0

Status Affected: None

Encoding:

00	1111	dfff	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.
If the result is 0, the next instruction, which is already fetched, is discarded. A `NOP` is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example

```
HERE      INCFSZ    CNT,  1
          GOTO      LOOP
CONTINUE  •
          •
          •
```

Before Instruction
PC = address `HERE`
After Instruction
CNT = CNT + 1
if CNT= 0,
PC = address `CONTINUE`
if CNT≠ 0,
PC = address `HERE +1`

IORLW — Inclusive OR Literal with W

Syntax: [*label*] IORLW k

Operands: $0 \le k \le 255$

Operation: (W) .OR. k → (W)

Status Affected: Z

Encoding:

11	1000	kkkk	kkkk

Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example

```
IORLW   0x35
```

Before Instruction
W = 0x9A
After Instruction
W = 0xBF
Z = 1

and test the sample code. In addition, PICDEM-17 supports down-loading of programs to and executing out of external FLASH memory on board. The PICDEM-17 is also usable with the MPLAB-ICE or PICMASTER emulator, and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

11.17 SEEVAL Evaluation and Programming System

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

11.18 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

12.1 DC Characteristics: PIC12C671/672 (Commercial, Industrial, Extended) PIC12CE673/674 (Commercial, Industrial, Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended)					
Parm No.	**Characteristic**	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D001	**Supply Voltage**	VDD	3.0		5.5	V	
D002	**RAM Data Retention Voltage(2)**	VDR		1.5*		V	Device in SLEEP mode
D003	**VDD Start Voltage to ensure Power-on Reset**	VPOR		VSS		V	See section on Power-on Reset for details
D004	**VDD Rise Rate to ensure Power-on Reset**	SVDD	0.05*			V/ms	See section on Power-on Reset for details
D010	**Supply Current(3)**	IDD	—	1.2	2.5	mA	FOSC = 4MHz, VDD = 3.0V XT and EXTRC mode (Note 4)
D010C			—	1.2	2.5	mA	FOSC = 4MHz, VDD = 3.0V INTRC mode (Note 6)
			—	2.2	8	mA	FOSC = 10MHz, VDD = 5.5V HS mode
D010A			—	19	29	µA	FOSC = 32kHz, VDD = 3.0V, WDT disabled LP mode, Commercial Temperature
			—	19	37	µA	FOSC = 32kHz, VDD = 3.0V, WDT disabled LP mode, Industrial Temperature
			—	32	60	µA	FOSC = 32kHz, VDD = 3.0V, WDT disabled LP mode, Extended Temperature
D020 D021 D021B	**Power-down Current(5)**	IPD	— — — — — —	0.25 0.25 2 0.5 0.8 3	6 7 14 8 9 16	µA µA µA µA µA µA	VDD = 3.0V, Commercial, WDT disabled VDD = 3.0V, Industrial, WDT disabled VDD = 3.0V, Extended, WDT disabled VDD = 5.5V, Commercial, WDT disabled VDD = 5.5V, Industrial, WDT disabled VDD = 5.5V, Extended, WDT disabled
D022	**Watchdog Timer Current**	ΔIWDT	— — —	2.2 2.2 4	5 6 11	µA µA µA	VDD = 3.0V, Commercial VDD = 3.0V, Industrial VDD = 3.0V, Extended
D028	**Supply Current(3)** During read/write to EEPROM peripheral	ΔIEE	—	0.1	0.2	mA	FOSC = 4MHz, VDD = 5.5V, SCL = 400kHz For PIC12CE673/674 only

* These parameters are characterized but not tested.

Note 1: Data in Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD,
$\overline{\text{MCLR}}$ = VDD; WDT disabled.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: For EXTRC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula:
Ir = VDD/2REXT (mA) with REXT in kOhm.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

6: INTRC calibration value is for 4MHz nominal at 5V, 25°C.

DC CHARACTERISTICS							Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended)
Parm No.	**Characteristic**	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	LP Oscillator Operating Frequency	FOSC	0		200	kHz	All temperatures
	INTRC/EXTRC Oscillator Operating Frequency		—		4(6)	MHz	All temperatures
	XT Oscillator Operating Frequency		0		4	MHz	All temperatures
	HS Oscillator Operating Frequency		0		10	MHz	All temperatures

* These parameters are characterized but not tested.

Note 1: Data in Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD,
$\overline{\text{MCLR}}$ = VDD; WDT disabled.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: For EXTRC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula:
Ir = VDD/2REXT (mA) with REXT in kOhm.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

6: INTRC calibration value is for 4MHz nominal at 5V, 25°C.

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise specified) Operating temperature 0°C $\leq T_A \leq$ +70°C (commercial) –40°C $\leq T_A \leq$ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 12.1 and Section 12.2.					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	Output High Voltage						
D090	I/O ports (Note 3)	V_{OH}	V_{DD} - 0.7	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 4.5V, –40°C to +85°C
D090A			V_{DD} - 0.7	—	—	V	I_{OH} = -2.5 mA, V_{DD} = 4.5V, –40°C to +125°C
D092	OSC2/CLKOUT		V_{DD} - 0.7	—	—	V	I_{OH} = TBD, V_{DD} = 4.5V, –40°C to +85°C
D092A			V_{DD} - 0.7	—	—	V	I_{OH} = TBD, V_{DD} = 4.5V, –40°C to +125°C
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	C_{OSC2}	—	—	15	pF	In XT and LP modes when external clock is used to drive OSC1.
D101	All I/O pins	C_{IO}	—	—	50	pF	

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C67X be driven with external clock in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: Does not include GP3. For GP3 see parameters D061 and D061A.

5: This spec. applies to GP3/$\overline{\text{MCLR}}$ configured as external $\overline{\text{MCLR}}$ and GP3/$\overline{\text{MCLR}}$ configured as input with internal pull-up enabled.

6: This spec. applies when GP3/$\overline{\text{MCLR}}$ is configured as an input with pull-up disabled. The leakage current of the $\overline{\text{MCLR}}$ circuit is higher than the standard I/O logic.

TABLE 12-2: CALIBRATED INTERNAL RC FREQUENCIES -PIC12C671, PIC12C672, PIC12CE673, PIC12CE674, PIC12LC671, PIC12LC672, PIC12LCE673, PIC12LCE674

AC Characteristics — **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature $0°C \le T_A \le +70°C$ (commercial),
$-40°C \le T_A \le +85°C$ (industrial),
$-40°C \le T_A \le +125°C$ (extended)
Operating Voltage V_{DD} range is described in Section 10.1

Parameter No.	Sym	Characteristic	Min*	Typ(1)	Max*	Units	Conditions
		Internal Calibrated RC Frequency	3.65	4.00	4.28	MHz	V_{DD} = 5.0V
		Internal Calibrated RC Frequency	3.55	4.00	4.31	MHz	V_{DD} = 2.5V

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 12-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, AND POWER-UP TIMER TIMING

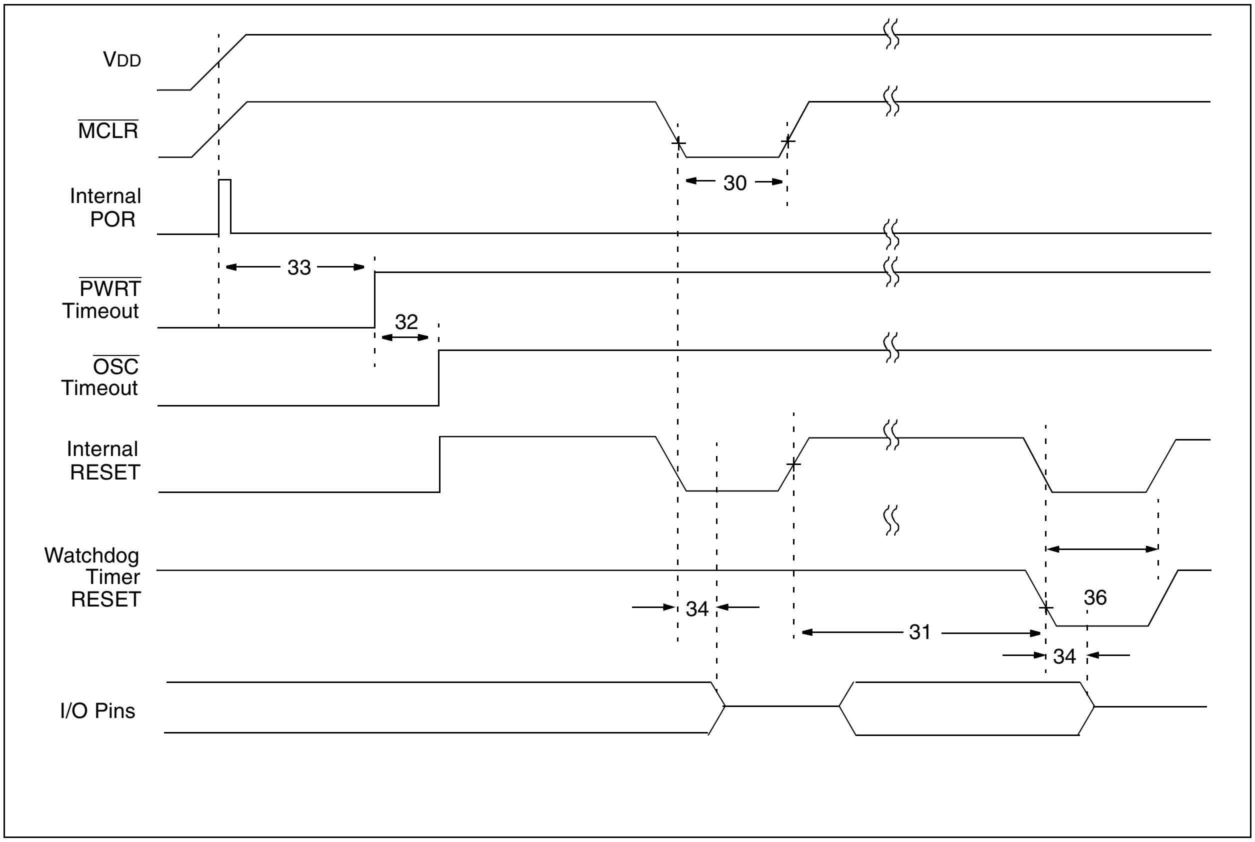


TABLE 12-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER

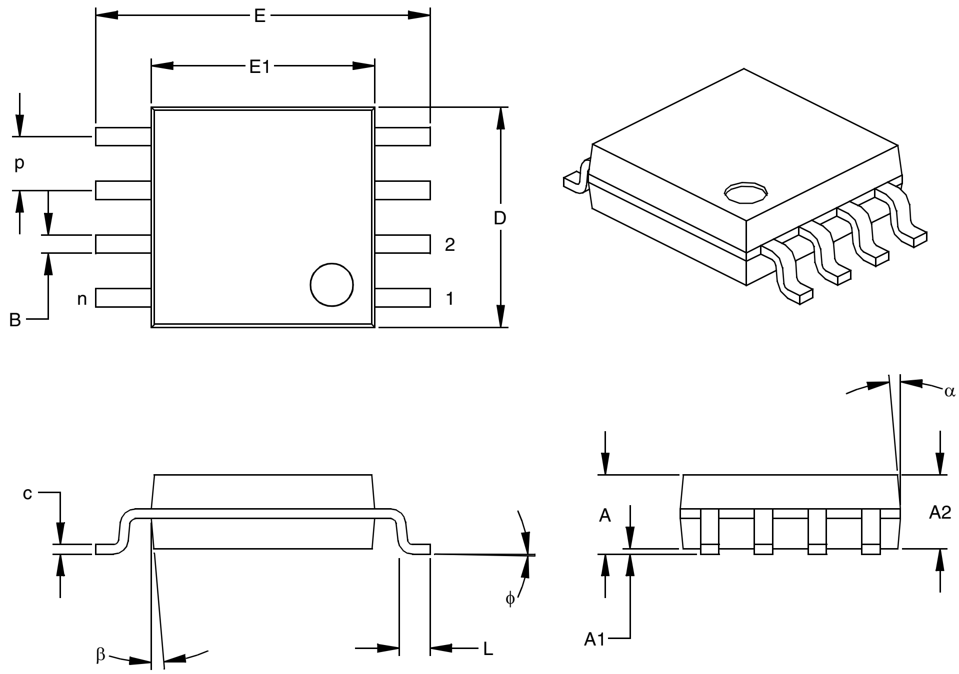
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	µs	VDD = 5V, –40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, –40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power up Timer Period	28	72	132	ms	VDD = 5V, –40°C to +125°C
34	TIOZ	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	—	2.1	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

8-Lead Plastic Small Outline (SM) – Medium, 208 mil (SOIC)

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.070	.075	.080	1.78	1.97	2.03
Molded Package Thickness	A2	.069	.074	.078	1.75	1.88	1.98
Standoff	A1	.002	.005	.010	0.05	0.13	0.25
Overall Width	E	.300	.313	.325	7.62	7.95	8.26
Molded Package Width	E1	.201	.208	.212	5.11	5.28	5.38
Overall Length	D	.202	.205	.210	5.13	5.21	5.33
Foot Length	L	.020	.025	.030	0.51	0.64	0.76
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-056

Note the following details of the code protection feature on Microchip devices:

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