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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOIJ
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic12c672t-04i-sm">https://www.e-xfl.com/product-detail/microchip-technology/pic12c672t-04i-sm</a>

# PIC12C67X

## 3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, and the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

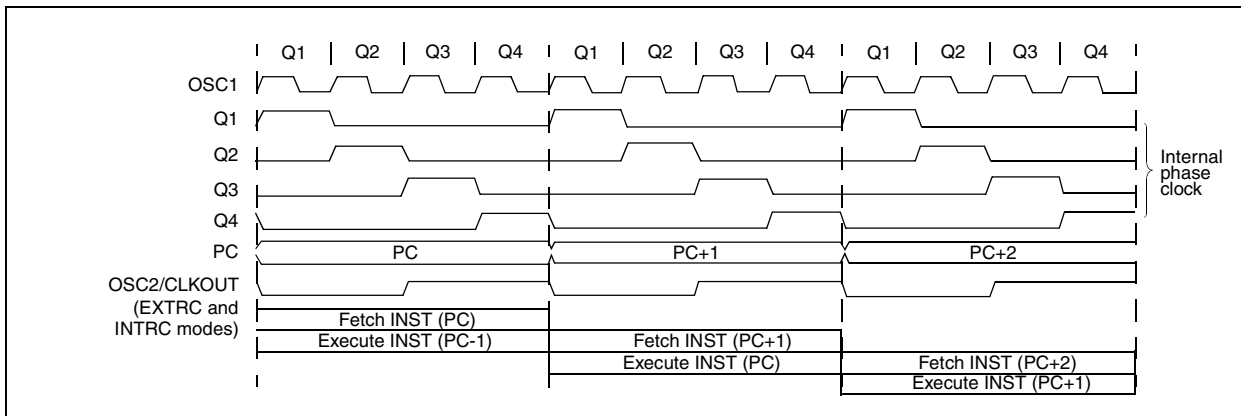
## 3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (i.e., GOTO), then two cycles are required to complete the instruction (Example 3-1).

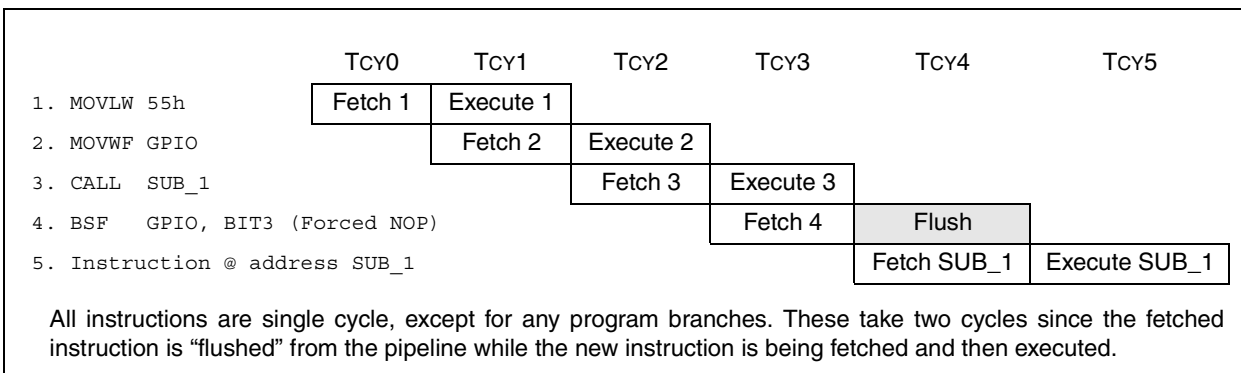
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register" (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

**FIGURE 3-2: CLOCK/INSTRUCTION CYCLE**



**EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW**



## 5.0 I/O PORT

As with any other register, the I/O register can be written and read under program control. However, read instructions (i.e., `MOVF GPIO, W`) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance), since the I/O control registers are all set.

### 5.1 GPIO

GPIO is an 8-bit I/O register. Only the low order 6 bits are used (GP<5:0>). Bits 6 and 7 (SDA and SCL, respectively) are used by the EEPROM peripheral on the PIC12CE673/674. Refer to Section 6.0 and Appendix B for use of SDA and SCL. Please note that GP3 is an input only pin. The configuration word can set several I/O's to alternate functions. When acting as alternate functions, the pins will read as '0' during port read. Pins GP0, GP1 and GP3 can be configured with weak pull-ups and also with interrupt-on-change. The interrupt on change and weak pull-up functions are not pin selectable. If pin 4, (GP3), is configured as MCLR, a weak pull-up is always on. Interrupt-on-change for this pin is not set and GP3 will read as '0'. Interrupt-on-change is enabled by setting bit GPIE, `INTCON<3>`. Note that external oscillator use overrides the GPIO functions on GP4 and GP5.

### 5.2 TRIS Register

This register controls the data direction for GPIO. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer. The exceptions are GP3, which is input only and its TRIS bit will always read as '1', while GP6 and GP7 TRIS bits will read as '0'.

**Note:** A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

Upon reset, the TRIS Register is all '1's, making all pins inputs.

TRIS for pins GP4 and GP5 is forced to a '1' where appropriate. Writes to TRIS <5:4> will have an effect in EXTRC and INTRC oscillator modes only. When GP4 is configured as CLKOUT, changes to TRIS<4> will have no effect.

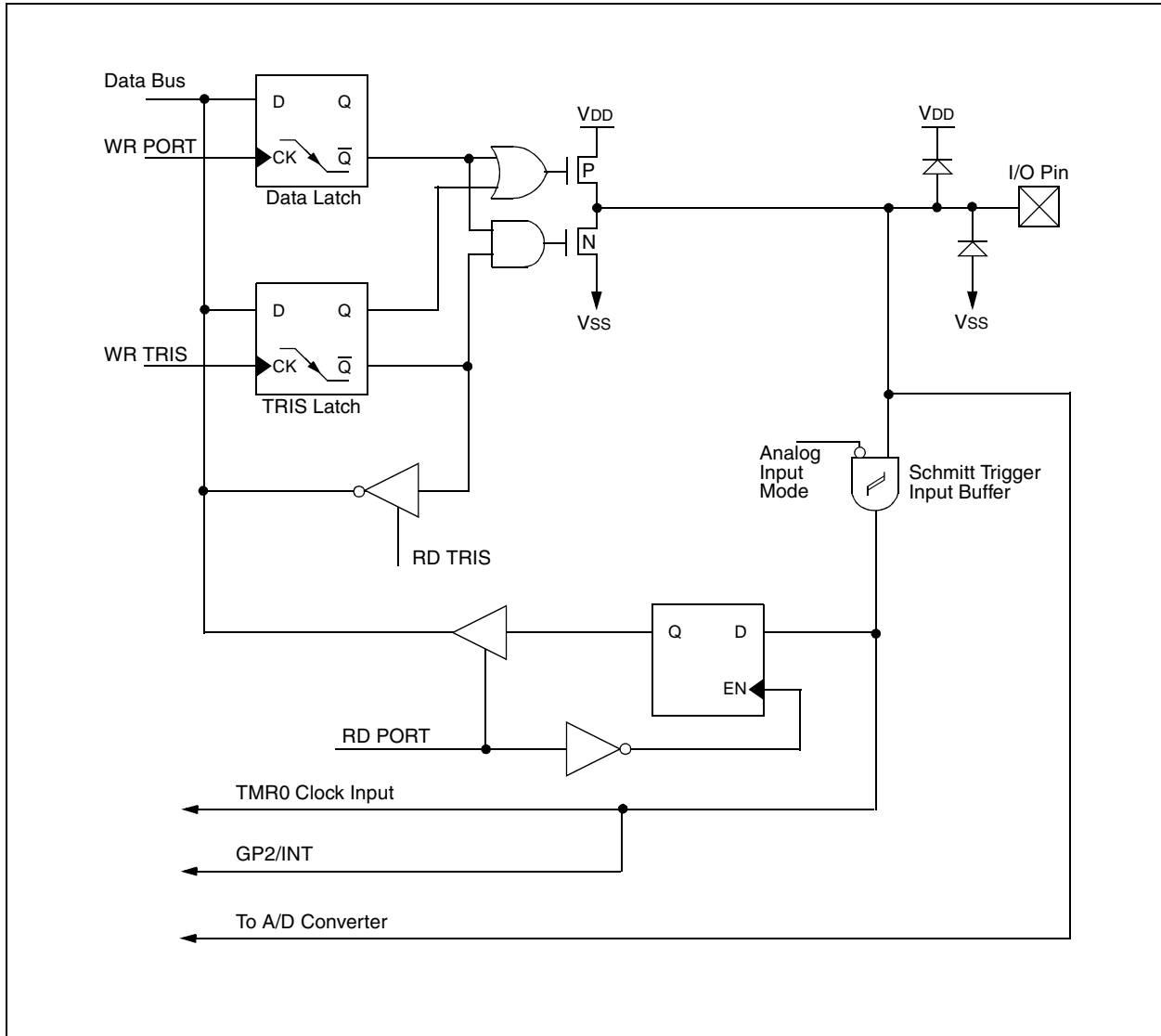
### 5.3 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 5-1 through Figure 5-5. All port pins, except GP3, which is input only, may be used for both input and output operations. For input operations, these ports are non-latching. Any input must be present until read by an input instruction (i.e., `MOVF GPIO, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit in TRIS must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin (except GP3) can be programmed individually as input or output.

Port pins GP6 (SDA) and GP7 (SCL) are used for the serial EEPROM interface on the PIC12CE673/674. These port pins are not available externally on the package. Users should avoid writing to pins GP6 (SDA) and GP7 (SCL) when not communicating with the serial EEPROM memory. Please see Section 6.0, EEPROM Peripheral Operation, for information on serial EEPROM communication.

**Note:** On a Power-on Reset, GP0, GP1, GP2 and GP4 are configured as analog inputs and read as '0'.

**FIGURE 5-2: BLOCK DIAGRAM OF GP2/T0CKI/AN2/INT PIN**





## 7.2 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

### 7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is used as the clock source. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

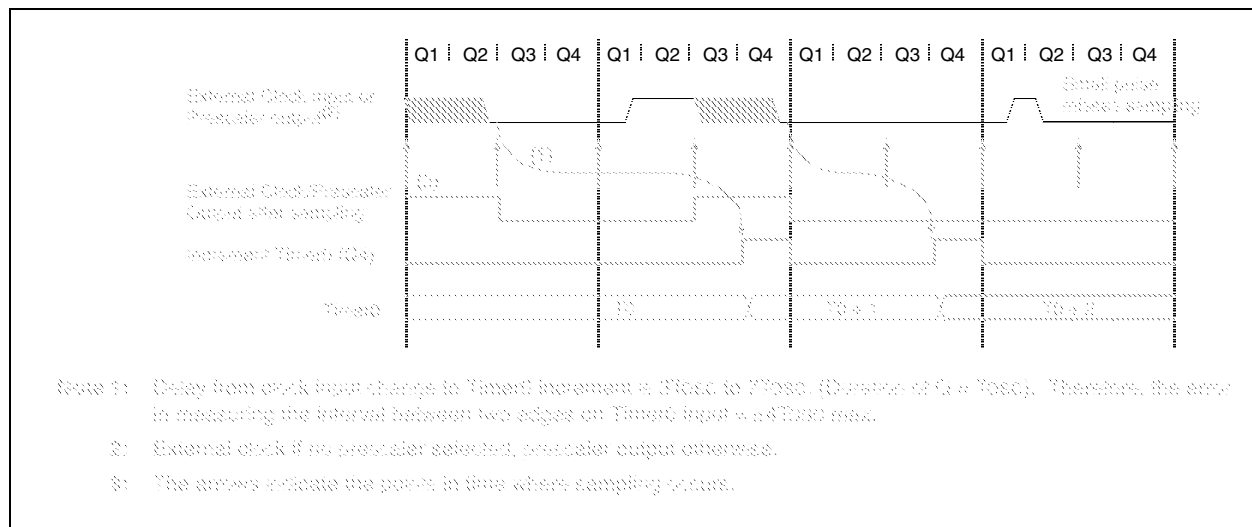
When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type pres-

caler, so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

### 7.2.2 TMR0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.

**FIGURE 7-5: TIMER0 TIMING WITH EXTERNAL CLOCK**



## 7.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, (i.e., it can be changed “on-the-fly” during program execution).

**Note:** To avoid an unintended device RESET, the following instruction sequence (shown in Example 7-1) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

### EXAMPLE 7-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF    STATUS, RP0    ;Bank 0
CLRF   TMR0           ;Clear TMR0 & Prescaler
BSF    STATUS, RP0    ;Bank 1
CLRWDT           ;Clears WDT
MOVLW  b'xxxx1xxx'    ;Select new prescale
MOVWF  OPTION_REG     ;value & WDT
BCF    STATUS, RP0    ;Bank 0
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 7-2.

### EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT           ;Clear WDT and
                  ;prescaler
BSF     STATUS, RP0 ;Bank 1
MOVLW   b'xxx0xxx' ;Select TMR0, new
                  ;prescale value and
MOVWF   OPTION_REG ;clock source
BCF     STATUS, RP0 ;Bank 0
```

**TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER0**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other Resets
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	TOIE	INTE	GPIE	TOIF	INTF	GPIF	0000 000x	0000 000u
81h	OPTION	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRIS	—	—	TRIS5	TRIS4	TRIS3	TRIS2	TRIS1	TRIS0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

# PIC12C67X

## REGISTER 8-2: ADCON1 REGISTER (ADDRESS 9Fh)

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCFG2	PCFG1	PCFG0
bit7					bit0		

R = Readable bit  
 W = Writable bit  
 U = Unimplemented bit,  
 read as '0'  
 - n = Value at POR reset

bit 7-2: **Unimplemented:** Read as '0'

bit 1-0: **PCFG<2:0>:** A/D Port Configuration Control bits

PCFG<2:0>	GP4	GP2	GP1	GP0	VREF
000 <sup>(1)</sup>	A	A	A	A	VDD
001	A	A	VREF	A	GP1
010	D	A	A	A	VDD
011	D	A	VREF	A	GP1
100	D	D	A	A	VDD
101	D	D	VREF	A	GP1
110	D	D	D	A	VDD
111	D	D	D	D	VDD

A = Analog input

D = Digital I/O

**Note 1:** Value on reset.

**2:** Any instruction that reads a pin configured as an analog input will read a '0'.



## 9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC12C67X family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- Oscillator selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming

The PIC12C67X has a Watchdog Timer, which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep

the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer Wake-up, or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The INTRC/EXTRC oscillator option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options.

### 9.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h-3FFFh), which can be accessed only during programming.

### REGISTER 9-1: CONFIGURATION WORD

CP1	CP0	CP1	CP0	CP1	CP0	MCLR	CP1	CP0	PWRT	WDTE	FOSC2	FOSC1	FOSC0	Register: CONFIG Address: 2007h
bit13													bit0	
bit 13-8, <b>CP&lt;1:0&gt;</b> : Code Protection bit pairs <sup>(1)</sup>														
6-5: 11 = Code protection off														
10 = Locations 400h through 7FEh code protected (do not use for PIC12C671 and PIC12CE673)														
01 = Locations 200h through 7FEh code protected														
00 = All memory is code protected														
bit 7: <b>MCLR</b> : Master Clear Reset Enable bit														
1 = Master Clear Enabled														
0 = Master Clear Disabled														
bit 4: <b>PWRT</b> : Power-up Timer Enable bit														
1 = PWRT disabled														
0 = PWRT enabled														
bit 3: <b>WDTE</b> : Watchdog Timer Enable bit														
1 = WDT enabled														
0 = WDT disabled														
bit 2-0: <b>FOSC&lt;2:0&gt;</b> : Oscillator Selection bits														
111 = EXTRC, Clockout on OSC2														
110 = EXTRC, OSC2 is I/O														
101 = INTRC, Clockout on OSC2														
100 = INTRC, OSC2 is I/O														
011 = Invalid Selection														
010 = HS Oscillator														
001 = XT Oscillator														
000 = LP Oscillator														
<b>Note 1:</b> All of the CP<1:0> pairs have to be given the same value to enable the code protection scheme listed.														

# PIC12C67X

## 9.2 Oscillator Configurations

### 9.2.1 OSCILLATOR TYPES

The PIC12C67X can be operated in seven different oscillator modes. The user can program three configuration bits (FOSC<2:0>) to select one of these seven modes:

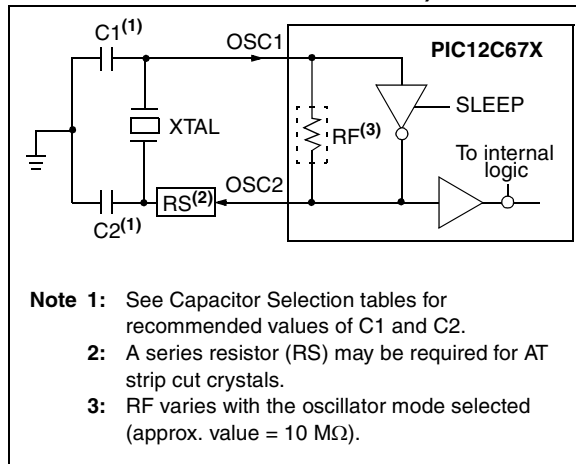
- LP: Low Power Crystal
- HS: High Speed Crystal/Resonator
- XT: Crystal/Resonator
- INTRC\*: Internal 4 MHz Oscillator
- EXTRC\*: External Resistor/Capacitor

\*Can be configured to support CLKOUT

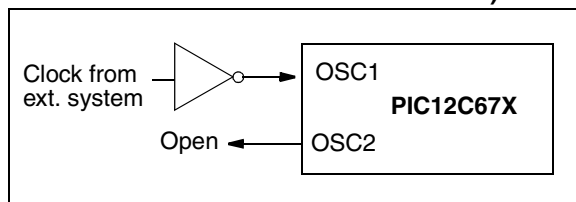
### 9.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, HS or LP modes, a crystal or ceramic resonator is connected to the GP5/OSC1/CLKIN and GP4/OSC2 pins to establish oscillation (Figure 9-1). The PIC12C67X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, HS or LP modes, the device can have an external clock source drive the GP5/OSC1/CLKIN pin (Figure 9-2).

**FIGURE 9-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (XT, HS OR LP OSC CONFIGURATION)**



**FIGURE 9-2: EXTERNAL CLOCK INPUT OPERATION (XT, HS OR LP OSC CONFIGURATION)**



**TABLE 9-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC12C67X**

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	22-100 pF	22-100 pF
	2.0 MHz	15-68 pF	15-68 pF
	4.0 MHz	15-68 pF	15-68 pF
HS	4.0 MHz	15-68 pF	15-68 pF
	8.0 MHz	10-68 pF	10-68 pF
	10.0 MHz	10-22 pF	10-22 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

**TABLE 9-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC12C67X**

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz <sup>(1)</sup>	15 pF	15 pF
	100 kHz	15-30 pF	30-47 pF
	200 kHz	15-30 pF	15-30 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15-30 pF	15-30 pF
	4 MHz	15-47 pF	15-47 pF
HS	4 MHz	15-30 pF	15-30 pF
	8 MHz	15-30 pF	15-30 pF
	10 MHz	15-30 pF	15-30 pF

**Note 1:** For VDD > 4.5V, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

# PIC12C67X

## 9.5 Interrupts

There are four sources of interrupt:

Interrupt Sources
TMR0 Overflow Interrupt
External Interrupt GP2/INT pin
GPIO Port Change Interrupts (pins GP0, GP1, GP3)
A/D Interrupt

The Interrupt Control Register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

**Note:** Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

A global interrupt enable bit, GIE (INTCON<7>), enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit. The GIE bit is cleared on reset.

The "return-from-interrupt" instruction, `RETFIE`, exits the interrupt routine, as well as sets the GIE bit, which re-enables interrupts.

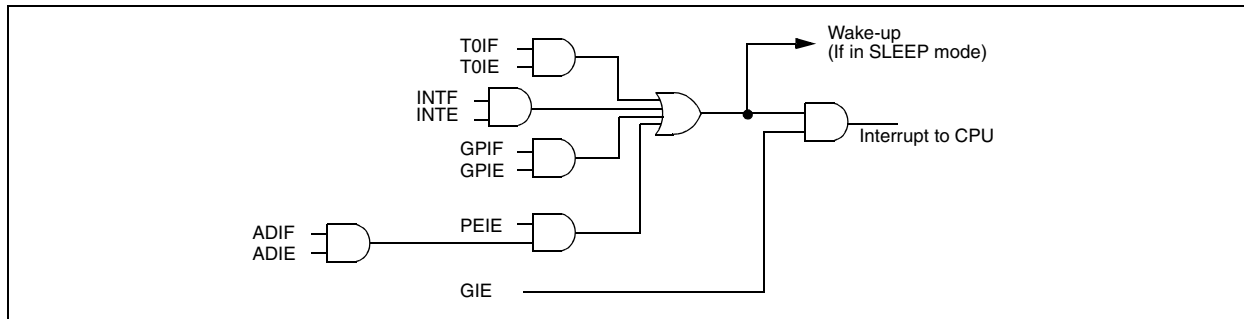
The GP2/INT, GPIO port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flag ADIF, is contained in the Special Function Register PIR1. The corresponding interrupt enable bit is contained in Special Function Register PIE1, and the peripheral interrupt enable bit is contained in Special Function Register INTCON.

When an interrupt is responded to, the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the interrupt service routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid repeated interrupts.

For external interrupt events, such as GPIO change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends on when the interrupt event occurs (Figure 9-14). The latency is the same for one or two cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

**FIGURE 9-13: INTERRUPT LOGIC**



BCF		Bit Clear f							
Syntax:	[ <i>label</i> ] BCF f,b								
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$								
Operation:	$0 \rightarrow (f<b>)$								
Status Affected:	None								
Encoding:	<table border="1"><tr><td>01</td><td>00bb</td><td>bfff</td><td>ffff</td></tr></table>					01	00bb	bfff	ffff
01	00bb	bfff	ffff						
Description:	Bit 'b' in register 'f' is cleared.								
Words:	1								
Cycles:	1								
Example	BCF FLAG_REG, 7								
	Before Instruction								
	FLAG_REG = 0xC7								
	After Instruction								
	FLAG_REG = 0x47								

BTFSC		Bit Test, Skip if Clear							
Syntax:	[ <i>label</i> ] BTFSC f,b								
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$								
Operation:	skip if (f<b>) = 0								
Status Affected:	None								
Encoding:	<table border="1"><tr><td>01</td><td>10bb</td><td>bfff</td><td>ffff</td></tr></table>					01	10bb	bfff	ffff
01	10bb	bfff	ffff						
Description:	<p>If bit 'b' in register 'f' is '0', then the next instruction is skipped.</p> <p>If bit 'b' is '0', then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a 2 cycle instruction.</p>								
Words:	1								
Cycles:	1(2)								
Example	HERE      BTFSC      FLAG,1								

Before Instruction  
PC = address HERE

After Instruction  
if  $FLAG<1> = 0$ ,  
PC = address TRUE  
if  $FLAG<1> \geq 1$ ,  
PC = address FALSE

BSF		Bit Set f							
Syntax:	[ <i>label</i> ] BSF f,b								
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$								
Operation:	$1 \rightarrow (f<b>)$								
Status Affected:	None								
Encoding:	<table border="1"><tr><td>01</td><td>01bb</td><td>bfff</td><td>ffff</td></tr></table>					01	01bb	bfff	ffff
01	01bb	bfff	ffff						
Description:	Bit 'b' in register 'f' is set.								
Words:	1								
Cycles:	1								
Example	<pre>BSF    FLAG_REG, 7</pre> <p>Before Instruction FLAG_REG = 0x0A</p> <p>After Instruction FLAG_REG = 0x8A</p>								

## CLRWDT Clear Watchdog Timer

**Syntax:** [ *label* ] CLRWDT

**Operands:** None

**Operation:** 00h → WDT  
0 → WDT prescaler,  
1 →  $\overline{TO}$   
1 →  $\overline{PD}$

**Status Affected:**  $\overline{TO}$ ,  $\overline{PD}$

**Encoding:**

00	0000	0110	0100
----	------	------	------

**Description:** CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits  $\overline{TO}$  and  $\overline{PD}$  are set.

**Words:** 1

**Cycles:** 1

**Example**

```
CLRWDT

Before Instruction
    WDT counter = ?
After Instruction
    WDT counter = 0x00
    WDT prescaler = 0
     $\overline{TO}$  = 1
     $\overline{PD}$  = 1
```

## COMF Complement f

**Syntax:** [ *label* ] COMF f,d

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:** ( $\bar{f}$ ) → (dest)

**Status Affected:** Z

**Encoding:**

00	1001	dfff	ffff
----	------	------	------

**Description:** The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.

**Words:** 1

**Cycles:** 1

**Example**

```
COMF    REG1, 0

Before Instruction
    REG1 = 0x13
After Instruction
    REG1 = 0x13
    W    = 0xEC
```

## DECF Decrement f

**Syntax:** [ *label* ] DECF f,d

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:** (f) - 1 → (dest)

**Status Affected:** Z

**Encoding:**

00	0011	dfff	ffff
----	------	------	------

**Description:** Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

**Words:** 1

**Cycles:** 1

**Example**

```
DECF    CNT, 1

Before Instruction
    CNT = 0x01
    Z   = 0
After Instruction
    CNT = 0x00
    Z   = 1
```

## DECFSZ Decrement f, Skip if 0

**Syntax:** [ *label* ] DECFSZ f,d

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:** (f) - 1 → (dest); skip if result = 0

**Status Affected:** None

**Encoding:**

00	1011	dfff	ffff
----	------	------	------

**Description:** The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

**Words:** 1

**Cycles:** 1(2)

**Example**

```
HERE    DECFSZ    CNT, 1
        GOTO     LOOP
CONTINUE •
        •
        •

Before Instruction
    PC = address HERE
After Instruction
    CNT = CNT - 1
    if CNT = 0,
    PC = address CONTINUE
    if CNT ≠ 0,
    PC = address HERE+1
```

# PIC12C67X

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NOTES:

## 12.0 ELECTRICAL SPECIFICATIONS FOR PIC12C67X

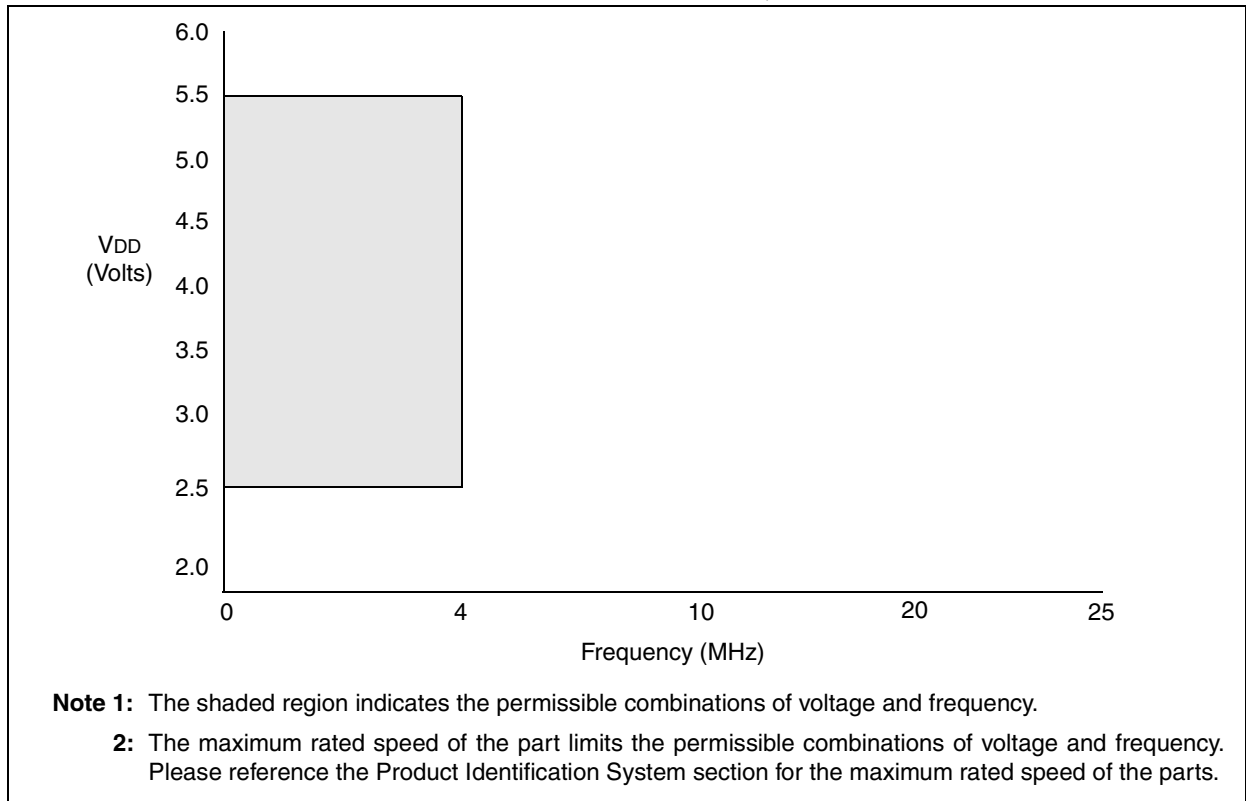
### Absolute Maximum Ratings †

Ambient temperature under bias .....	–40° to +125°C
Storage temperature .....	–65°C to +150°C
Voltage on any pin with respect to VSS (except VDD and $\overline{\text{MCLR}}$ ).....	–0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS .....	0 to +7.0V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS (Note 2).....	0 to +14V
Total power dissipation (Note 1) .....	700 mW
Maximum current out of VSS pin .....	200 mA
Maximum current into VDD pin .....	150 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > VDD).....	± 20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > VDD) .....	± 20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin .....	25 mA
Maximum current sunk by GPIO pins combined .....	100 mA
Maximum current sourced by GPIO pins combined.....	100 mA

**Note 1:** Power dissipation is calculated as follows:  $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$ .

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**FIGURE 12-3: PIC12LC67X VOLTAGE-FREQUENCY GRAPH,  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$**





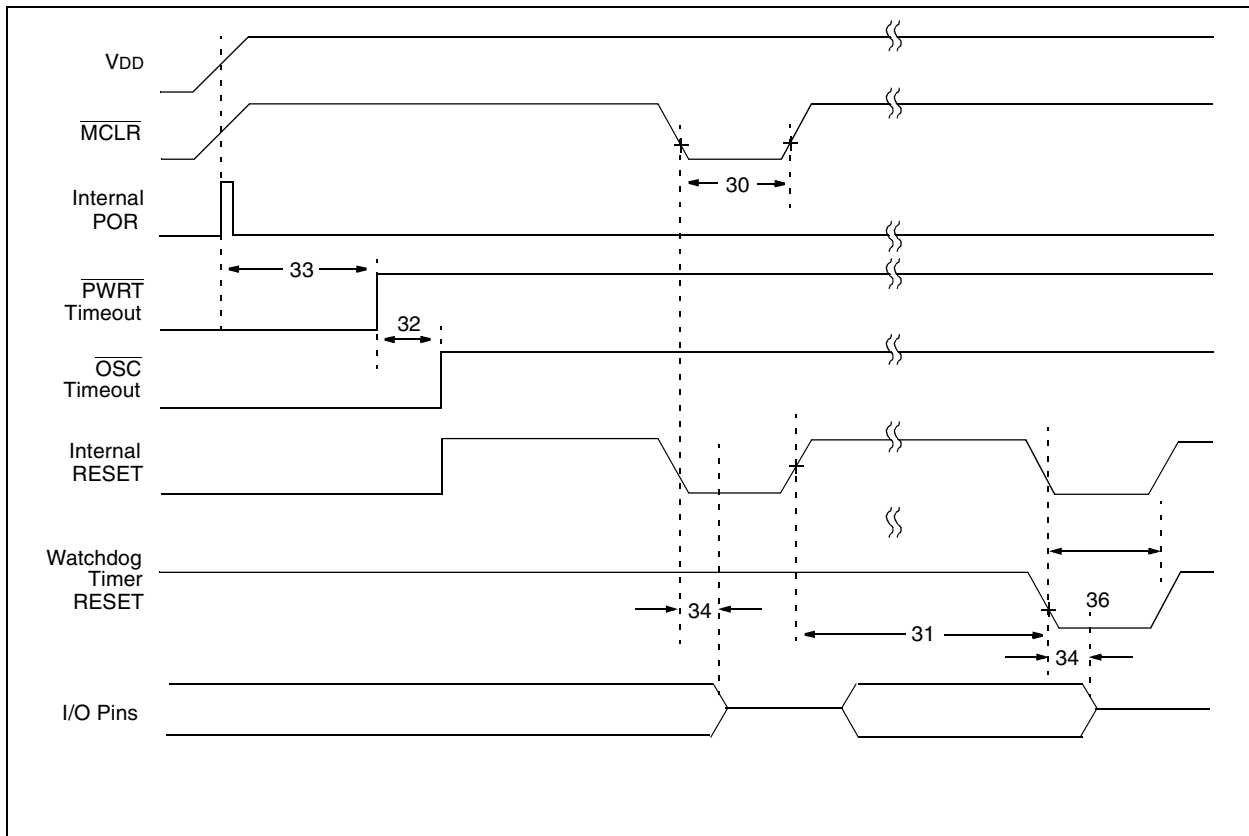
# PIC12C67X

<b>Standard Operating Conditions (unless otherwise specified)</b> Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) Operating voltage $V_{DD}$ range as described in DC spec Section 12.1 and Section 12.2.							
<b>DC CHARACTERISTICS</b>							
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D090	<b>Output High Voltage</b> I/O ports (Note 3)	VOH	$V_{DD} - 0.7$	—	—	V	IOH = -3.0 mA, $V_{DD} = 4.5\text{V}$ , -40°C to +85°C
D090A			$V_{DD} - 0.7$	—	—	V	
D092			$V_{DD} - 0.7$	—	—	V	
D092A			$V_{DD} - 0.7$	—	—	V	
	<b>Capacitive Loading Specs on Output Pins</b>						
D100	OSC2 pin	COSC2	—	—	15	pF	In XT and LP modes when external clock is used to drive OSC1.
D101	All I/O pins	CIO	—	—	50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C67X be driven with external clock in RC mode.
- 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as coming out of the pin.
- 4:** Does not include GP3. For GP3 see parameters D061 and D061A.
- 5:** This spec. applies to GP3/MCLR configured as external MCLR and GP3/MCLR configured as input with internal pull-up enabled.
- 6:** This spec. applies when GP3/MCLR is configured as an input with pull-up disabled. The leakage current of the MCLR circuit is higher than the standard I/O logic.

**FIGURE 12-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, AND POWER-UP TIMER TIMING**



**TABLE 12-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	2	—	—	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024Tosc	—	—	Tosc = OSC1 period
33*	Tpwrt	Power up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	TIOZ	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.1	μs	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**TABLE 12-9: EEPROM MEMORY BUS TIMING REQUIREMENTS - PIC12CE673/674 ONLY.**

AC Characteristics		Standard Operating Conditions (unless otherwise specified)			
		Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ , $V_{CC} = 3.0\text{V}$ to $5.5\text{V}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ , $V_{CC} = 3.0\text{V}$ to $5.5\text{V}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ , $V_{CC} = 4.5\text{V}$ to $5.5\text{V}$ (extended) Operating Voltage $V_{DD}$ range is described in Section 12.1			
Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK	— — —	100 100 400	kHz	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ (E Temp range) $3.0\text{V} \leq V_{CC} \leq 4.5\text{V}$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
Clock high time	T <sub>HIGH</sub>	4000 4000 600	— — —	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ (E Temp range) $3.0\text{V} \leq V_{CC} \leq 4.5\text{V}$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
Clock low time	T <sub>LOW</sub>	4700 4700 1300	— — —	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ (E Temp range) $3.0\text{V} \leq V_{CC} \leq 4.5\text{V}$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
SDA and SCL rise time (Note 1)	T <sub>R</sub>	— — —	1000 1000 300	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ (E Temp range) $3.0\text{V} \leq V_{CC} \leq 4.5\text{V}$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
SDA and SCL fall time	T <sub>F</sub>	—	300	ns	(Note 1)
START condition hold time	T <sub>HD:STA</sub>	4000 4000 600	— — —	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ (E Temp range) $3.0\text{V} \leq V_{CC} \leq 4.5\text{V}$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
START condition setup time	T <sub>SU:STA</sub>	4700 4700 600	— — —	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ (E Temp range) $3.0\text{V} \leq V_{CC} \leq 4.5\text{V}$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
Data input hold time	T <sub>HD:DAT</sub>	0	—	ns	(Note 2)
Data input setup time	T <sub>SU:DAT</sub>	250 250 100	— — —	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ (E Temp range) $3.0\text{V} \leq V_{CC} \leq 4.5\text{V}$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
STOP condition setup time	T <sub>SU:STO</sub>	4000 4000 600	— — —	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ (E Temp range) $3.0\text{V} \leq V_{CC} \leq 4.5\text{V}$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
Output valid from clock (Note 2)	T <sub>AA</sub>	— — —	3500 3500 900	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ (E Temp range) $3.0\text{V} \leq V_{CC} \leq 4.5\text{V}$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
Bus free time: Time the bus must be free before a new transmis- sion can start	T <sub>BUF</sub>	4700 4700 1300	— — —	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ (E Temp range) $3.0\text{V} \leq V_{CC} \leq 4.5\text{V}$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
Output fall time from V <sub>IH</sub> minimum to V <sub>IL</sub> maximum	T <sub>OF</sub>	20+0.1 CB	250	ns	(Note 1), $C_B \leq 100\text{ pF}$
Input filter spike suppression (SDA and SCL pins)	T <sub>SP</sub>	—	50	ns	(Notes 1, 3)
Write cycle time	T <sub>WC</sub>	—	4	ms	
Endurance		1M	—	cycles	25°C, $V_{CC} = 5.0\text{V}$ , Block Mode (Note 4)

**Note 1:** Not 100% tested.  $C_B$  = total capacitance of one bus line in pF.

**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL and avoid unintended generation of START or STOP conditions.

**3:** The combined T<sub>SP</sub> and V<sub>HYS</sub> specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a T<sub>I</sub> specification for standard operation.

**4:** This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's website.

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NOTES:

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