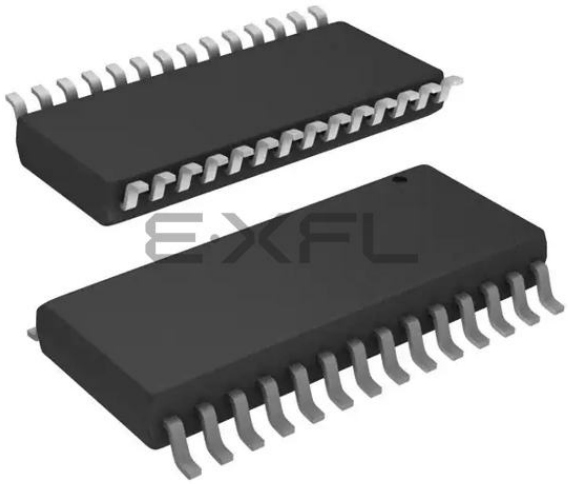

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1513-e-so

PIC16(L)F1512/3

28-Pin Flash Microcontrollers with XLP Technology

High-Performance RISC CPU:

- C Compiler Optimized Architecture
- Only 49 Instructions
- Up to 7 Kbytes Linear Program Memory Addressing
- Up to 256 Bytes Linear Data Memory Addressing
- Operating Speed:
  - DC – 20 MHz clock input @ 2.5V
  - DC – 16 MHz clock input @ 1.8V
  - DC – 200 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

Flexible Oscillator Structure:

- 16 MHz Internal Oscillator Block:
  - Factory calibrated to ± 1%, typical
  - Software selectable frequency range from 16 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - Four crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 20 MHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops
- Two-Speed Oscillator Start-up
- Oscillator Start-up Timer (OST)

Analog Features:

- Analog-to-Digital Converter (ADC):
  - 10-bit resolution
  - Up to 17 channels
  - Special Event Triggers
  - Conversion available during Sleep
  - Hardware Capacitive Voltage Divider (CVD)
  - Double sample conversions
  - Two result registers
  - Inverted acquisition
  - 7-bit pre-charge timer
  - 7-bit acquisition timer
  - Two guard ring output drives
  - Adjustable sample and hold capacitor array
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
- Integrated Temperature Indicator

Extreme Low-Power Management PIC16LF1512/3 with nanoWatt XLP:

- Sleep mode: 20 nA @ 1.8V, typical
- Watchdog Timer: 300 nA @ 1.8V, typical
- Secondary Oscillator: 600 nA @ 32 kHz, 1.8V, typical
- Operating Current: 30 μA/MHz @ 1.8V, typical

Special Microcontroller Features:

- Operating Voltage Range:
  - 2.3V-5.5V (PIC16F1512/3)
  - 1.8V-3.6V (PIC16LF1512/3)
- Self-Programmable under Software Control
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Programmable Low-Power Brown-out Reset (LPBOR)
- Extended Watchdog Timer (WDT)
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Programmable Code Protection
- Low-Power Sleep mode
- 128 Bytes High-Endurance Flash:
  - 100,000 write Flash endurance (minimum)

Peripheral Highlights:

- Up to 25 I/O Pins (1 input-only pin):
  - High current sink/source 25 mA/25 mA
  - Individually programmable weak pull-ups
  - Individually programmable interrupt-on-change (IOC) pins
- Timer0: 8-Bit Timer/Counter with 8-Bit Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Low-power 32 kHz secondary oscillator driver
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two Capture/Compare (CCP) modules:
- Master Synchronous Serial Port (MSSP) with SPI and I^2C^{TM} with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module:
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect
  - Auto-wake-up on start

PIC16(L)F151X/152X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	I/O's(2)	ADC		Timers (8/16-bit)	EUSART	MSSP (I^2C™/SPI)	CCP	Debug(1)	XLP
					10-bit (ch)	Advanced Control						
PIC16(L)F1512	(1)	2048	128	25	17	Y	2/1	1	1	2	I	Y
PIC16(L)F1513	(1)	4096	256	25	17	Y	2/1	1	1	2	I	Y
PIC16(L)F1516	(2)	8192	512	25	17	N	2/1	1	1	2	I	Y
PIC16(L)F1517	(2)	8192	512	36	28	N	2/1	1	1	2	I	Y
PIC16(L)F1518	(2)	16384	1024	25	17	N	2/1	1	1	2	I	Y
PIC16(L)F1519	(2)	16384	1024	36	28	N	2/1	1	1	2	I	Y
PIC16(L)F1526	(3)	8192	768	54	30	N	6/3	2	2	10	I	Y
PIC16(L)F1527	(3)	16384	1536	54	30	N	6/3	2	2	10	I	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, Requires Debug Header.

2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

1: Future Product PIC16(L)F1512/13 Data Sheet, 28-Pin Flash, 8-bit Microcontrollers.

2: DS41452 PIC16(L)F1516/7/8/9 Data Sheet, 28/40/44-Pin Flash, 8-bit MCUs.

3: DS41458 PIC16(L)F1526/27 Data Sheet, 64-Pin Flash, 8-bit MCUs.

FIGURE 1: 28-PIN SPDIP, SOIC, SSOP PACKAGE DIAGRAM FOR PIC16(L)F1512/3

28-Pin SPDIP, SOIC, SSOP

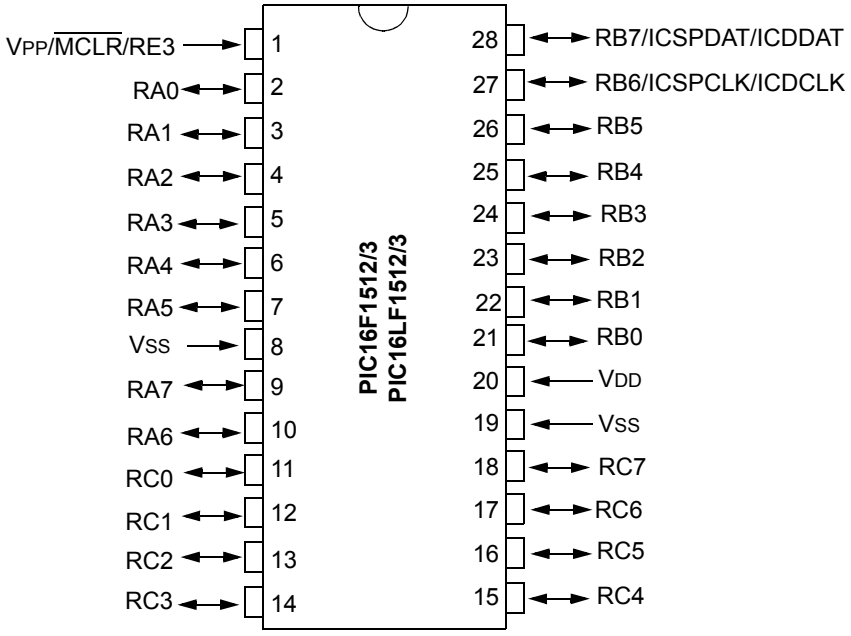

FIGURE 2: 28-PIN UQFN (4X4) PACKAGE DIAGRAM FOR PIC16(L)F1512/3

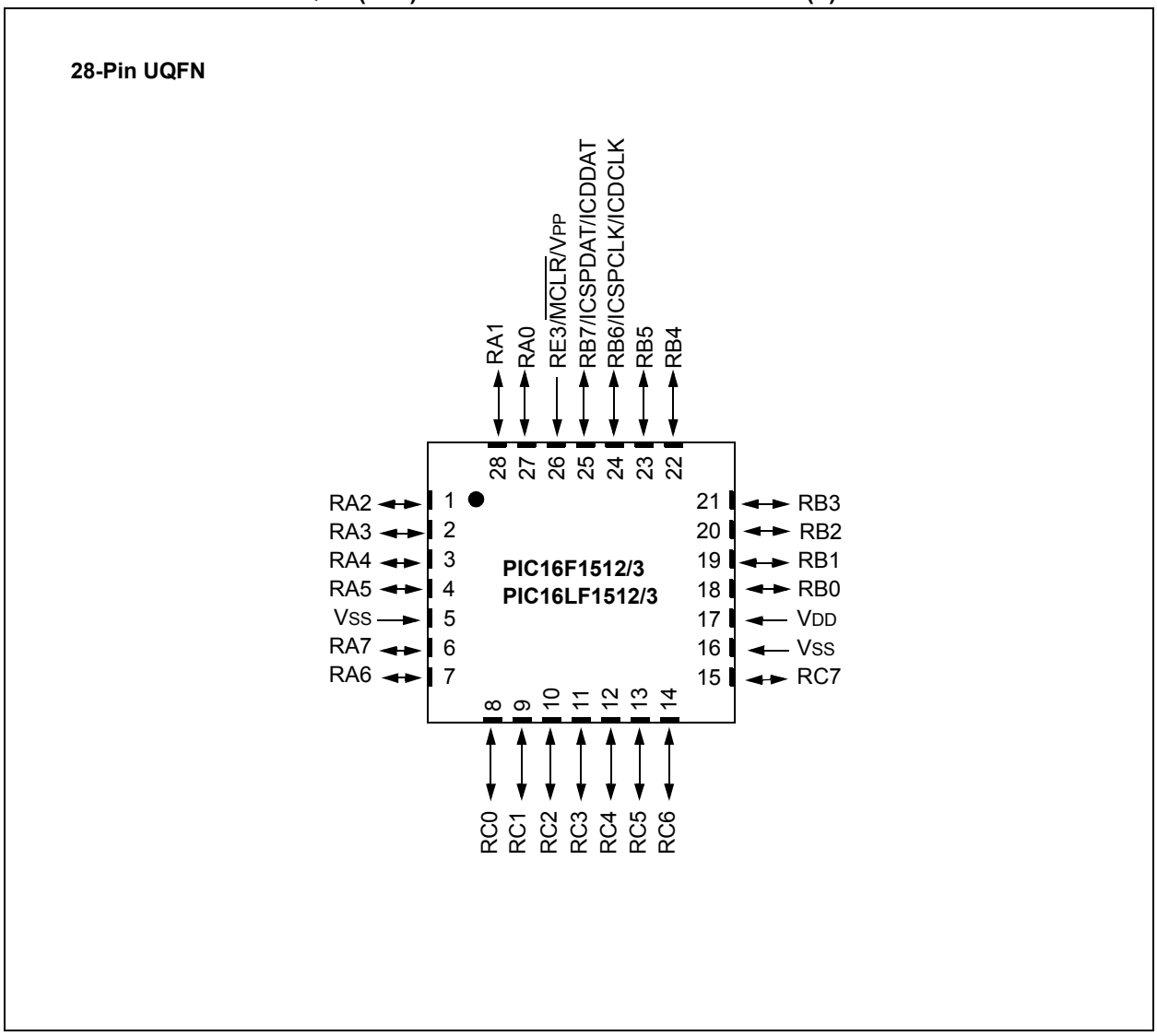

TABLE 1: 28-PIN ALLOCATION TABLE (PIC16(L)F1512/3)

I/O	28-Pin SPDIP, SOIC, SSOP	28-Pin UQFN	A/D	Timers	CCP	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	2	27	AN0	—	—	—	$\overline{SS}$(2)	—	—	—
RA1	3	28	AN1	—	—	—	—	—	—	—
RA2	4	1	AN2	—	—	—	—	—	—	—
RA3	5	2	AN3/VREF+	—	—	—	—	—	—	—
RA4	6	3	—	T0CKI	—	—	—	—	—	—
RA5	7	4	AN4	—	—	—	$\overline{SS}$(1)	—	—	VCAP
RA6	10	7	—	—	—	—	—	—	—	OSC2/CLKOUT
RA7	9	6	—	—	—	—	—	—	—	OSC1/CLKIN
RB0	21	18	AN12	—	—	—	—	INT/IOC	Y	—
RB1	22	19	AN10	—	—	—	—	IOC	Y	—
RB2	23	20	AN8	—	—	—	—	IOC	Y	—
RB3	24	21	AN9	—	CCP2(2)	—	—	IOC	Y	—
RB4	25	22	AN11 ADOUT	—	—	—	—	IOC	Y	—
RB5	26	23	AN13	T1G	—	—	—	IOC	Y	—
RB6	27	24	ADGRDA	—	—	—	—	IOC	Y	ICSPCLK/ICDCLK
RB7	28	25	ADGRDB	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	11	8	—	SOSCO/T1CKI	—	—	—	—	—	—
RC1	12	9	—	SOSCI	CCP2(1)	—	—	—	—	—
RC2	13	10	AN14	—	CCP1	—	—	—	—	—
RC3	14	11	AN15	—	—	—	SCK/SCL	—	—	—
RC4	15	12	AN16	—	—	—	SDI/SDA	—	—	—
RC5	16	13	AN17	—	—	—	SDO	—	—	—
RC6	17	14	AN18	—	—	TX/CK	—	—	—	—
RC7	18	15	AN19	—	—	RX/DT	—	—	—	—
RE3	1	26	—	—	—	—	—	—	Y	$\overline{MCLR}$/VPP
VDD	20	17	—	—	—	—	—	—	—	—
VSS	8,19	5,16	—	—	—	—	—	—	—	—
NC	—	—	—	—	—	—	—	—	—	—

Note 1: Peripheral pin location selected using APFCON register. Default location.
2: Peripheral pin location selected using APFCON register. Alternate location.

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