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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

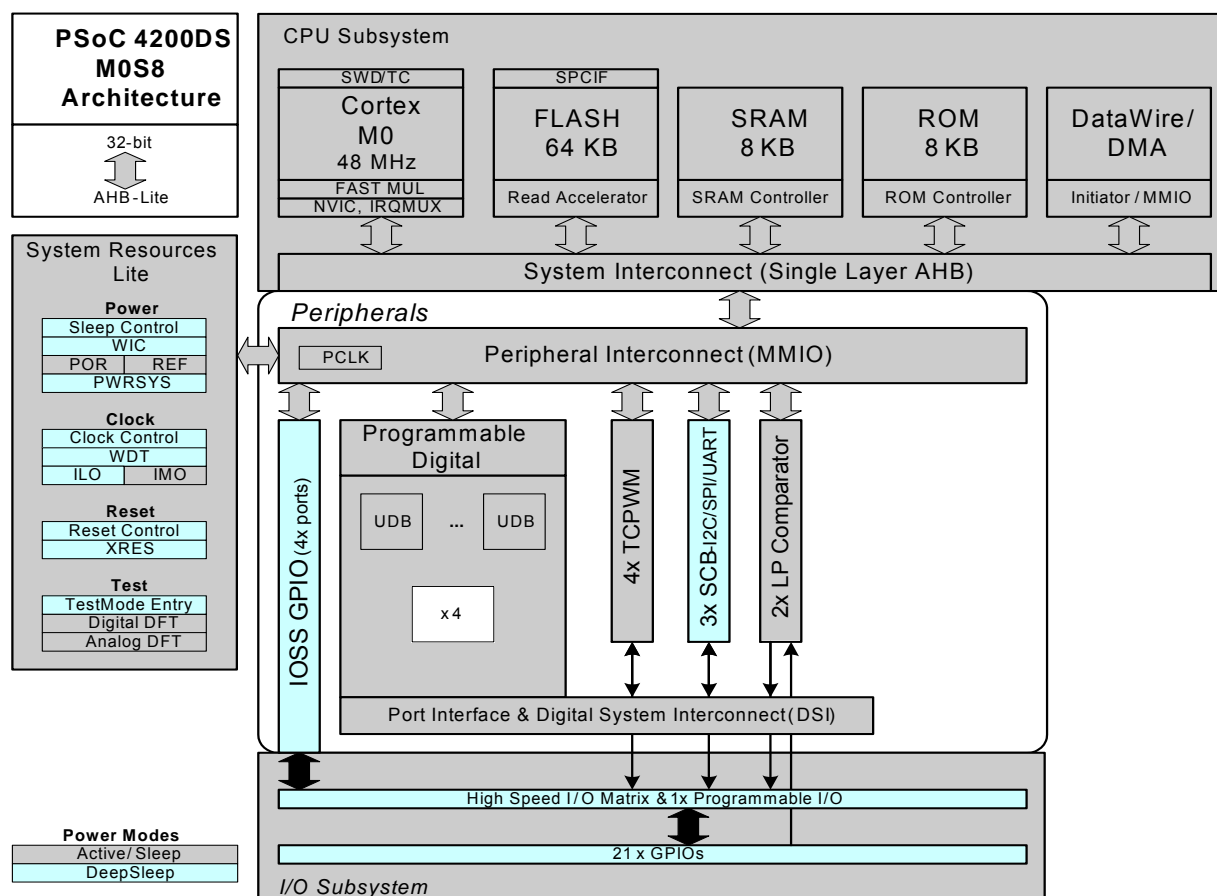
#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	25-UFBGA, WLCSP
Supplier Device Package	25-WLCSP (2.07×2.11)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4245fni-ds402t">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4245fni-ds402t</a>

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## PSoC 4200DS Block Diagram



The PSoC 4200DS devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial\_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 4200DS devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4200DS family provides a level of security not possible with multi-chip application solutions or with microcontrollers. This is due to its ability to disable debug features, robust flash protection, and

because it allows customer-proprietary functionality to be implemented in on-chip programmable blocks.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4200DS with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4200DS allows the customer to make.

### Reset

The PSoC 4200DS can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

### Analog Block

#### Low-power Comparators

The PSoC 4200DS has a pair of low-power comparators, with two different power modes allowing trade-off of power versus response time.

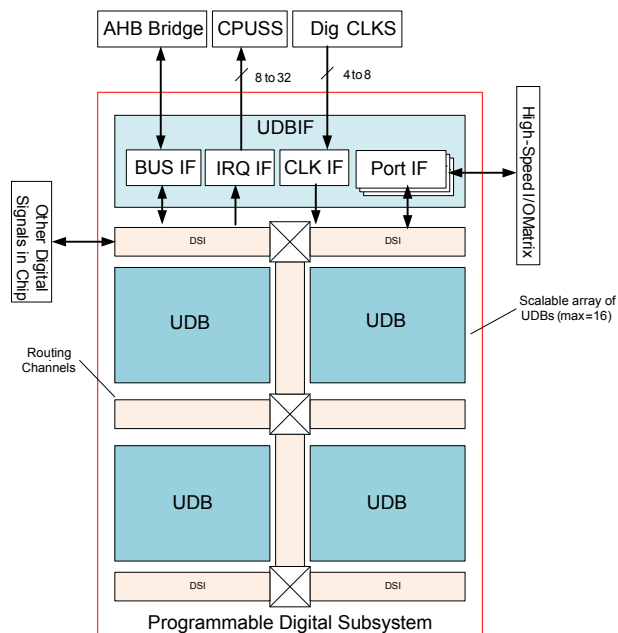
### Programmable Digital

#### Universal Digital Blocks (UDBs) and Port Interfaces

The PSoC 4200DS has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. The UDB array is shown in the following figure.

UDBs can be clocked from a clock divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

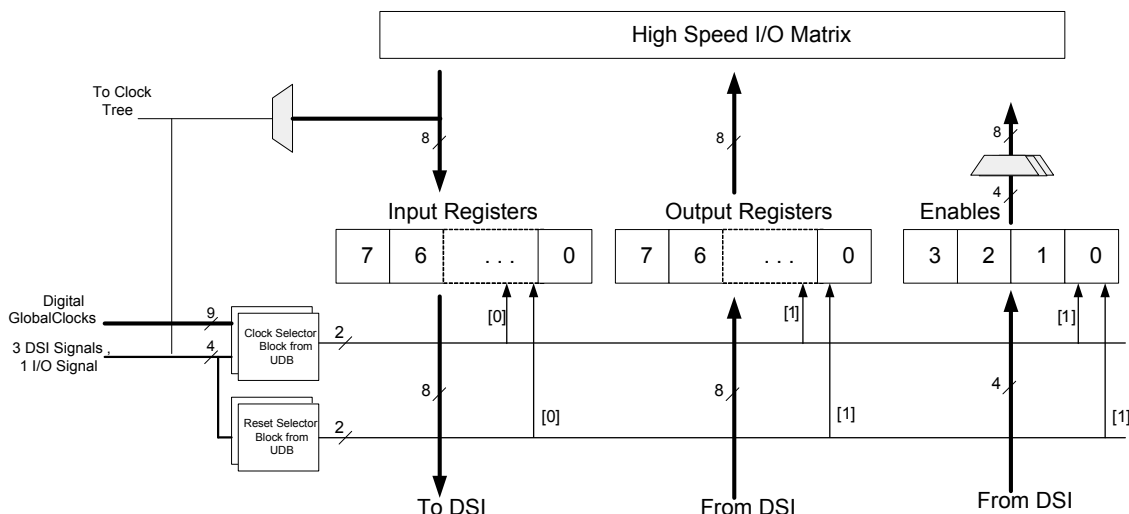
**Figure 3. UDB Array**



A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs. The port interface is shown in Figure 4.

The UDBs can generate interrupts (one UDB at a time) to the interrupt controller. The UDBs retain the ability to connect to any pin on the chip through the DSI.

**Figure 4. Port Interface**



## Pinouts

The following is the pin list for the PSoC 4200DS. Pins 16, 17, and 18 are No-Connects in the 28-pin SSOP package.

**Table 1. PSoC 4200DS Pin Description**

28-Pin SSOP		25-Ball CSP		Alternate Functions for Pins						Pin Description
Pin	Name	Pin	Name	Analog	PRGIO	Alt 1	Alt 2	Alt 3	Alt 4	
19	P0.0	E4	P0.0	lpcomp.in_p[0]		tcpwm.line[2]			scb[0].spi_select <sub>1</sub>	P0.0, LPC0, TCPWM2, SCB0
20	P0.1	E3	P0.1	lpcomp.in_n[0]		tcpwm.line_compl[ <sub>2</sub> ]			scb[0].spi_select <sub>2</sub>	P0.1, LPC0, TCPWM2, SCB0
21	P0.2	D3	P0.2			tcpwm.line[3]			scb[0].spi_select <sub>3</sub>	P0.2, TCPWM3, SCB0
22	P0.4	E2	P0.4				scb[1].uart_rx	scb[1].i2c_sc <sub>1</sub>	scb[1].spi_mosi	P0.4, SCB1
23	P0.5	C4	P0.5				scb[1].uart_tx	scb[1].i2c_sd <sub>a</sub>	scb[1].spi_miso	P0.5, SCB1
24	P0.6	C3	P0.6			ext_clk	scb[1].uart_cts		scb[1].spi_clk	P0.6, Ext Clock, SCB1
25	XRES	D2	XRES							XRES
26	VCCD	E1	VCCD							Regulator Output
28	VSSD	D1	VSSD							Power Supply
27	VDDD	C1	VDDD							Ground
1	P1.0	C2	P1.0			tcpwm.line[2]	scb[0].uart_rx	scb[0].i2c_sc <sub>1</sub>	scb[0].spi_mosi	P1.0, TCPWM2, SCB0
2	P1.1	B2	P1.1			tcpwm.line_compl[ <sub>2</sub> ]	scb[0].uart_tx	scb[0].i2c_sd <sub>a</sub>	scb[0].spi_miso	P1.1, TCPWM2, SCB0
3	P1.2	B1	P1.2			tcpwm.line[3]	scb[0].uart_cts		scb[0].spi_clk	P1.2, TCPWM3, SCB0
4	P1.3	A1	P1.3			tcpwm.line_compl[ <sub>3</sub> ]	scb[0].uart_rts		scb[0].spi_select <sub>0</sub>	P1.3, TCPWM3, SCB0
5	P2.2	B3	P2.2		prgio[0].io[2]		scb[2].uart_rx	scb[2].i2c_sc <sub>1</sub>	scb[2].spi_mosi	P2.2, PRG, SCB2
6	P2.3	A2	P2.3		prgio[0].io[3]		scb[2].uart_tx	scb[2].i2c_sd <sub>a</sub>	scb[2].spi_miso	P2.3, PRG, SCB2
7	P2.4	B4	P2.4		prgio[0].io[4]	tcpwm.line[0]	scb[2].uart_cts	lpcomp.comp[0]	scb[2].spi_clk	P2.4, PRG, TCPWM0, SCB2, LPC0
8	P2.5	A4	P2.5		prgio[0].io[5]	tcpwm.line_compl[ <sub>0</sub> ]	scb[2].uart_rts		scb[2].spi_select <sub>0</sub>	P2.5, PRG, TCPWM0, SCB2
9	P2.6	A3	P2.6		prgio[0].io[6]	tcpwm.line[1]			scb[2].spi_select <sub>1</sub>	P2.6, PRG, TCPWM1, SCB2
10	P2.7	A5	P2.7		prgio[0].io[7]	tcpwm.line_compl[ <sub>1</sub> ]			scb[2].spi_select <sub>2</sub>	P2.7, PRG, TCPWM1, SCB2

**Table 1. PSoC 4200DS Pin Description** *(continued)*

28-Pin SSOP		25-Ball CSP		Alternate Functions for Pins						Pin Description
Pin	Name	Pin	Name	Analog	PRGIO	Alt 1	Alt 2	Alt 3	Alt 4	
11	P3.0	D5	P3.0			tcpwm.line[0]	scb[1].uart_rx	scb[1].i2c_sc l	scb[1].spi_mosi	P3.0, TCPWM0, SCB1
12	P3.1	C5	P3.1			tcpwm.line_compl[ 0]	scb[1].uart_tx	scb[1].i2c_sd a	scb[1].spi_miso	P3.1, TCPWM0, SCB1
13	P3.2	E5	P3.2			tcpwm.line[1]	scb[1].uart_cts	swd_data	scb[1].spi_clk	P3.2, TCPWM1, SCB1, SWD_IO
14	P3.3	B5	P3.3			tcpwm.line_compl[ 1]	scb[1].uart_rts	swd_clk	scb[1].spi_select 0	P3.3, TCPWM1, SCB1, SWD_CLK
15	P3.4	D4	P3.4						scb[1].spi_select 1	P3.4, SCB1

**Descriptions of the power pin functions are as follows:**

**VDDD:** Power supply for the chip.

**VSSD:** Ground pin.

**VCCD:** Regulated digital supply (1.8 V ±5% if supplied externally).

## Electrical Specifications

### Absolute Maximum Ratings

**Table 2. Absolute Maximum Ratings**<sup>[1]</sup>

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID1	V <sub>DD_ABS</sub>	Analog or digital supply relative to V <sub>SS</sub> (V <sub>SSD</sub> = V <sub>SSA</sub> )	−0.5	—	6	V	Absolute maximum
SID2	V <sub>CCD_ABS</sub>	Direct digital core voltage input relative to V <sub>SSD</sub>	−0.5	—	1.95	V	Absolute maximum
SID3	V <sub>GPIO_ABS</sub>	GPIO voltage; V <sub>DDD</sub> or V <sub>DDA</sub>	−0.5	—	V <sub>DD</sub> +0.5	V	Absolute maximum
SID4	I <sub>GPIO_ABS</sub>	Current per GPIO	−25	—	25	mA	Absolute maximum
SID5	I <sub>G-PIO_injection</sub>	GPIO injection current per pin	−0.5	—	0.5	mA	Absolute maximum
BID44	ESD_HBM	Electrostatic discharge human body model	2200	—	—	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	—	—	V	
BID46	LU	Pin current for latch-up	−140	—	140	mA	

### Device Level Specifications

All specifications are valid for −40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

**Table 3. DC Specifications**

Spec Id#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID53	V <sub>DDD</sub>	Power supply input voltage unregulated	1.8	—	5.5	V	With on-chip internal regulator enabled
SID255	V <sub>DDD</sub>	Power supply input voltage externally regulated	1.71	1.8	1.89	V	Externally regulated within this range
SID54	V <sub>CCD</sub>	Output voltage (for core logic)	—	1.8	—	V	
SID55	C <sub>EFC</sub>	External regulator voltage bypass	—	0.1	—	μF	X5R ceramic or better
SID56	C <sub>EXC</sub>	Power supply decoupling capacitor	—	1	—	μF	X5R ceramic or better

#### Active Mode

SID6	I <sub>DD1</sub>	Execute from flash; CPU at 6 MHz	—	2.1	2.85	mA	
SID7	I <sub>DD2</sub>	Execute from flash; CPU at 12 MHz	—	3.6	4	mA	
SID8	I <sub>DD3</sub>	Execute from flash; CPU at 24 MHz	—	5.3	6	mA	
SID9	I <sub>DD4</sub>	Execute from flash; CPU at 48 MHz	—	9.8	13	mA	

#### Sleep Mode

SID21	I <sub>DD16</sub>	I <sup>2</sup> C wakeup, WDT, and comparators on. Regulator off.	—	1.45	1.65	mA	V <sub>DD</sub> = 1.71 to 1.89, 6 MHz
SID22	I <sub>DD17</sub>	I <sup>2</sup> C wakeup, WDT, and comparators on.	—	1.8	2.45	mA	V <sub>DD</sub> = 1.8 to 5.5, 6 MHz
SID23	I <sub>DD18</sub>	I <sup>2</sup> C wakeup, WDT, and comparators on. Regulator off.	—	1.6	1.9	mA	V <sub>DD</sub> = 1.71 to 1.89, 12 MHz

#### Note

- Usage above the absolute maximum conditions listed in Table 2 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

**Table 3. DC Specifications** (continued)

Spec Id#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID24	I <sub>DD19</sub>	I <sup>2</sup> C wakeup, WDT, and comparators on.	–	2	2.7	mA	V <sub>DD</sub> = 1.8 to 5.5, 12 MHz
<b>Deep Sleep Mode, -40 °C to + 60 °C (Guaranteed by characterization)</b>							
SID30	I <sub>DD25</sub>	I <sup>2</sup> C wakeup and WDT on. Regulator off.	–	2	15	μA	V <sub>DD</sub> = 1.71 to 1.89
SID31	I <sub>DD26</sub>	I <sup>2</sup> C wakeup and WDT on.	–	2	15	μA	V <sub>DD</sub> = 1.8 to 3.6
SID32	I <sub>DD27</sub>	I <sup>2</sup> C wakeup and WDT on.	–	2	15	μA	V <sub>DD</sub> = 3.6 to 5.5
<b>Deep Sleep Mode, +85 °C (Guaranteed by characterization)</b>							
SID33	I <sub>DD28</sub>	I <sup>2</sup> C wakeup and WDT on. Regulator off.	–	4	45	μA	V <sub>DD</sub> = 1.71 to 1.89
SID34	I <sub>DD29</sub>	I <sup>2</sup> C wakeup and WDT on.	–	4	45	μA	V <sub>DD</sub> = 1.8 to 3.6
SID35	I <sub>DD30</sub>	I <sup>2</sup> C wakeup and WDT on.	–	4	45	μA	V <sub>DD</sub> = 3.6 to 5.5
<b>XRES current</b>							
SID307	I <sub>DD_XR</sub>	Supply current while XRES (Active Low) asserted	–	2	5	mA	

**Table 4. AC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F <sub>CPU</sub>	CPU frequency	DC	–	48	MHz	1.71 ≤ V <sub>DD</sub> ≤ 5.5
SID49	T <sub>SLEEP</sub>	Wakeup from sleep mode	–	0	–	μs	Guaranteed by characterization
SID50	T <sub>DEEPSLEEP</sub>	Wakeup from Deep Sleep mode	–	–	35	μs	Guaranteed by characterization
SID52	T <sub>RESETWIDTH</sub>	External reset pulse width	1	–	–	μs	Guaranteed by characterization

#### GPIO

**Table 5. GPIO DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V <sub>IH</sub> <sup>[2]</sup>	Input voltage high threshold	0.7 × V <sub>DDD</sub>	–	–	V	CMOS Input
SID58	V <sub>IL</sub>	Input voltage low threshold	–	–	0.3 × V <sub>DDD</sub>	V	CMOS Input
SID241	V <sub>IH</sub> <sup>[2]</sup>	LVTTL input, V <sub>DDD</sub> < 2.7 V	0.7 × V <sub>DDD</sub>	–	–	V	
SID242	V <sub>IL</sub>	LVTTL input, V <sub>DDD</sub> < 2.7 V	–	–	0.3 × V <sub>DDD</sub>	V	
SID243	V <sub>IH</sub> <sup>[2]</sup>	LVTTL input, V <sub>DDD</sub> ≥ 2.7 V	2.0	–	–	V	
SID244	V <sub>IL</sub>	LVTTL input, V <sub>DDD</sub> ≥ 2.7 V	–	–	0.8	V	
SID59	V <sub>OH</sub>	Output voltage high level	V <sub>DDD</sub> – 0.6	–	–	V	I <sub>OH</sub> = 4 mA at 3 V V <sub>DDD</sub>
SID60	V <sub>OH</sub>	Output voltage high level	V <sub>DDD</sub> – 0.5	–	–	V	I <sub>OH</sub> = 1 mA at 1.8 V V <sub>DDD</sub>
SID61	V <sub>OL</sub>	Output voltage low level	–	–	0.6	V	I <sub>OL</sub> = 4 mA at 1.8 V V <sub>DDD</sub>

**Note**

2. V<sub>IH</sub> must not exceed V<sub>DDD</sub> + 0.2 V.



**Table 5. GPIO DC Specifications** (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID62	$V_{OL}$	Output voltage low level	–	–	0.6	V	$I_{OL} = 8 \text{ mA}$ at 3 V $V_{DDD}$
SID62A	$V_{OL}$	Output voltage low level	–	–	0.4	V	$I_{OL} = 3 \text{ mA}$ at 3 V $V_{DDD}$
SID63	$R_{PULLUP}$	Pull-up resistor	3.5	5.6	8.5	k $\Omega$	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	k $\Omega$	
SID65	$I_{IL}$	Input leakage current (absolute value)	–	–	2	nA	25 °C, $V_{DDD} = 3.0 \text{ V}$
SID66	$C_{IN}$	Input capacitance	–	–	7	pF	
SID67	$V_{HYSTTL}$	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \geq 2.7 \text{ V}$
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DDD}$	–	–	mV	
SID69	$I_{DIODE}$	Current through protection diode to $V_{DD}/V_{SS}$	–	–	100	$\mu\text{A}$	Guaranteed by characterization
SID69A	$I_{TOT\_GPIO}$	Maximum Total Source or Sink Chip Current	–	–	200	mA	Guaranteed by characterization

**Table 6. GPIO AC Specifications**

 (Guaranteed by Characterization)<sup>[3]</sup>

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	$T_{RISEF}$	Rise time in fast strong mode	2	–	12	ns	3.3 V $V_{DDD}$ , Load = 25 pF
SID71	$T_{FALLF}$	Fall time in fast strong mode	2	–	12	ns	3.3 V $V_{DDD}$ , Load = 25 pF
SID72	$T_{RISES}$	Rise time in slow strong mode	10	–	60	ns	3.3 V $V_{DDD}$ , Load = 25 pF
SID73	$T_{FALLS}$	Fall time in slow strong mode	10	–	60	ns	3.3 V $V_{DDD}$ , Load = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout; 3.3 V $\leq V_{DDD} \leq 5.5 \text{ V}$ . Fast strong mode.	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout; 1.7 V $\leq V_{DDD} \leq 3.3 \text{ V}$ . Fast strong mode.	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout; 3.3 V $\leq V_{DDD} \leq 5.5 \text{ V}$ . Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout; 1.7 V $\leq V_{DDD} \leq 3.3 \text{ V}$ . Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	$F_{GPIOIN}$	GPIO input operating frequency; 1.71 V $\leq V_{DDD} \leq 5.5 \text{ V}$	–	–	48	MHz	90/10% $V_{IO}$

**Note**

3. Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.

## XRES

**Table 7. XRES DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	$V_{IH}$	Input voltage high threshold	$0.7 \times V_{DDD}$	–	–	V	CMOS Input
SID78	$V_{IL}$	Input voltage low threshold	–	–	$0.3 \times V_{DDD}$	V	CMOS Input
SID79	$R_{PULLUP}$	Pull-up resistor	3.5	5.6	8.5	k $\Omega$	
SID80	$C_{IN}$	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	$I_{DIODE}$	Current through protection diode to $V_{DDD}/V_{SS}$	–	–	100	$\mu$ A	Guaranteed by characterization

**Table 8. XRES AC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	$\mu$ s	Guaranteed by characterization

## Analog Peripherals

### Comparator

**Table 9. Comparator DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID85	$V_{OFFSET2}$	Input offset voltage, Common Mode voltage range from 0 to $V_{DD}-1$	–	–	$\pm 4$	mV	
SID86	$V_{HYST}$	Hysteresis when enabled, Common Mode voltage range from 0 to $V_{DD}-1$ .	–	10	35	mV	Guaranteed by characterization
SID87	$V_{ICM1}$	Input common mode voltage in normal mode	0	–	$V_{DDD} - 0.1$	V	Modes 1 and 2.
SID247	$V_{ICM2}$	Input common mode voltage in low-power mode	0	–	$V_{DDD}$	V	
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	$V_{DDD} \geq 2.7$ V. Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	–	–	dB	$V_{DDD} < 2.7$ V. Guaranteed by characterization
SID89	$I_{CMP1}$	Block current, normal mode	–	–	400	$\mu$ A	Guaranteed by characterization
SID248	$I_{CMP2}$	Block current, low power mode	–	–	100	$\mu$ A	Guaranteed by characterization
SID90	$Z_{CMP}$	DC input impedance of comparator	35	–	–	M $\Omega$	Guaranteed by characterization

**Table 10. Comparator AC Specifications**

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	$T_{RESP1}$	Response time, normal mode	–	–	110	ns	50-mV overdrive
SID258	$T_{RESP2}$	Response time, low power mode	–	–	200	ns	50-mV overdrive

## Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode.

Timer/Counter/PWM

**Table 11. TCPWM Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	–	–	Fc	MHz	Fc max = Fcpu. Maximum = 48 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width for all Trigger Events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs.

I<sup>2</sup>C

**Table 12. Fixed I<sup>2</sup>C DC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I <sub>I2C1</sub>	Block current consumption at 100 kHz	–	–	50	μA	
SID150	I <sub>I2C2</sub>	Block current consumption at 400 kHz	–	–	135	μA	
SID151	I <sub>I2C3</sub>	Block current consumption at 1 Mbps	–	–	310	μA	
SID152	I <sub>I2C4</sub>	I <sup>2</sup> C enabled in Deep Sleep mode	–	–	1.4	μA	

**Table 13. Fixed I<sup>2</sup>C AC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F <sub>I2C1</sub>	Bit rate	–	–	1	Mbps	

**Table 14. Fixed UART DC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I <sub>UART1</sub>	Block current consumption at 100 Kbits/sec	–	–	55	μA	
SID161	I <sub>UART2</sub>	Block current consumption at 1000 Kbits/sec	–	–	312	μA	

**Table 15. Fixed UART AC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F <sub>UART</sub>	Bit rate	–	–	1	Mbps	

#### SPI Specifications

**Table 16. Fixed SPI DC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I <sub>SPI1</sub>	Block current consumption at 1 Mbits/sec	–	–	360	μA	
SID164	I <sub>SPI2</sub>	Block current consumption at 4 Mbits/sec	–	–	560	μA	
SID165	I <sub>SPI3</sub>	Block current consumption at 8 Mbits/sec	–	–	600	μA	

**Table 17. Fixed SPI AC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F <sub>SPI</sub>	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	

**Table 18. Fixed SPI Master mode AC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID167	T <sub>DMO</sub>	MOSI valid after Sclk driving edge	–	–	15	ns
SID168	T <sub>DSI</sub>	MISO valid before Sclk capturing edge. Full clock, late MISO Sampling used	20	–	–	ns
SID169	T <sub>HMO</sub>	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns

**Table 19. Fixed SPI Slave mode AC Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID170	$T_{DMI}$	MOSI valid before Scklock capturing edge	40	–	–	ns
SID171	$T_{DSO}$	MISO valid after Scklock driving edge	–	–	$42 + 3 \times (1/FCPU)$	ns
SID171A	$T_{DSO\_ext}$	MISO valid after Scklock driving edge in Ext. Clock mode	–	–	48	ns
SID172	$T_{HSO}$	Previous MISO data hold time	0	–	–	ns
SID172A	$T_{SSELCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns

## Memory

**Table 20. Flash DC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	$V_{PE}$	Erase and program voltage	1.71	–	5.5	V	

**Table 21. Flash AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
SID175	$T_{ROWERASE}$	Row erase time	–	–	13	ms	
SID176	$T_{ROWPROGRAM}$	Row program time after erase	–	–	7	ms	
SID178	$T_{BULKERASE}$	Bulk erase time (64 KB)	–	–	35	ms	
SID180	$T_{DEVPROG}$	Total device program time	–	–	15	seconds	Guaranteed by characterization
SID181	$F_{END}$	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	$F_{RET}$	Flash retention. $T_A \leq 55^\circ\text{C}$ , 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A		Flash retention. $T_A \leq 85^\circ\text{C}$ , 10 K P/E cycles	10	–	–	years	Guaranteed by characterization

## System Resources

*Power-on-Reset and Brown-out Detect (BOD) Specifications*
**Table 22. Power On Reset**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization
BID51	Twupo	Initialization after Power-On	–	–	3	ms	

**Table 23. Brown-out Detect (BOD) for  $V_{CCD}$** 

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	-	1.62	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.11	-	1.5	V	Guaranteed by characterization

#### SWD Interface

**Table 24. SWD Interface Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	$F_{\_SWDCLK1}$	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	$SWDCLK \leq 1/3$ CPU clock frequency
SID214	$F_{\_SWDCLK2}$	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7	MHz	$SWDCLK \leq 1/3$ CPU clock frequency
SID215	$T_{\_SWDI\_SETUP}$	$T = 1/f_{SWDCLK}$	$0.25 \cdot T$	–	–	ns	Guaranteed by characterization
SID216	$T_{\_SWDI\_HOLD}$	$T = 1/f_{SWDCLK}$	$0.25 \cdot T$	–	–	ns	Guaranteed by characterization
SID217	$T_{\_SWDO\_VALID}$	$T = 1/f_{SWDCLK}$	–	–	$0.5 \cdot T$	ns	Guaranteed by characterization
SID217A	$T_{\_SWDO\_HOLD}$	$T = 1/f_{SWDCLK}$	1	–	–	ns	Guaranteed by characterization

#### Internal Main Oscillator

**Table 25. IMO DC Specifications**

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	$I_{IMO1}$	IMO operating current at 48 MHz	–	–	250	$\mu\text{A}$	
SID219	$I_{IMO2}$	IMO operating current at 24 MHz	–	–	180	$\mu\text{A}$	

**Table 26. IMO AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation	–	–	$\pm 2$	%	
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	$\mu\text{s}$	
SID228	$T_{JITRMSIMO2}$	RMS Jitter at 24 MHz	–	145	–	ps	

#### Internal Low-Speed Oscillator

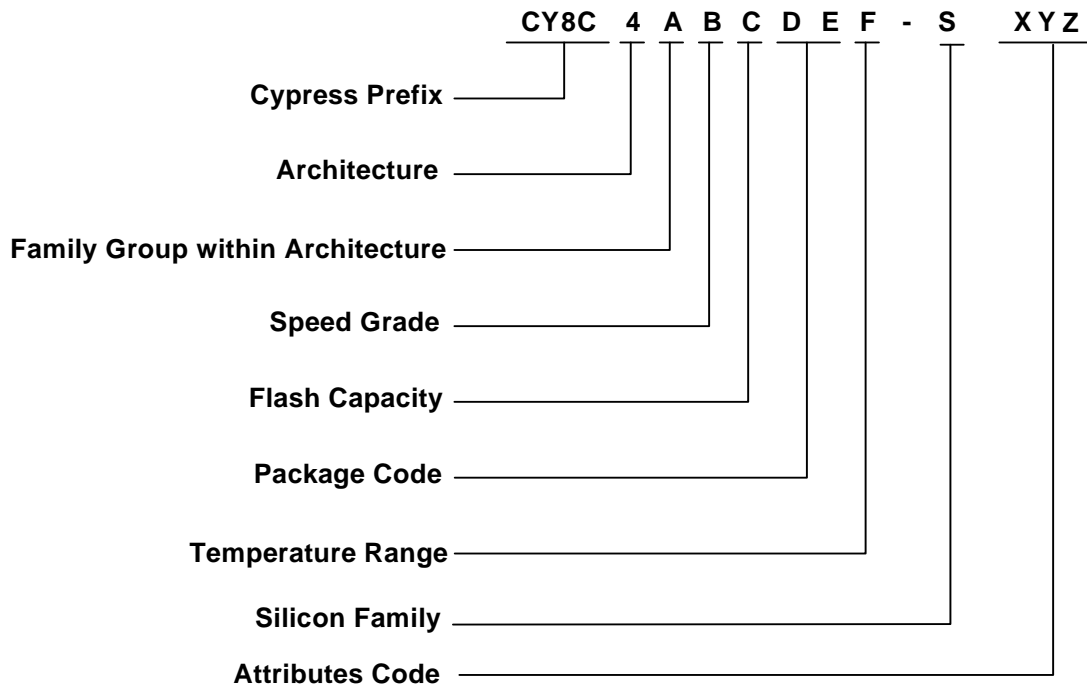
**Table 27. ILO DC Specifications**

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	$I_{ILO1}$	ILO operating current	–	0.3	1.05	$\mu\text{A}$	Guaranteed by Characterization

### Part Numbering Conventions

The part number fields are defined as follows.



## Packaging

The description of the PSoC 4200D package dimensions follows.

Spec Id#	Package	Description	Package Dwg #
PKG_1	28-pin SSOP	28-pin SSOP, 8 mm × 10 mm × 2.0 mm height with 0.65-mm pitch	51-85079
PKG_2	25-ball CSP	25-ball CSP, 2.07 mm × 2.11 mm × 0.55 mm height with 0.4-mm pitch	001-97945

**Table 33. Package Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Units
T <sub>A</sub>	Operating ambient temperature		−40	25	85	°C
T <sub>J</sub>	Operating junction temperature		−40		100	°C
T <sub>JA</sub>	Package θ <sub>JA</sub> (28-pin SSOP)		–	67	–	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (28-pin SSOP)		–	26	–	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (25-ball CSP)		–	48	–	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (25-ball CSP)		–	0.47	–	°C/Watt

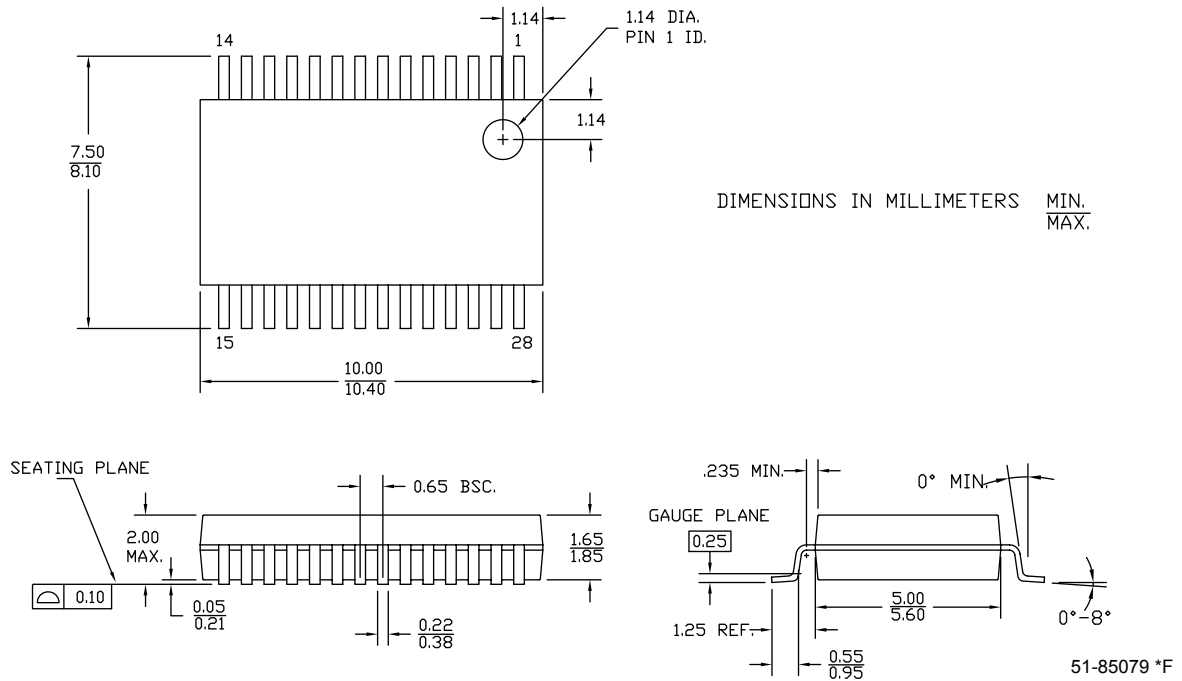
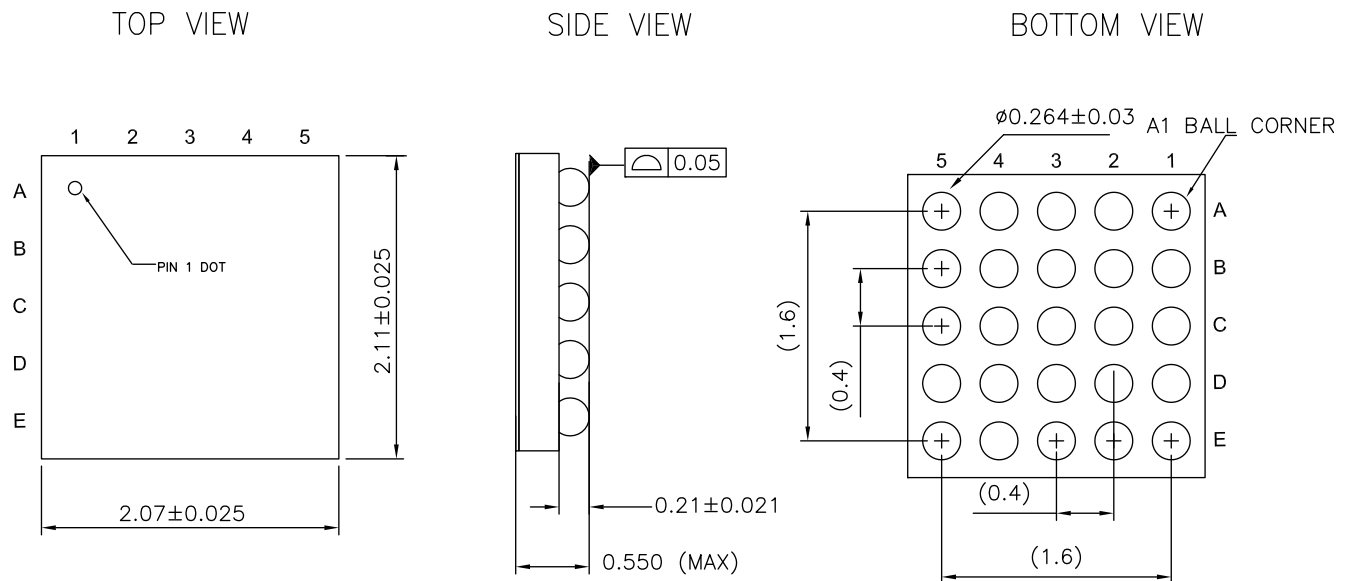
**Table 34. Solder Reflow Peak Temperature**

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds

**Table 35. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

Package	MSL
28-pin SSOP	MSL 3
25-ball CSP	MSL 1



**Figure 5. 28-Pin SSOP Package Outline**

**Figure 6. 25-ball CSP 2.07 × 2.11 × 0.55 mm**


Note: 1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18  
 2. ALL DIMENSIONS ARE IN MILLIMETER

001-97945 \*\*

## Acronyms

**Table 36. Acronyms Used in this Document**

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

**Table 36. Acronyms Used in this Document** *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I <sup>2</sup> C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board

## Document Conventions

### Units of Measure

**Table 37. Units of Measure**

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

## Revision History

Description Title: PSoC® 4: PSoC 4200DS Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-98044				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4795389	WKA	06/23/2015	New datasheet
*A	4931127	WKA	09/23/2015	Removed 28-pin SSOP package. Updated Pinouts. Updated DC Specifications. Removed SID85A, SID247A, SID259, and SID92. Added BID51.
*B	4958966	WKA	10/12/2015	Updated package dimensions. Updated bulk erase time to 64 KB. Changed SID226 max to 7. Updated T <sub>JA</sub> typ to 48 and T <sub>JC</sub> typ to 0.47.
*C	5759255	WKA	05/31/2017	Added 28-pin SSOP package. Updated to new template.
*D	5825921	WKA	07/20/2017	Updated Document Title to read as "PSoC® 4: PSoC 4200DS Family Datasheet Programmable System-on-Chip (PSoC®)". Replaced "PSoC 4200D" with "PSoC 4200DS" in all instances across the document.

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