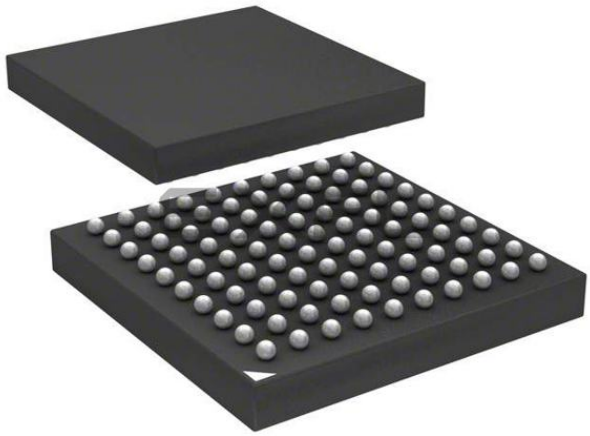

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, I²C, SPI, SSI, SSP, UART/USART, USB
Peripherals	DMA, PWM, WDT
Number of I/O	72
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str750fv1h6

1 Description

The STR750 family of 32-bit microcontrollers combines the industry-standard ARM7TDMI® 32-bit RISC core, featuring high performance, very low power, and very dense code, with a comprehensive set of peripherals and ST's latest 0.18µ embedded Flash technology. The STR750 family comprises a range of devices integrating a common set of peripherals as well as USB, CAN and some key innovations like clock failure detection and an advanced motor control timer. It supports both 3.3V and 5V, and it is also available in an extended temperature range (-40 to +105°C). This makes it a genuine general purpose microcontroller family, suitable for a wide range of applications:

- Appliances, brushless motor drives
- USB peripherals, UPS, alarm systems
- Programmable logic controllers, circuit breakers, inverters
- Medical and portable equipment

2 Device overview

Table 2. Device overview

Features	STR755FR0 STR755FR1 STR755FR2	STR751FR0/ STR751FR1/ STR751FR2	STR752FR0/ STR752FR1/ STR752FR2	STR755FV0 STR755FV1/ STR755FV2	STR750FV0/ STR750FV1/ STR750FV2
Flash - Bank 0 (bytes)	64K/128K/256K				
Flash - Bank 1 (bytes)	16K RWW				
RAM (bytes)	16K				
Operating Temperature.	Ambient temp.:-40 to +85°C / -40 to +105°C (see *Table 49*) Junction temp. -40 to + 125 °C (see *Table 10*)				
Common Peripherals	3 UARTs, 2 SSPs, 1 I2C, 3 timers 1 PWM timer, 38 I/Os 13 Wake-up lines, 11 A/D Channels			3 UARTs, 2 SSPs, 1 I^2C, 3 timers 1 PWM timer, 72 I/Os 15 Wake-up lines, 16 A/D Channels	
USB/CAN peripherals	None	USB	CAN	None	USB+CAN
Operating Voltage	3.3V or 5V	3.3V	3.3V or 5V		
Packages (**x**)	**T**=LQFP64 10x10, **H**=LFBGA64			**T**=LQFP100 14x14, **H**=LFBGA100	

periodic interrupt. It is clocked by an external 32.768 kHz oscillator or the internal low power RC oscillator. The RC has a typical frequency of 300 kHz and can be calibrated.

WDG (watchdog timer)

The watchdog timer is based on a 16-bit downcounter and 8-bit prescaler. It can be used as watchdog to reset the device when a problem occurs, or as free running timer for application time out management.

Timebase timer (TB)

The timebase timer is based on a 16-bit auto-reload counter and not connected to the I/O pins. It can be used for software triggering, or to implement the scheduler of a real-time operating system.

Synchronizable standard timers (TIM2:0)

The three standard timers are based on a 16-bit auto-reload counter and feature up to 2 input captures and 2 output compares (for external triggering or time base / time out management). They can work together with the PWM timer via the Timer Link feature for synchronization or event chaining. In reset state, timer Alternate Function I/Os are connected to the same
I/O ports in both 64-pin and 100-pin devices. To optimize timer functions in 64-pin devices, timer Alternate Function I/Os can be connected, or “remapped”, to other I/O ports as summarized in *Table 3* and detailed in *Table 6*. This remapping is done by the application via a control register.

Table 3. Standard timer alternate function I/Os

Standard timer functions		Number of alternate function I/Os		
		100-pin package	64-pin package	
			Default mapping	Remapped
TIM 0	Input Capture	2	1	2
	Output Compare/PWM	2	1	2
TIM 1	Input Capture	2	1	1
	Output Compare/PWM	2	1	1
TIM 2	Input Capture	2	2	2
	Output Compare/PWM	2	1	2

Any of the standard timers can be used to generate PWM outputs. One timer (TIM0) is mapped to a DMA channel.

Motor control PWM timer (PWM)

The Motor Control PWM Timer (PWM) can be seen as a three-phase PWM multiplexed on 6 channels. The 16-bit PWM generator has full modulation capability (0...100%), edge or centre-aligned patterns and supports dead-time insertion. It has many features in common with the standard TIM timers which has the same architecture and it can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.The PWM timer is mapped to a DMA channel.

4.1 Pin description table

Legend / abbreviations for *Table 6*:

Type:	I = input, O = output, S = supply,
Input levels:	All Inputs are LVTTL at V_{DD_IO} = 3.3V+/-0.3V or TTL at V_{DD_IO} = 5V± 0.5V. In both cases, T_T means V_{ILmax} =0.8V V_{IHmin}=2.0V
Inputs:	All inputs can be configured as floating or with internal weak pull-up or pull down (pu/pd)
Outputs:	All Outputs can be configured as Open Drain (OD) or Push-Pull (PP) (see also note 6 below *Table 6*). There are 3 different types of Output with different drives and speed characteristics: – O8: f_{max} = 40 MHz on C_L=50pF and 8 mA static drive capability for V_{OL}=0.4V and up to 20 mA for V_{OL}=1.3V (see*Output driving current on page 55*) – O4: f_{max} = 20 MHz on C_L=50pF and 4 mA static drive capability for V_{OL}=0.4V (see*Output driving current on page 55*) – O2: f_{max} = 10 MHz on C_L=50pF and 2 mA static drive capability of for V_{OL}=0.4V (see*Output driving current on page 55*)
External interrupts/wake-up lines:	EITx

Table 6. STR750F pin description (continued)

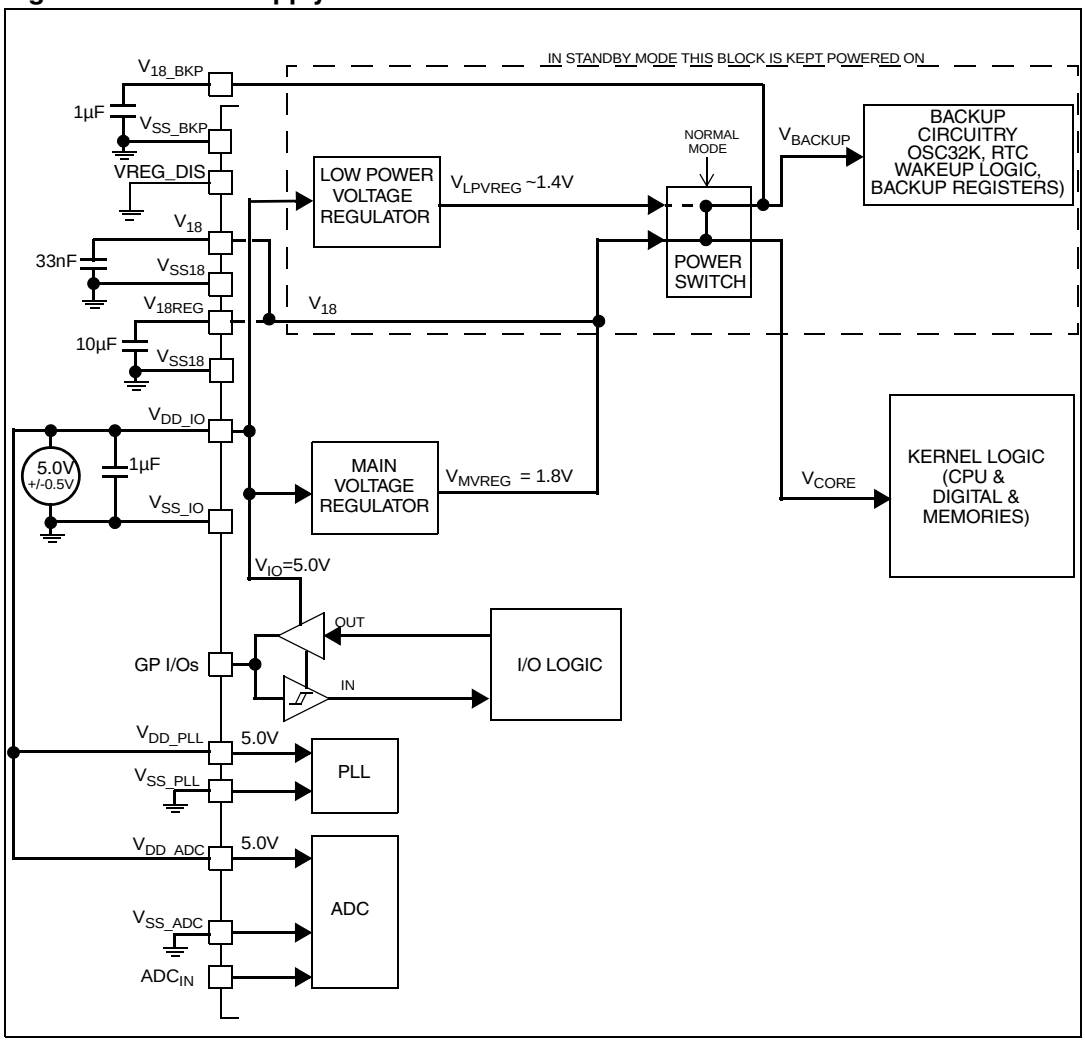
Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
7	D1	5	D1	P0.29 / TIM1_TI1 / ADC_IN8	I/O	T_T	**X**	X		O2	X	X		**Port 0.29**	TIM1: Input Capture 1	ADC: Analog input 8
8	E1	6	D2	P0.28 / TIM1_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 0.28**	TIM1: Output Compare 1	
9	E5	7	D3	TEST	I									Reserved, must be tied to ground		
10	E4	8	D4	VSS_IO	S									Ground Voltage for digital I/Os		
11	E2			P0.23 / UART1_RTS / ADC_IN6	I/O	T_T	**X**	X		O2	X	X		**Port 0.23**	UART1: Ready To Send output(4)	ADC analog input 6
12	F5			P2.04 / TIM2_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 2.04**	TIM2: Output Compare 1(4)	
13	F1			P2.03 / UART1_RTS	I/O	T_T	**X**	X		O2	X	X		**Port 2.03**	UART1: Ready To Send output(4)	
14	F4			P2.02	I/O	T_T	**X**	X		O2	X	X		**Port 2.02**		
15	E3			P0.22 / UART1_CTS / ADC_IN5	I/O	T_T	**X**	X		O2	X	X		**Port 0.22**	UART1: Clear To Send input	ADC: Analog input 5
16	F2	9	E4	P0.21 / UART1_TX	I/O	T_T	**X**	X		O2	X	X		**Port 0.21**	UART1: Transmit data output (remappable to P0.15)(4)	
17	F3	10	E3	P0.20 / UART1_RX	I/O	T_T	**X**	X		O2	X	X		**Port 0.20**	UART1: Receive data input (remappable to P0.14)(4)	
18	G3	11	E2	P1.19 / JTMS	I/O	T_T	X	X		O2	X	X		**JTAG mode selection input(6)**	Port 1.19	
19	G2	12	E1	P1.18 / JTCK	I/O	T_T	X	X		O2	X	X		**JTAG clock input(6)**	Port 1.18	
20	H3	13	F4	P1.17 / JTDO	I/O	T_T	X	X		O8	X	X		**JTAG data output(6)**	Port 1.17	
21	H2	14	F3	P1.16 / JTDI	I/O	T_T	X	X		O2	X	X		**JTAG data input(6)**	Port 1.16	
22	G1	15	F2	NJTRST	I	T_T								JTAG reset input(5)		
23	G4			P2.01	I/O	T_T	**X**	X		O2	X	X		**Port 2.01**		
24	G5			P2.00	I/O	T_T	**X**	X		O2	X	X		**Port 2.00**		
25	H1	16	F1	P0.13 / RTCK / UART0_RTS UART2_TX	I/O	T_T	X	X		O8	X	X		**JTAG return clock output(6)**	Port 0.13 / UART0: Ready To Send output(4)	UART2: Transmit Data output (when remapped)(8)

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
68	A10			P1.02 / TIM2_OC2	I/O	T_T	X	X		O2	X	X		**Port 1.02**	TIM2: Output compare 2 (remappable to P0.06)(8)	
69	D7	44	C6	VDD_IO	S									Supply Voltage for digital I/Os		
70	D8	45	D6	VDDA_ADC	S									Supply Voltage for A/D converter		
71	C9			P2.11	I/O	T_T	X	X		O2	X	X		**Port 2.11**		
72	B10			P2.10	I/O	T_T	X	X		O2	X	X		**Port 2.10**		
73	C8	46	D7	VSSA_ADC	S									Ground Voltage for A/D converter		
74	C7	47	C7	VSS_IO	S									Ground Voltage for digital I/Os		
75	E8	48	D5	VREG_DIS	I	T_T								Voltage Regulator Disable input		
76	A9	49	A8	P0.07 / SMI_DOUT / SSP0_MOSI	I/O	T_T	X	X	EIT2	O4	X	X		**Port 0.07**	Serial Memory Interface: data output	SSP0: Master out Slave in data
77	A8	50	A7	P0.06 / SMI_DIN / SSP0_MISO	I/O	T_T	X	X		O4	X	X		**Port 0.06**	Serial Memory Interface: data input	SSP0: Master in Slave out data
78	A7	51	A6	P0.05 / SSP0_SCLK / SMI_CK	I/O	T_T	X	X	EIT1	O4	X	X		**Port 0.05**	SSP0: Serial clock	Serial Memory Interface: Serial clock output
79	B7	52	B6	P0.04 / SMI_CS0 / SSP0_NSS	I/O	T_T	X	X		O4	X	X		**Port 0.04**	Serial Memory Interface: chip select output 0	SSP0: Slave select input
80	C5	53	B7	P1.10 PWM_EMERGENCY	I/O	T_T	X	X	EIT10	O2	X	X		**Port 1.10**	PWM: Emergency input	
81	B6	54	B5	P1.09 / PWM1	I/O	T_T	X	X	EIT9	O4	X	X		**Port 1.09**	PWM: PWM1 output	
82	C6			P2.09 / PWM1N	I/O	T_T	X	X		O2	X	X		**Port 2.09**	PWM: PWM1 complementary output(4)	
83	G7			P2.08 / PWM2	I/O	T_T	X	X		O2	X	X		**Port 2.08**	PWM: PWM2 output(4)	
84	G6			P2.07 / PWM2N	I/O	T_T	X	X		O2	X	X		**Port 2.07**	PWM: PWM2 complementary output(4)	
85	F7			P2.06 / PWM3	I/O	T_T	X	X		O2	X	X		**Port 2.06**	PWM: PWM3 output(4)	
86	F6			P2.05 / PWM3N	I/O	T_T	X	X		O2	X	X		**Port 2.05**	PWM: PWM3 complementary output(4)	
87	A6	55	A5	P1.08 / PWM1N / ADC_IN11	I/O	T_T	X	X		O4	X	X		**Port 1.08**	PWM: PWM1 complementary output(8)	ADC: analog input 11
88	B5	56	B4	P1.07 / PWM2	I/O	T_T	X	X	EIT8	O4	X	X		**Port 1.07**	PWM: PWM2 output(4)	
89	A5	57	A4	P1.06 / PWM2N / ADC_IN10	I/O	T_T	X	X		O4	X	X		**Port 1.06**	PWM: PWM2 complementary output(4)	ADC: analog input 10
90	B4	58	B3	P1.05 / PWM3	I/O	T_T	X	X	EIT7	O4	X	X		**Port 1.05**	PWM: PWM3 output(4)	

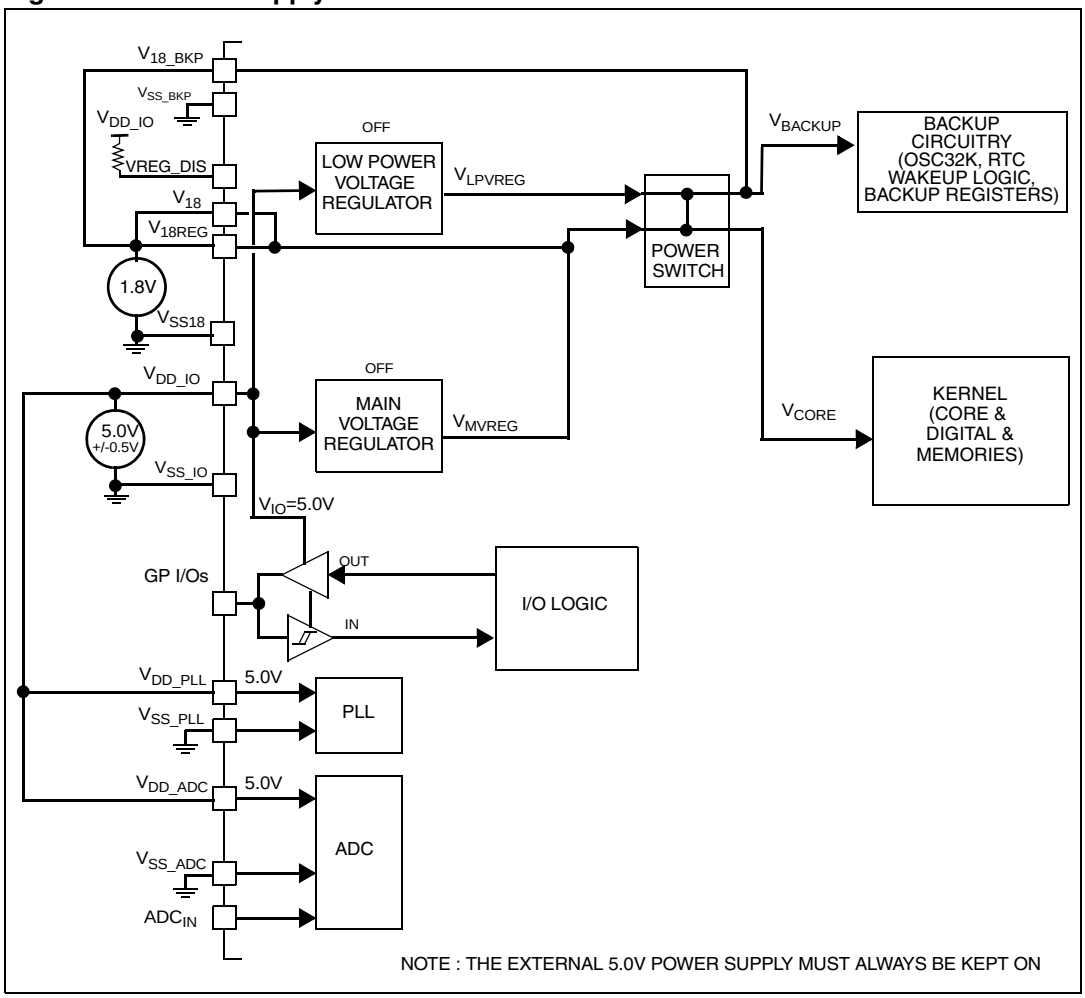
Power supply scheme 3: Single external 5 V power source

Figure 10. Power supply scheme 3



Power supply scheme 4: Dual external 1.8 V and 5.0 V supply

Figure 11. Power supply scheme 4



6.1.7 I/O characteristics versus the various power schemes (3.3V or 5.0V)

Unless otherwise mentioned, all the I/O characteristics are valid for both

- V_{DD_IO}=3.0 V to 3.6 V with bit EN33=1
- V_{DD_IO}=4.5 V to 5.5 V with bit EN33=0

When V_{DD_IO}=3.0 V to 3.6 V, I/Os are not 5V tolerant.

6.1.8 Current consumption measurements

All the current consumption measurements mentioned below refer to Power scheme 1 and 2 as described in *Figure 12* and *Figure 13*

Figure 14. Power consumption measurements in power scheme 3 (regulators enabled)

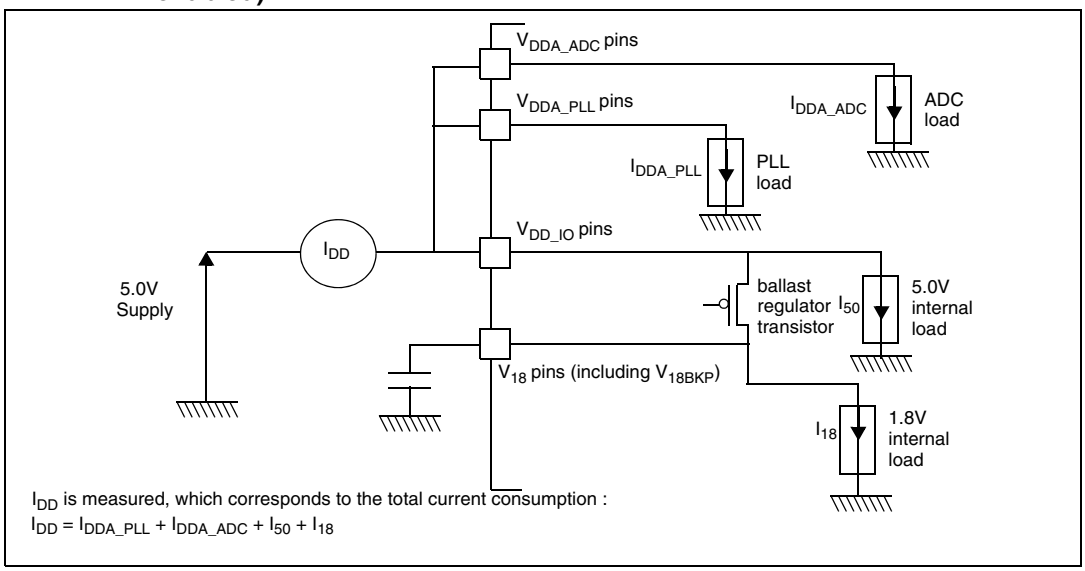
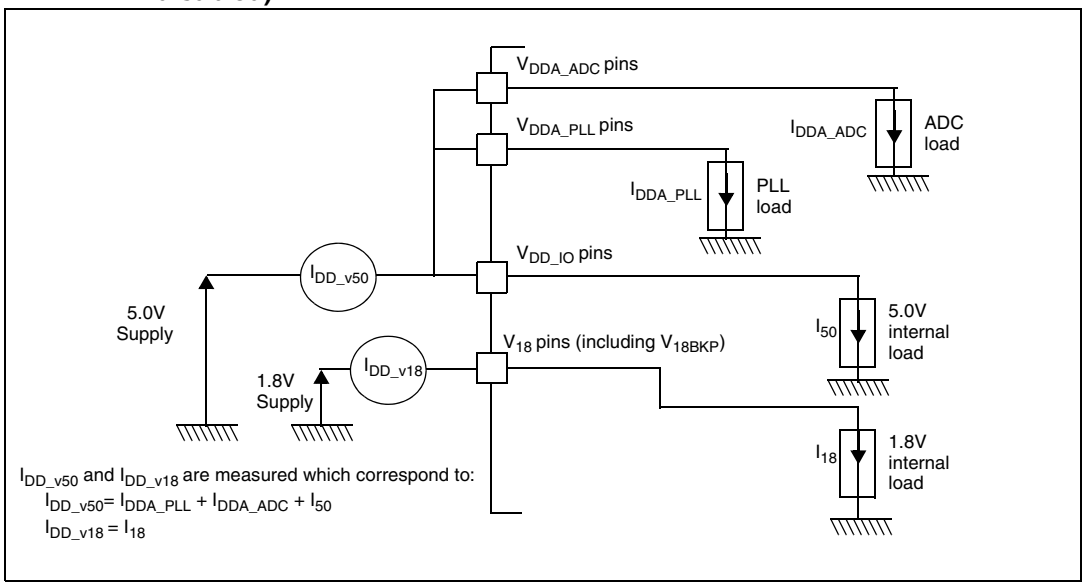


Figure 15. Power consumption measurements in power scheme 4 (regulators disabled)



On-Chip peripheral power consumption

Conditions:

- V_{DD_IO}=V_{DDA_ADC}=V_{DDA_PLL}=3.3 V or 5 V ±10% unless otherwise specified.
- T_A= 25° C
- Clocked by OSC4M with PLL multiplication, f_{CK_SYS}=64 MHz, f_{HCLK}=32 MHz, f_{PCLK}=32 MHz

Table 19. On-Chip peripherals

Symbol	Parameter	Typ (3.3V and 5.0V)	Unit
$I_{DD(TIM)}$	TIM Timer supply current (1)	0.7	mA
$I_{DD(PWM)}$	PWM Timer supply current(2)	1	
$I_{DD(SSP)}$	SSP supply current (3)	1.3	
$I_{DD(UART)}$	UART supply current (4)	1.6	
$I_{DD(I2C)}$	I2C supply current (5)	0.3	
$I_{DD(ADC)}$	ADC supply current when converting (6)	1.2	
$I_{DD(USB)}$	USB supply current (7) **Note:** V_{DD_IO} must be 3.3 V ±10%	0.90	
$I_{DD(CAN)}$	CAN supply current (8)	2.8	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 32 MHz. No IC/OC programmed (no I/O pads toggling)
2. Data based on a differential I_{DD} measurement between reset configuration and PWM running at 32 MHz. This measurement does not include PWM pads toggling consumption.
3. Data based on a differential I_{DD} measurement between reset configuration and permanent SPI master communication at maximum speed 16 MHz. The data sent is 55h. This measurement does not include the pad toggling consumption.
4. Data based on a differential I_{DD} measurement between reset configuration and a permanent UART data transmit sequence at 1Mbauds. This measurement does not include the pad toggling consumption.
5. Data based on a differential I_{DD} measurement between reset configuration (I2C disabled) and a permanent I2C master communication at 100kHz (data sent equal to 55h). This measurement includes the pad toggling consumption but not the external 10kOhm external pull-up on clock and data lines.
6. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions at 8 MHz in scan mode on 16 inputs configured as AIN.
7. Data based on a differential I_{DD} measurement between reset configuration and a running generic HID application.
8. Data based on a differential IDD measurement between reset configuration (CAN disabled) and a permanent CAN data transmit sequence in loopback mode at 1MHz. This measurement does not include the pad toggling consumption.

difference between N+1 consecutive clock rising edges and T_{min} is the minimum time difference between N+1 consecutive clock rising edges.

N should be kept sufficiently large to have a long term jitter (ex: thousands).

For N=1, this becomes the single period jitter.

See *Figure 23*

- Cycle-to-cycle jitter (N period jitter)

  This corresponds to the time variation between adjacent cycles over a random sample of adjacent clock cycles pairs. Jitter(cycle-to-cycle) = Max(Tcycle n- Tcycle n-1) for n=1 to N.

  See *Figure 24*

Figure 23. Self-referred jitter (single and long term)

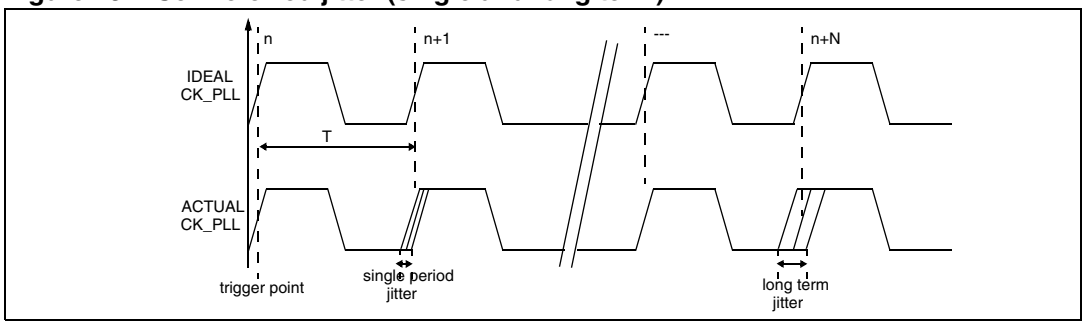
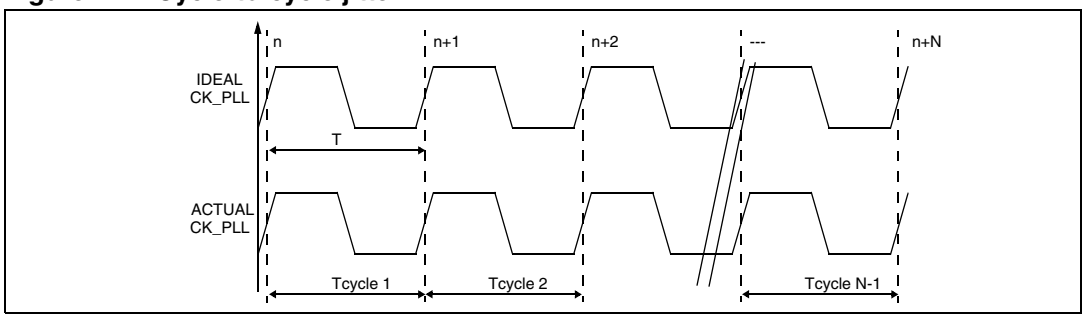


Figure 24. Cycle-to-cycle jitter



6.3.6 Memory characteristics

Flash memory

Subject to general operating conditions for V_{DD_IO} and V_{18}, T_A = -40 to 105 °C unless otherwise specified.

Table 26. Flash memory characteristics

Symbol	Parameter	Test Conditions	Value		Unit
			Typ	Max(1)	
t_{PW}	Word Program		35		µs
t_{PDW}	Double Word Program		60		µs
t_{PB0}	Bank 0 Program (256K)	Single Word programming of a checker-board pattern	2	4.9(2)	s
t_{PB1}	Bank 1 Program (16K)	Single Word programming of a checker-board pattern	125	224(2)	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed (all 1) Preprogrammed (all 0)	1.54 1.176	2.94(2) 2.38(2)	s
t_{ES}	Sector Erase (8K)	Not preprogrammed (all 1) Preprogrammed (all 0)	392 343	560(2) 532(2)	ms
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed (all 1) Preprogrammed (all 0)	8.0 6.6	13.7 11.2	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed (all 1) Preprogrammed (all 0)	0.9 0.8	1.5 1.3	s
t_{RPD}	Recovery when disabled			20	µs
t_{PSL}	Program Suspend Latency			10	µs
t_{ESL}	Erase Suspend Latency			300	µs

1. Data based on characterisation not tested in production
2. 10K program/erase cycles.

Table 27. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END_B0}	Endurance (Bank 0 sectors)		10			kcycles
N_{END_B1}	Endurance (Bank 1 sectors)		100			kcycles
Y_{RET}	Data Retention	T_A=85° C	20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

1. Data based on characterisation not tested in production.

6.3.7 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electro magnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behaviour is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 28. EMC characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-2	Class A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-4	Class A

Static and dynamic latch-up

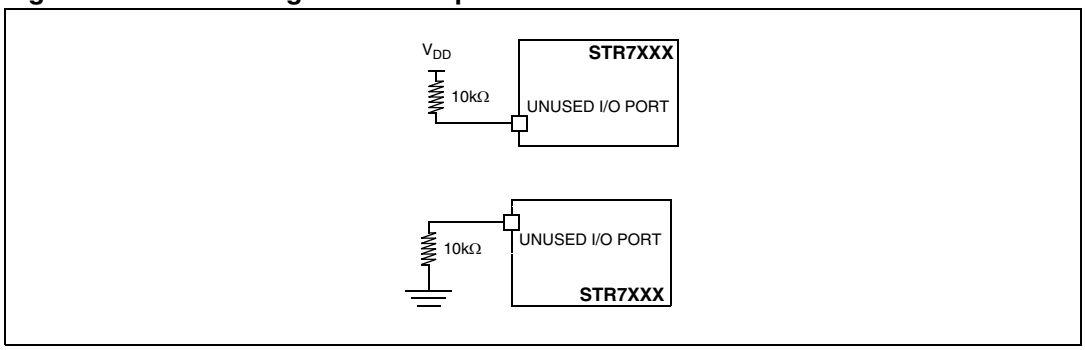
- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 31. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A=+25° C T_A=+85° C T_A=+105° C	Class A
DLU	Dynamic latch-up class	V_{DD}= 5.5 V, f_{OSC4M}=4 MHz, f_{CK_SYS}=32 MHz, T_A=+25° C	Class A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

Figure 25. Connecting unused I/O pins



Output driving current

The GP I/Os have different drive capabilities:

- O2 outputs can sink or source up to +/-2 mA.
- O4 outputs can sink or source up to +/-4 mA.
- outputs can sink or source up to +/-8 mA or can sink +20 mA (with a relaxed V_{OL}).

In the application, the user must limit the number of I/O pins which can drive current to respect the absolute maximum rating specified in *Section 6.2.2* :

- The sum of the current sourced by all the I/Os on $V_{DD\_IO,}$ plus the maximum RUN consumption of the MCU sourced on $V_{DD\_IO,}$ can not exceed the absolute maximum rating IV_{DD_IO}.
- The sum of the current sunk by all the I/Os on V_{SS_IO} plus the maximum RUN consumption of the MCU sunk on V_{SS_IO} can not exceed the absolute maximum rating IV_{SS_IO}.

Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

Table 33. Output driving current

I/O Output drive characteristics for V_{DD_IO} = 3.0 to 3.6 V and EN33 bit =1 or V_{DD_IO} = 4.5 to 5.5 V and EN33 bit =0						
I/O Type	**Symbol**	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
O2	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+2 mA		0.4	V
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-2 mA	V_{DD_IO}-0.8		
O4	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+4 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-4 mA	V_{DD_IO}-0.8		
O8	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+8 mA		0.4	
		Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time	I_{IO}=+20 mA, $T_A \leq 85°C$ $T_A \geq 85°C$		1.3 1.5	
			I_{IO}=+8 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-8 mA	V_{DD_IO}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS_IO}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD_IO}.

Table 37. PWM Timer (PWM)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(PWM)}$	PWM resolution time	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
		$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	16.6(1)			ns
Res_{PWM}	PWM resolution				16	bit
V_{OS}(1)	PWM/DAC output step voltage	V_{DD_IO}=3.3 V, Res=16-bits		50(1)		µV
		V_{DD_IO}=5.0 V, Res=16-bits		76(1)		µV
$t_{COUNTER}$	Timer clock period when internal clock is selected		1		65536	t_{CK_TIM}
		f_{CK_TIM}=60 MHz	0.0166		1087	µs
t_{MAX_COUNT}	Maximum Possible Count				65536x 65536	t_{CK_TIM}
		$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s

1. Take into account the frequency limitation due to the I/O speed capability when outputting the PWM to an I/O pin, as described in *: Output speed on page 57*.

Figure 31. TI configuration - master mode, single transfer

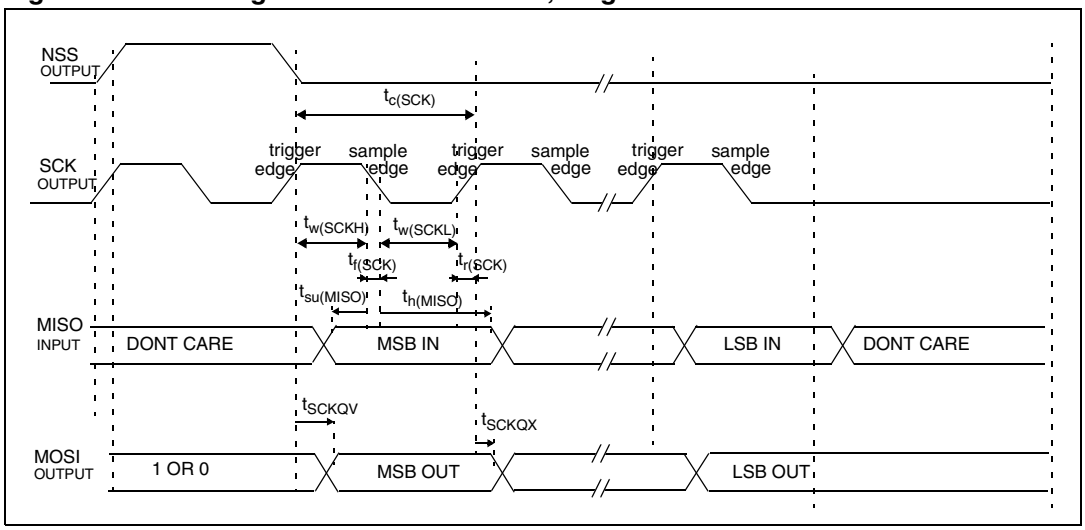
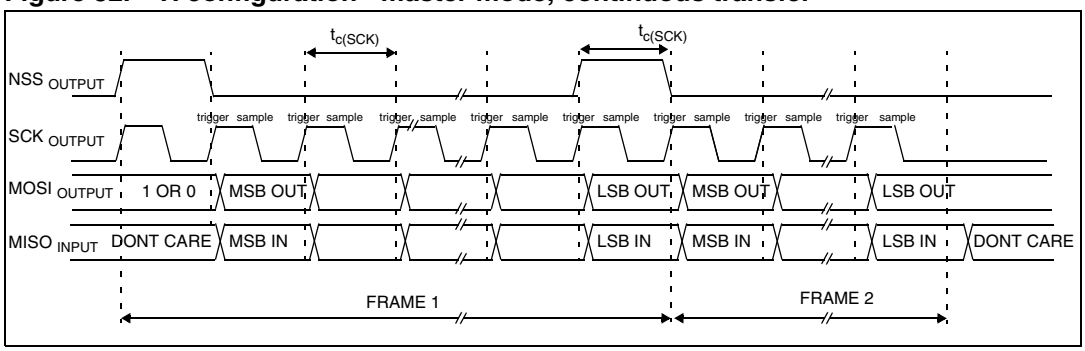


Figure 32. TI configuration - master mode, continuous transfer



SMI - serial memory interface

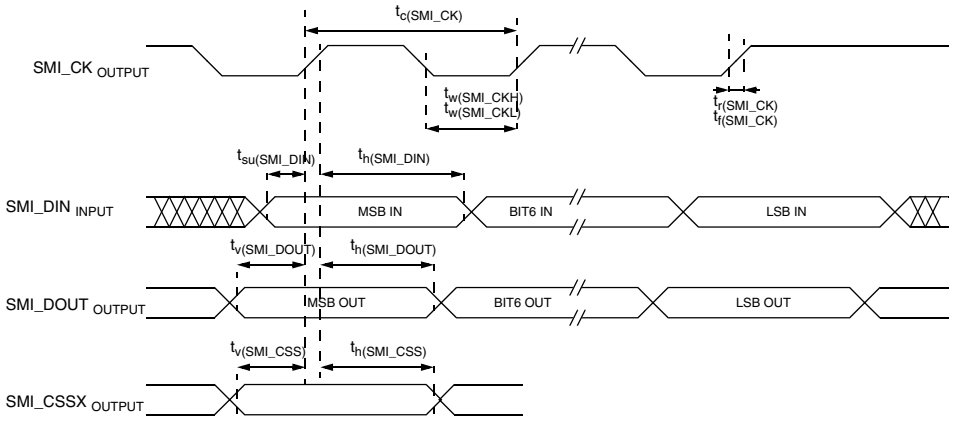
Subject to general operating conditions with $C_L \approx 30$ pF.

Table 40. SMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
f_{SMI_CK}	SMI clock frequency		32(2)(3)	MHz
			48(4)	
$t_{r(SMI\_CK)}$	SMI clock rise time		10	ns
$t_{f(SMI\_CK)}$	SMI clock fall time		8	
$t_{v(SMI\_DOUT)}$	Data output valid time		10	
$t_{h(SMI\_DOUT)}$	Data output hold time		0	
$t_{v(SMI\_CSSx)}$	CSS output valid time		10	
$t_{h(SMI\_CSSx)}$	CSS output hold time		0	
$t_{su(SMI\_DIN)}$	Data input setup time	0		
$t_{h(SMI\_DIN)}$	Data input hold time	5		

1. Data based on characterisation results, not tested in production.
2. Max. frequency = $f_{PCLK}/2 = 64/2 = 32$ MHz.
3. Valid for all temperature ranges: -40 to 105 °C, with 30 pF load capacitance.
4. Valid up to 60 °C, with 10 pF load capacitance.

Figure 39. SMI timing diagram



I²C - Inter IC control interface

Subject to general operating conditions for V_{DD_IO}, f_{PCLK}, and T_A unless otherwise specified.

The I²C interface meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Restriction: The I/O pins which SDA and SCL are mapped to are not “True” Open-Drain: when configured as open-drain, the PMOS connected between the I/O pin and V_{DD_IO} is disabled, but it is still present. Also, there is a protection diode between the I/O pin and V_{DD_IO}. Consequently, when using this I²C in a multi-master network, it is

General PCB design guidelines

To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 µF and optionally, if needed 10 pF capacitors as close as possible to the STR7 power supply pins and a 1 to 10 µF capacitor close to the power source (see *Figure 43*).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{DDA_ADC} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs near the A/D input being converted.

Software filtering of spurious conversion results

For EMC performance reasons, it is recommended to filter A/D conversion outliers using software filtering techniques.

Figure 43. Power supply filtering

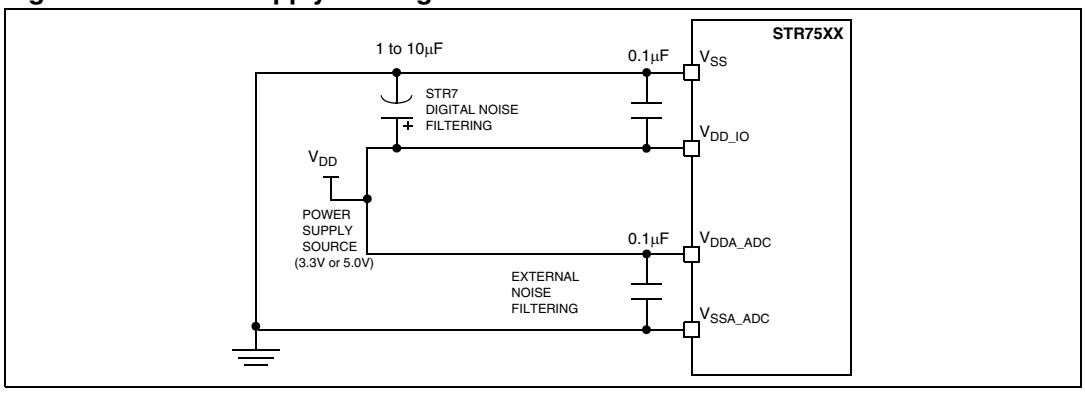


Table 49. Order codes (continued)

Order code	Flash Prog. Memory (Bank 0) Kbytes	Package	CAN Periph	USB Periph	Nominal Temp. Range (T_A)
STR755FV0T6	64	LQFP100 14x14	-	-	-40 to +85°C
STR755FV1T6	128				
STR755FV2T6	256				
STR755FV0H6	64	LFBGA100 10x10			
STR755FV1H6	128				
STR755FV2H6	256				