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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM7® |
| Core Size | 32-Bit Single-Core |
| Speed | 60MHz |
| Connectivity | CANbus, I²C, SPI, SSI, SSP, UART/USART, USB |
| Peripherals | DMA, PWM, WDT |
| Number of I/O | 72 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/str750fv1t6 |

### Serial memory interface (SMI)

The Serial Memory interface is directly able to access up to 4 serial FLASH devices. It can be used to access data, execute code directly or boot the application from external memory. The memory is addressed as 4 banks of up to 16 Mbytes each.

### Clocks and start-up

After RESET or when exiting from Low Power Mode, the CPU is clocked immediately by an internal RC oscillator (FREEOSC) at a frequency centered around 5 MHz, so the application code can start executing without delay. In parallel, the 4/8 MHz Oscillator is enabled and its stabilization time is monitored using a dedicated counter.

An oscillator failure detection is implemented: when the clock disappears on the XT1 pin, the circuit automatically switches to the FREEOSC oscillator and an interrupt is generated.

In Run mode, the AHB and APB clock speeds can be set at a large number of different frequencies thanks to the PLL and various prescalers: up to 60 MHz for AHB and up to 32 MHz for APB when fetching from Flash (64 MHz and 32 MHz when fetching from SRAM).

In SLOW mode, the AHB clock can be significantly decreased to reduce power consumption.

The built-in Clock Controller also provides the 48 MHz USB clock directly without any extra oscillators or PLL. For instance, starting from the 4 MHz crystal source, it is possible to obtain in parallel 60 MHz for the AHB clock, 48 MHz for the USB clock and 30 MHz for the APB peripherals.

### Boot modes

At start-up, boot pins are used to select one of five boot options:

- Boot from internal flash
- Boot from external serial Flash memory
- Boot from internal boot loader
- Boot from internal SRAM

Booting from SMI memory allows booting from a serial flash. This way, a specific boot monitor can be implemented. Alternatively, the STR750F can boot from the internal boot loader that implements a boot from UART.

### Power supply schemes

You can connect the device in any of the following ways depending on your application.

- **Power Scheme 1: Single external 3.3V power source**. In this configuration the $V_{CORE}$ supply required for the internal logic is generated internally by the main voltage regulator and the $V_{BACKUP}$ supply is generated internally by the low power voltage regulator. This scheme has the advantage of requiring only one 3.3V power source.
- **Power Scheme 2: Dual external 3.3V and 1.8V power sources.** In this configuration, the internal voltage regulators are switched off by forcing the VREG_DIS pin to high level. $V_{CORE}$ is provided externally through the $V_{18}$ and $V_{18REG}$ power pins and $V_{BACKUP}$ through the $V_{18\_BKP}$ pin. This scheme is intended to save power consumption for applications which already provide an 1.8V power supply.
- **Power Scheme 3: Single external 5.0V power source.** In this configuration the $V_{CORE}$ supply required for the internal logic is generated internally by the main voltage

periodic interrupt. It is clocked by an external 32.768 kHz oscillator or the internal low power RC oscillator. The RC has a typical frequency of 300 kHz and can be calibrated.

### WDG (watchdog timer)

The watchdog timer is based on a 16-bit downcounter and 8-bit prescaler. It can be used as watchdog to reset the device when a problem occurs, or as free running timer for application time out management.

### Timebase timer (TB)

The timebase timer is based on a 16-bit auto-reload counter and not connected to the I/O pins. It can be used for software triggering, or to implement the scheduler of a real-time operating system.

### Synchronizable standard timers (TIM2:0)

The three standard timers are based on a 16-bit auto-reload counter and feature up to 2 input captures and 2 output compares (for external triggering or time base / time out management). They can work together with the PWM timer via the Timer Link feature for synchronization or event chaining. In reset state, timer Alternate Function I/Os are connected to the same
I/O ports in both 64-pin and 100-pin devices. To optimize timer functions in 64-pin devices, timer Alternate Function I/Os can be connected, or “remapped”, to other I/O ports as summarized in *Table 3* and detailed in *Table 6*. This remapping is done by the application via a control register.

**Table 3. Standard timer alternate function I/Os**

| Standard timer functions | | Number of alternate function I/Os | | |
|---|---|---|---|---|
| | | 100-pin package | 64-pin package | |
| | | | Default mapping | Remapped |
| TIM 0 | Input Capture | 2 | 1 | 2 |
| | Output Compare/PWM | 2 | 1 | 2 |
| TIM 1 | Input Capture | 2 | 1 | 1 |
| | Output Compare/PWM | 2 | 1 | 1 |
| TIM 2 | Input Capture | 2 | 2 | 2 |
| | Output Compare/PWM | 2 | 1 | 2 |

Any of the standard timers can be used to generate PWM outputs. One timer (TIM0) is mapped to a DMA channel.

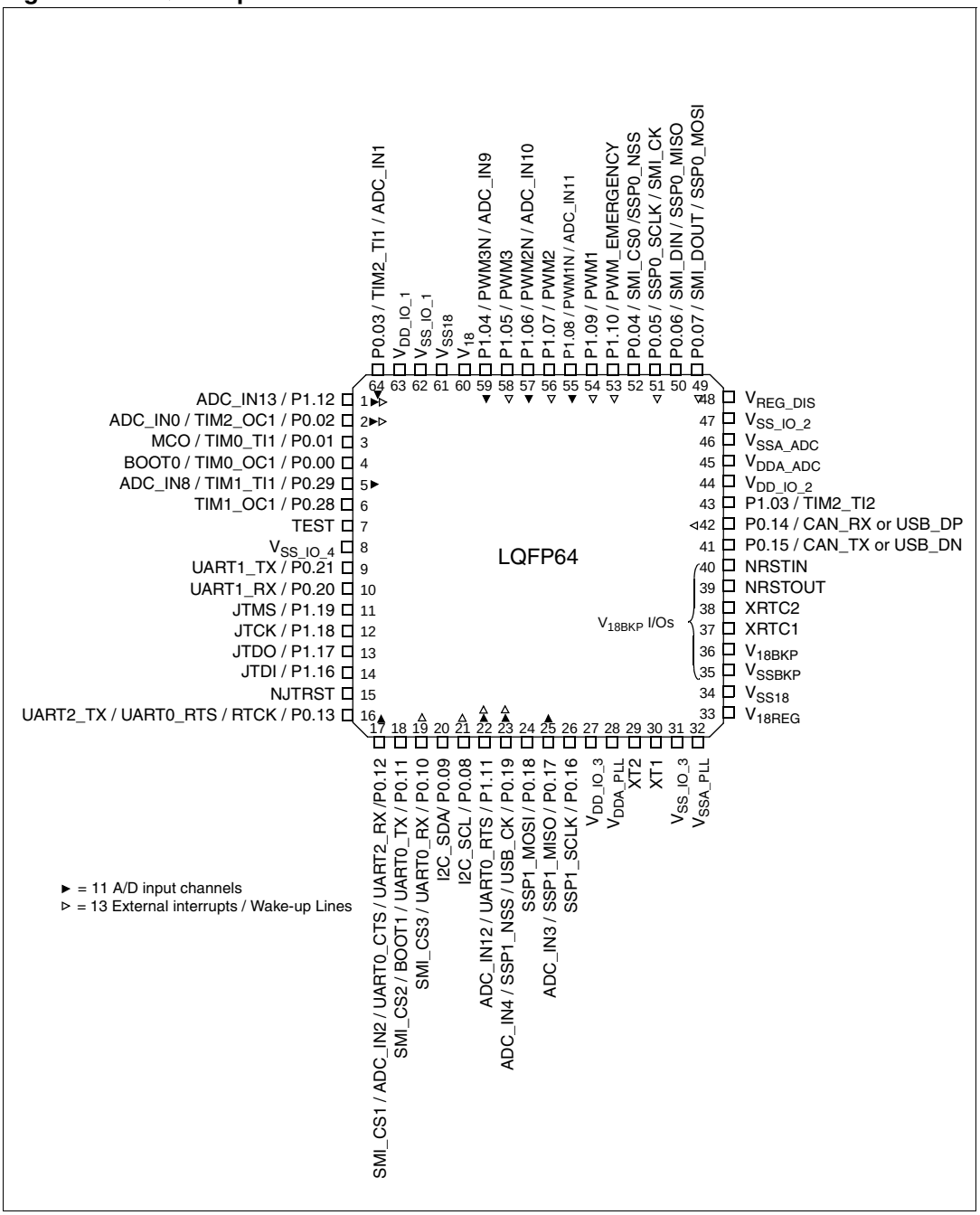
### Motor control PWM timer (PWM)

The Motor Control PWM Timer (PWM) can be seen as a three-phase PWM multiplexed on 6 channels. The 16-bit PWM generator has full modulation capability (0...100%), edge or centre-aligned patterns and supports dead-time insertion. It has many features in common with the standard TIM timers which has the same architecture and it can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.The PWM timer is mapped to a DMA channel.

### GPIOs (general purpose input/output)

Each of the 72 GPIO pins (38 GPIOs in 64-pin devices) can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as Peripheral Alternate Function. Port 1.15 is an exception, it can be used as general-purpose input only or wake-up from STANDBY mode (WKP_STDBY). Most of the GPIO pins are shared with digital or analog alternate functions.

**Figure 3. LQFP64 pinout**



## 4.1 Pin description table

**Legend / abbreviations for *Table 6*:**

| | |
|---|---|
| **Type:** | I = input, O = output, S = supply, |
| **Input levels:** | All Inputs are LVTTL at $V_{DD\_IO}$ = 3.3V+/-0.3V or TTL at $V_{DD\_IO}$ = 5V± 0.5V. In both cases, $T_T$ means $V_{ILmax}$ =0.8V $V_{IHmin}$=2.0V |
| **Inputs:** | All inputs can be configured as floating or with internal weak pull-up or pull down (pu/pd) |
| **Outputs:** | All Outputs can be configured as Open Drain (OD) or Push-Pull (PP) (see also note 6 below *Table 6*).<br>There are 3 different types of Output with different drives and speed characteristics:<br>– O8: $f_{max}$ = 40 MHz on $C_L$=50pF and 8 mA static drive capability for $V_{OL}$=0.4V and up to 20 mA for $V_{OL}$=1.3V (see*Output driving current on page 55*)<br>– O4: $f_{max}$ = 20 MHz on $C_L$=50pF and 4 mA static drive capability for $V_{OL}$=0.4V (see*Output driving current on page 55*)<br>– O2: $f_{max}$ = 10 MHz on $C_L$=50pF and 2 mA static drive capability of for $V_{OL}$=0.4V (see*Output driving current on page 55*) |
| **External interrupts/wake-up lines:** | EITx |

**Table 6. STR750F pin description (continued)**

| Pin n° | | | | Pin name | Type | Input | | | | Output | | | Usable in Standby | Main function (after reset) | Alternate function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100(1) | LFBGA100(1) | LQFP64(2) | LFBGA64(2) | | | Input Level | floating | pu/pd | Ext. int /Wake-up | Capability | OD (3) | PP | | | | |
| 7 | D1 | 5 | D1 | P0.29 / TIM1_TI1 / ADC_IN8 | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 0.29** | TIM1: Input Capture 1 | ADC: Analog input 8 |
| 8 | E1 | 6 | D2 | P0.28 / TIM1_OC1 | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 0.28** | TIM1: Output Compare 1 | |
| 9 | E5 | 7 | D3 | TEST | I | | | | | | | | | Reserved, must be tied to ground | | |
| 10 | E4 | 8 | D4 | VSS_IO | S | | | | | | | | | Ground Voltage for digital I/Os | | |
| 11 | E2 | | | P0.23 / UART1_RTS / ADC_IN6 | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 0.23** | UART1: Ready To Send output(4) | ADC analog input 6 |
| 12 | F5 | | | P2.04 / TIM2_OC1 | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 2.04** | TIM2: Output Compare 1(4) | |
| 13 | F1 | | | P2.03 / UART1_RTS | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 2.03** | UART1: Ready To Send output(4) | |
| 14 | F4 | | | P2.02 | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 2.02** | | |
| 15 | E3 | | | P0.22 / UART1_CTS / ADC_IN5 | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 0.22** | UART1: Clear To Send input | ADC: Analog input 5 |
| 16 | F2 | 9 | E4 | P0.21 / UART1_TX | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 0.21** | UART1: Transmit data output (remappable to P0.15)(4) | |
| 17 | F3 | 10 | E3 | P0.20 / UART1_RX | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 0.20** | UART1: Receive data input (remappable to P0.14)(4) | |
| 18 | G3 | 11 | E2 | P1.19 / JTMS | I/O | $T_T$ | X | X | | O2 | X | X | | **JTAG mode selection input(6)** | Port 1.19 | |
| 19 | G2 | 12 | E1 | P1.18 / JTCK | I/O | $T_T$ | X | X | | O2 | X | X | | **JTAG clock input(6)** | Port 1.18 | |
| 20 | H3 | 13 | F4 | P1.17 / JTDO | I/O | $T_T$ | X | X | | O8 | X | X | | **JTAG data output(6)** | Port 1.17 | |
| 21 | H2 | 14 | F3 | P1.16 / JTDI | I/O | $T_T$ | X | X | | O2 | X | X | | **JTAG data input(6)** | Port 1.16 | |
| 22 | G1 | 15 | F2 | NJTRST | I | $T_T$ | | | | | | | | JTAG reset input(5) | | |
| 23 | G4 | | | P2.01 | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 2.01** | | |
| 24 | G5 | | | P2.00 | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 2.00** | | |
| 25 | H1 | 16 | F1 | P0.13 / RTCK / UART0_RTS UART2_TX | I/O | $T_T$ | X | X | | O8 | X | X | | **JTAG return clock output(6)** | Port 0.13 / UART0: Ready To Send output(4) | UART2: Transmit Data output (when remapped)(8) |

**Table 6. STR750F pin description (continued)**

| Pin n° | | | | Pin name | Type | Input | | | | Output | | | Usable in Standby | Main function (after reset) | Alternate function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100(1) | LFBGA100(1) | LQFP64(2) | LFBGA64(2) | | | Input Level | floating | pu/pd | Ext. int /Wake-up | Capability | OD (3) | PP | | | | |
| 26 | J2 | 17 | G2 | P0.12 / UART2_RX / UART0_CTS / ADC_IN2 / SMI_CS1 | I/O | $T_T$ | X | X | | O4 | X | X | | **Port 0.12** | UART0: Clear To Send input | ADC: Analog input 2 |
| | | | | | | | | | | | | | | | Serial Memory Interface: chip select output 1 | UART2: Receive Data input (when remapped)(8) |
| 27 | J1 | 18 | G1 | P0.11 / UART0_TX / BOOT1 / SMI_CS2 | I/O | $T_T$ | X | X | | O4 | X | X | | **Port 0.11/Boot mode selection input 1** | UART0: Transmit data output | Serial Memory Interface: chip select output 2 |
| 28 | K1 | 19 | H1 | P0.10 / UART0_RX / SMI_CS3 | I/O | $T_T$ | X | X | EIT4 | O2 | X | X | | **Port 0.10** | UART0: Receive Data input | Serial Memory Interface: chip select output 3 |
| 29 | K2 | 20 | H2 | P0.09 / I2C_SDA | I/O | $T_T$ | X | X | | O4 | X | X | | **Port 0.09** | I2C: Serial Data | |
| 30 | K3 | 21 | H3 | P0.08 / I2C_SCL | I/O | $T_T$ | X | X | EIT3 | O4 | X | X | | **Port 0.08** | I2C: Serial clock | |
| 31 | H4 | | | P2.19 | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 2.19** | | |
| 32 | H5 | | | P2.18 | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 2.18** | | |
| 33 | H6 | | | P2.17 / UART2_RTS | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 2.17** | UART2: Ready To Send output(4) | |
| 34 | J3 | 22 | G3 | P1.11 /UART0_RTS ADC_IN12 | I/O | $T_T$ | X | X | EIT11 | O8 | X | X | | **Port 1.11** | UART0: Ready To Send output(4) | ADC: Analog input 12 |
| 35 | J4 | | | P0.27 / UART2_RTS / ADC_IN7 | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 0.27** | UART2: Ready To Send output(8) | ADC: Analog input 7 |
| 36 | J6 | | | P0.26 / UART2_CTS | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 0.26** | UART2: Clear To Send input | |
| 37 | J7 | | | P0.25 / UART2_TX | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 0.25** | UART2: Transmit data output (remappable to P0.13)(8) | |
| 38 | H7 | | | P0.24 / UART2_RX | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 0.24** | UART2: Receive data input (remappable to P0.12)(8) | |
| 39 | J5 | 23 | G4 | P0.19 / USB_CK / SSP1_NSS / ADC_IN4 | I/O | $T_T$ | X | X | EIT6 | O2 | X | X | | **Port 0.19** | SSP1: Slave select input (remappable to P0.11)(8) | ADC: Analog input 4 |
| | | | | | | | | | | | | | | | USB: 48 MHz Clock input | |
| 40 | K4 | 24 | H5 | P0.18 / SSP1_MOSI | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 0.18** | SSP1: Master out/slave in data (remappable to P0.10)(8) | |
| 41 | K5 | 25 | H4 | P0.17 / SSP1_MISO / ADC_IN3 | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 0.17** | SSP1: Master in/slave out data (remappable to P0.09)(8) | ADC: Analog input 3 |
| 42 | K6 | 26 | H6 | P0.16 / SSP1_SCLK | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 0.16** | SSP1: serial clock (remappable to P0.08)(8) | |

**Table 6. STR750F pin description (continued)**

| Pin n° | | | | Pin name | Type | Input | | | | Output | | | Usable in Standby | Main function (after reset) | Alternate function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100(1) | LFBGA100(1) | LQFP64(2) | LFBGA64(2) | | | Input Level | floating | pu/pd | Ext. int /Wake-up | Capability | OD (3) | PP | | | | |
| 68 | A10 | | | P1.02 / TIM2_OC2 | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 1.02** | TIM2: Output compare 2 (remappable to P0.06)(8) | |
| 69 | D7 | 44 | C6 | VDD_IO | S | | | | | | | | | Supply Voltage for digital I/Os | | |
| 70 | D8 | 45 | D6 | VDDA_ADC | S | | | | | | | | | Supply Voltage for A/D converter | | |
| 71 | C9 | | | P2.11 | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 2.11** | | |
| 72 | B10 | | | P2.10 | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 2.10** | | |
| 73 | C8 | 46 | D7 | VSSA_ADC | S | | | | | | | | | Ground Voltage for A/D converter | | |
| 74 | C7 | 47 | C7 | VSS_IO | S | | | | | | | | | Ground Voltage for digital I/Os | | |
| 75 | E8 | 48 | D5 | VREG_DIS | I | $T_T$ | | | | | | | | Voltage Regulator Disable input | | |
| 76 | A9 | 49 | A8 | P0.07 / SMI_DOUT / SSP0_MOSI | I/O | $T_T$ | X | X | EIT2 | O4 | X | X | | **Port 0.07** | Serial Memory Interface: data output | SSP0: Master out Slave in data |
| 77 | A8 | 50 | A7 | P0.06 / SMI_DIN / SSP0_MISO | I/O | $T_T$ | X | X | | O4 | X | X | | **Port 0.06** | Serial Memory Interface: data input | SSP0: Master in Slave out data |
| 78 | A7 | 51 | A6 | P0.05 / SSP0_SCLK / SMI_CK | I/O | $T_T$ | X | X | EIT1 | O4 | X | X | | **Port 0.05** | SSP0: Serial clock | Serial Memory Interface: Serial clock output |
| 79 | B7 | 52 | B6 | P0.04 / SMI_CS0 / SSP0_NSS | I/O | $T_T$ | X | X | | O4 | X | X | | **Port 0.04** | Serial Memory Interface: chip select output 0 | SSP0: Slave select input |
| 80 | C5 | 53 | B7 | P1.10 PWM_EMERGENCY | I/O | $T_T$ | X | X | EIT10 | O2 | X | X | | **Port 1.10** | PWM: Emergency input | |
| 81 | B6 | 54 | B5 | P1.09 / PWM1 | I/O | $T_T$ | X | X | EIT9 | O4 | X | X | | **Port 1.09** | PWM: PWM1 output | |
| 82 | C6 | | | P2.09 / PWM1N | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 2.09** | PWM: PWM1 complementary output(4) | |
| 83 | G7 | | | P2.08 / PWM2 | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 2.08** | PWM: PWM2 output(4) | |
| 84 | G6 | | | P2.07 / PWM2N | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 2.07** | PWM: PWM2 complementary output(4) | |
| 85 | F7 | | | P2.06 / PWM3 | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 2.06** | PWM: PWM3 output(4) | |
| 86 | F6 | | | P2.05 / PWM3N | I/O | $T_T$ | X | X | | O2 | X | X | | **Port 2.05** | PWM: PWM3 complementary output(4) | |
| 87 | A6 | 55 | A5 | P1.08 / PWM1N / ADC_IN11 | I/O | $T_T$ | X | X | | O4 | X | X | | **Port 1.08** | PWM: PWM1 complementary output(8) | ADC: analog input 11 |
| 88 | B5 | 56 | B4 | P1.07 / PWM2 | I/O | $T_T$ | X | X | EIT8 | O4 | X | X | | **Port 1.07** | PWM: PWM2 output(4) | |
| 89 | A5 | 57 | A4 | P1.06 / PWM2N / ADC_IN10 | I/O | $T_T$ | X | X | | O4 | X | X | | **Port 1.06** | PWM: PWM2 complementary output(4) | ADC: analog input 10 |
| 90 | B4 | 58 | B3 | P1.05 / PWM3 | I/O | $T_T$ | X | X | EIT7 | O4 | X | X | | **Port 1.05** | PWM: PWM3 output(4) | |

# 6 Electrical parameters

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referred to $V_{SS}$.

### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$max (given by the selected temperature range).

Data based on product characterisation, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$=25° C, $V_{DD\_IO}$=3.3 V (for the 3.0 V≤$V_{DD\_IO}$≤3.6 V voltage range) and $V_{18}$=1.8 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

## Power supply scheme 3: Single external 5 V power source

**Figure 10. Power supply scheme 3**

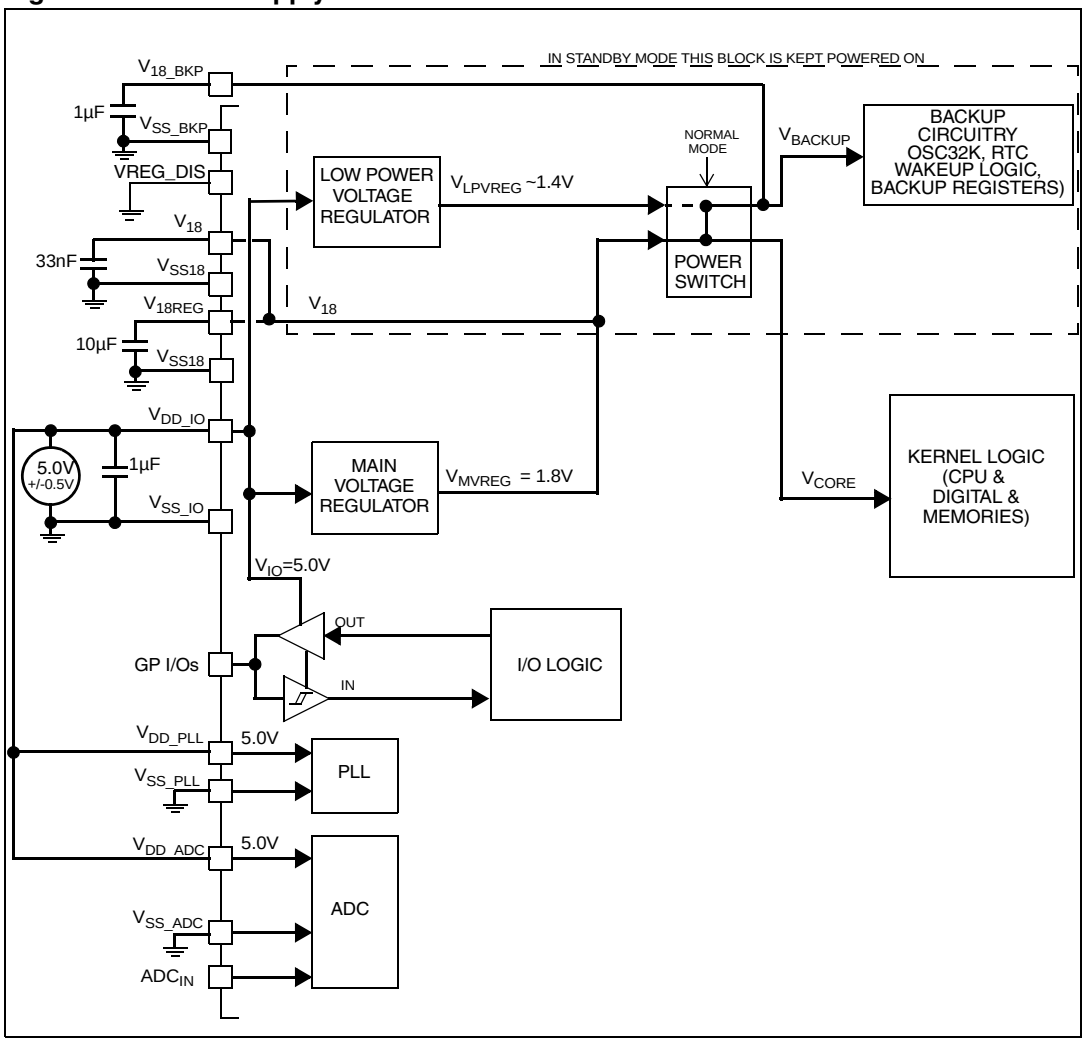


**Table 14. Maximum power consumption in STOP and STANDBY modes**

| Symbol | Parameter | Conditions[1] | | Typ[2] | Max[3] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ 25°C | $T_A$ 85°C | $T_A$ 105°C | |
| $I_{DD}$ | Supply current in STOP mode | LP_PARAM bits: ALL OFF[4] Single supply scheme see *Figure 12*. | 3.3V range | 12 | 16 | 117 | 250 | µA |
| | | LP_PARAM bits: ALL OFF Dual supply scheme see *Figure 13*. | $I_{DD\_V18}$<br>$I_{DD\_V33}$ | 5<br><1 | 8<br>3 | 60<br>20 | 110<br>26 | µA |
| | | LP_PARAM bits: ALL OFF[4] Single supply scheme see *Figure 10* | 5V range | 15 | 22 | 160 | 310 | µA |
| | | LP_PARAM bits: ALL OFF Dual supply scheme see *Figure 11* | $I_{DD\_V18}$<br>$I_{DD\_V50}$ | 5<br>3 | 8<br>6 | 60<br>50 | 110<br>65 | µA |
| | Supply current in STANDBY mode | RTC OFF | 3.3 V range | 10 | 20 | 25 | 28 | |
| | | | 5V range | 15 | 25 | 30 | 33 | |

1. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4*.
2. Typical data are based on $T_A$=25°C, $V_{DD\_IO}$=3.3V or 5.0V and $V_{18}$=1.8V unless otherwise specified.
3. Data based on product characterisation, tested in production at $V_{DD\_IO}$ max and $V_{18}$ max (1.95V in dual supply mode or regulator output value in single supply mode).
4. In this mode, the whole digital circuitry is powered internally by the LPVREG at approximately 1.4V, which significantly reduces the leakage currents.

### Typical power consumption

The following measurement conditions apply to *Table 15*, *Table 16* and *Table 17*.

In RUN mode:

- Program is executed from Flash (except if especially mentioned). The program consists of an infinite loop. When $f_{HCLK}$ > 32 MHz, burst mode is activated.
- A standard 4 MHz crystal source is used.
- In all cases the PLL is used to multiply the frequency.
- All measurements are done in the single supply scheme with internal regulators used (see *Figure 12*)

In WFI Mode:

- In WFI Mode the measurement conditions are similar to RUN mode (OSC4M and PLL enabled). In addition, the Flash can be disabled depending on burst mode activation:
  - For AHB frequencies greater than 32 MHz, burst mode is activated and the Flash is kept enabled by setting the WFI_FLASH_EN bit (this bit cannot be reset when burst mode is activated).
  - For AHB frequencies less than or equal to 32 MHz, burst mode is deactivated, WFI_FLASH_EN is reset and the LP_PARAM14 bit is set (Flash is disabled in WFI mode).

In SLOW mode:

- The same program as in RUN mode is executed from Flash. The CPU is clocked by the FREEOSC, OSC4M, LPOSC or OSC32K. Only EXTIT peripheral is enabled in the MRCC_PCLKEN register.

In SLOW-WFI mode:

- In SLOW-WFI, the measurement conditions are similar to SLOW mode (CPU clocked by a low frequency clock). In addition, the LP_PARAM14 bit is set (FLASH is OFF). The WFI routine itself is executed from SRAM (it is not allowed to execute a WFI from the internal FLASH)

In STOP mode:

- Several measurements are given: in the single supply scheme with internal regulators used (see *Figure 12*): and in the dual supply scheme (see *Figure 13*).

In STANDBY mode:

- Three measurements are given:
  - The RTC is disabled, only the consumption of the LPVREG and RSM remain (almost no leakage currents)
  - The RTC is running, clocked by a standard 32.768 kHz crystal.
  - The RTC is running, clocked by the internal Low Power RC oscillator (LPOSC)
- STANDBY mode is only supported in the single supply scheme (see *Figure 12*)

### Electro magnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

**Table 29. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored Frequency Band | Max vs. [$f_{OSC4M}/f_{HCLK}$] | | Unit |
|---|---|---|---|---|---|---|
| | | | | 4/32MHz | 4/60MHz | |
| $S_{EMI}$ | Peak level | Flash devices: $V_{DD\_IO}$=3.3 V or 5 V, $T_A$=+25° C, LQFP64 package conforming to SAE J 1752/3 | 0.1 MHz to 30 MHz | 22 | 26 | dBµV |
| | | | 30 MHz to 130 MHz | 31 | 26 | |
| | | | 130 MHz to 1 GHz | 19 | 23 | |
| | | | SAE EMI Level | >4 | >4 | - |

### Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

### Electro-Static discharge (ESD)

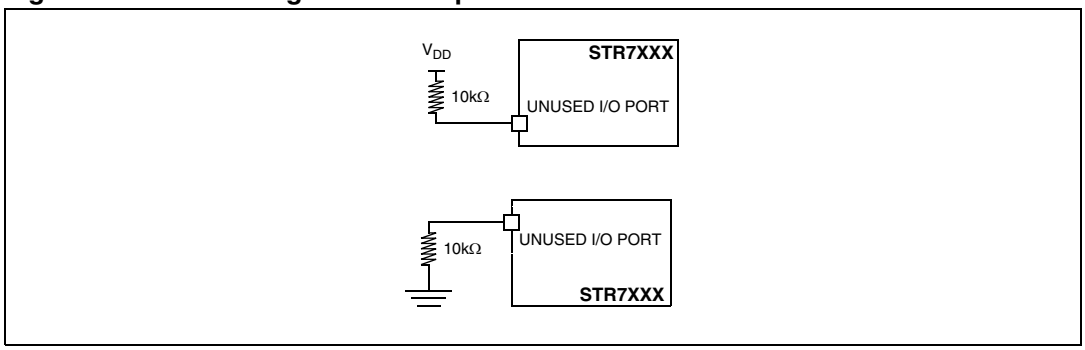
Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard.

**Table 30. Absolute maximum ratings**

| Symbol | Ratings | Conditions | Maximum value(1) | Unit |
|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electro-static discharge voltage (Human Body Model) | $T_A$=+25° C | 2000 | V |
| $V_{ESD(MM)}$ | Electro-static discharge voltage (Machine Model) | | 200 | |
| $V_{ESD(CDM)}$ | Electro-static discharge voltage (Charge Device Model) | | 750 | |

1. Data based on product characterisation, not tested in production.

**Figure 25. Connecting unused I/O pins**




### Output driving current

The GP I/Os have different drive capabilities:

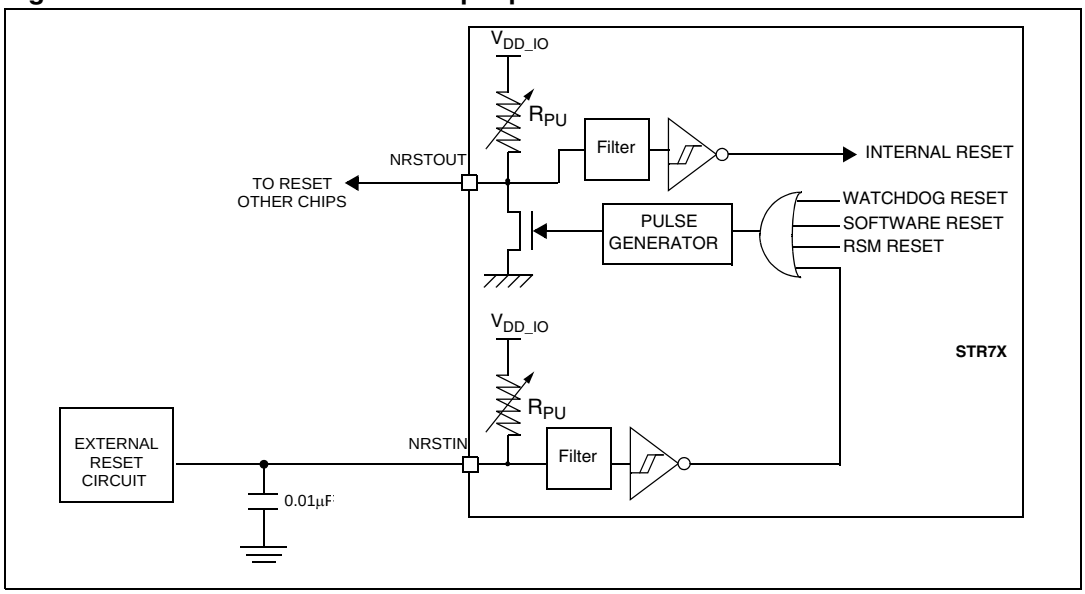
- O2 outputs can sink or source up to +/-2 mA.
- O4 outputs can sink or source up to +/-4 mA.
- outputs can sink or source up to +/-8 mA or can sink +20 mA (with a relaxed $V_{OL}$).

In the application, the user must limit the number of I/O pins which can drive current to respect the absolute maximum rating specified in *Section 6.2.2* :

- The sum of the current sourced by all the I/Os on $V_{DD\_IO,}$ plus the maximum RUN consumption of the MCU sourced on $V_{DD\_IO,}$ can not exceed the absolute maximum rating $IV_{DD\_IO}$.
- The sum of the current sunk by all the I/Os on $V_{SS\_IO}$ plus the maximum RUN consumption of the MCU sunk on $V_{SS\_IO}$ can not exceed the absolute maximum rating $IV_{SS\_IO}$.

Subject to general operating conditions for $V_{DD\_IO}$ and $T_A$ unless otherwise specified.

**Figure 27. Recommended NRSTIN pin protection**




1. The user must ensure that the level on the NRSTIN pin can go below the $V_{IL(NRSTIN)}$ max. level specified in *NRSTIN and NRSTOUT pins on page 58*. Otherwise the reset will not be taken into account internally.

### 6.3.9 TB and TIM timer characteristics

Subject to general operating conditions for $V_{DD\_IO}$, $f_{CK\_SYS}$, and $T_A$ unless otherwise specified.

Refer to *Section 6.3.8: I/O port pin characteristics on page 54* for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

**Table 36. TB and TIM timers**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{w(ICAP)in}$ | Input capture pulse time | TIM0,1,2 | | 2 | | | $t_{CK\_TIM}$ |
| $t_{res(TIM)}$ | Timer resolution time(1) | TB | $f_{CK\_TIM(MAX)} = f_{CK\_SYS}$ | 1 | | | $t_{CK\_TIM}$ |
| | | | $f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz | 16.6(1) | | | ns |
| | | TIM0,1,2 | $f_{CK\_TIM(MAX)} = f_{CK\_SYS}$ | 1 | | | $t_{CK\_TIM}$ |
| | | | $f_{CK\_TIM} = f_{CK\_SYS}$ = 60MHz | 16.6(1) | | | ns |
| $f_{EXT}$ | Timer external clock frequency on TI1 or TI2 | TIM0,1,2 | $f_{CK\_TIM(MAX)} = f_{CK\_SYS}$ | 0 | | $f_{CK\_TIM}/4$ | MHz |
| | | | $f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz | 0 | | 15 | MHz |
| $Res_{TIM}$ | Timer resolution | | | | | 16 | bit |
| $t_{COUNTER}$ | 16-bit Counter clock period when internal clock is selected (16-bit Prescaler) | TB | | 1 | | 65536 | $t_{CK\_TIM}$ |
| | | | $f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz | 0.0166 | | 1092 | µs |
| | | TIM0,1,2 | | 1 | | 65536 | $t_{CK\_TIM}$ |
| | | | $f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz | 0.0166 | | 1092 | µs |
| $t_{MAX\_COUNT}$ | Maximum Possible Count | TB | | | | 65536x65536 | $t_{CK\_TIM}$ |
| | | | $f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz | | | 71.58 | s |
| | | TIM0,1,2 | | | | 65536x65536 | $t_{CK\_TIM}$ |
| | | | $f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz | | | 71.58 | s |

1. Take into account the frequency limitation due to the I/O speed capability when outputting the PWM to I/O pin, described in *: Output speed on page 57*.

**Table 37. PWM Timer (PWM)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{res(PWM)}$ | PWM resolution time | $f_{CK\_TIM(MAX)} = f_{CK\_SYS}$ | 1 | | | $t_{CK\_TIM}$ |
| | | $f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz | 16.6(1) | | | ns |
| $Res_{PWM}$ | PWM resolution | | | | 16 | bit |
| $V_{OS}$(1) | PWM/DAC output step voltage | $V_{DD\_IO}$=3.3 V, Res=16-bits | | 50(1) | | µV |
| | | $V_{DD\_IO}$=5.0 V, Res=16-bits | | 76(1) | | µV |
| $t_{COUNTER}$ | Timer clock period when internal clock is selected | | 1 | | 65536 | $t_{CK\_TIM}$ |
| | | $f_{CK\_TIM}$=60 MHz | 0.0166 | | 1087 | µs |
| $t_{MAX\_COUNT}$ | Maximum Possible Count | | | | 65536x 65536 | $t_{CK\_TIM}$ |
| | | $f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz | | | 71.58 | s |

1. Take into account the frequency limitation due to the I/O speed capability when outputting the PWM to an I/O pin, as described in *: Output speed on page 57*.

## 6.3.10 Communication interface characteristics

### SSP synchronous serial peripheral in master mode (SPI or TI mode)

General operating conditions: $V_{33}$, 3.0V to 3.3V, V18 =1.8V, $C_L \approx 45$ pF.

**Table 38. SSP master mode characteristics(1)**

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SPI clock frequency(2) | | SSP0 | | 16 | MHz |
| | | | SSP1 | | 8 | |
| $t_{r(SCK)}$ | SPI clock rise time | | SSP0 | | 14 | ns |
| | | | SSP1 | | 33 | |
| $t_{f(SCK)}$ | SPI clock fall time | | SSP0 | | 11 | |
| | | | SSP1 | | 30 | |
| $t_{w(SCKH)}$ $t_{w(SCKL)}$ | SCK high and low time | | SSP0 | | 19 | |
| | | | SSP1 | | 30 | |
| $t_{NSSLQV}$ | NSS low to Data Output MOSI valid time | | SSP0 | | $0.5t_{SCK}$+15ns | |
| | | | SSP1 | | $0.5t_{SCK}$+30ns | |
| $t_{SCKNSSH}$ | SCK last edge to NSS high | CPHA = 0 | SSP0 | | $0.5t_{SCK}$+15ns | |
| | | | SSP1 | | $0.5t_{SCK}$+30ns | |
| | | CPHA = 1 | SSP0 | | $t_{SCK}$+15ns | |
| | | | SSP1 | | $t_{SCK}$+30ns | |
| $t_{SCKQV}$ | SCK trigger edge to data output MOSI valid time | | SSP0 | | 15 | |
| | | | SSP1 | | 30 | |
| $t_{SCKQX}$ | SCK trigger edge to data output MOSI invalid time | | SSP0 | 0 | | |
| | | | SSP1 | 0 | | |
| $t_{su}$ | Data input (MISO) setup time w.r.t SCK sampling edge | | SSP0 | 25 | | |
| | | | SSP1 | 25 | | |
| $t_h$ | Data input (MISO) hold time w.r.t SCK sampling edge | | SSP0 | 0 | | |
| | | | SSP1 | 0 | | |

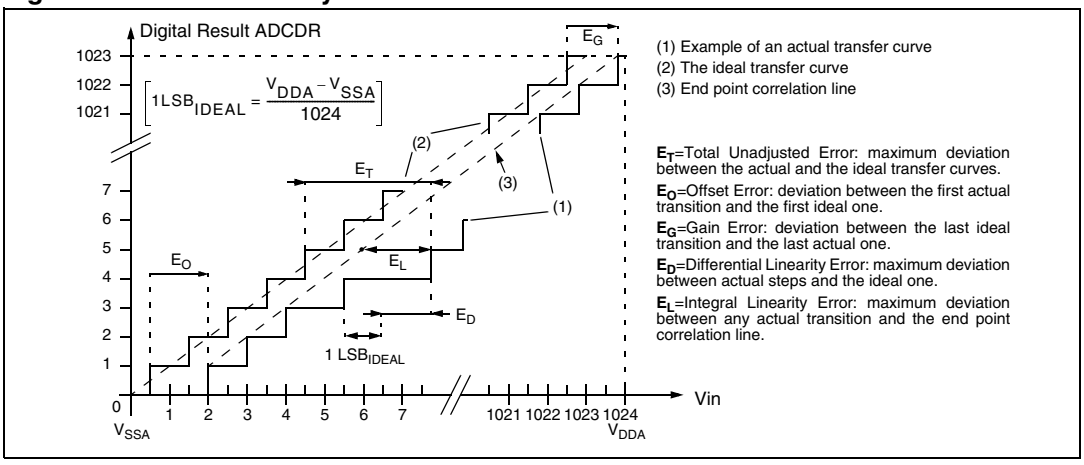
1. Data based on characterisation results, not tested in production.
2. Max frequency for the 2 SSPs is $f_{PCLK}/2$; $f_{PCLK}$ max = 32 MHz. This takes into account the frequency limitation due to I/O speed capability. SSP0 uses IO4 type while SSP1 uses IO2 type I/Os.

**Table 47. ADC accuracy**

| ADC accuracy with $f_{CK\_SYS}$ = 20 MHz, $f_{ADC}$=8 MHz, $R_{AIN}$ < 10 kΩ<br>This assumes that the ADC is calibrated(1) | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Typ** | **Max** | **Unit** |
| $\|E_T\|$ | Total unadjusted error (2) (3) | $V_{DDA\_ADC}$=3.3 V | 1 | 1.2 | LSB |
| | | $V_{DDA\_ADC}$=5.0 V | 1 | 1.2 | |
| $\|E_O\|$ | Offset error(2) (3) | $V_{DDA\_ADC}$=3.3 V | 0.15 | 0.5 | |
| | | $V_{DDA\_ADC}$=5.0 V | 0.15 | 0.5 | |
| $E_G$ | Gain Error (2) (3) | $V_{DDA\_ADC}$=3.3 V | -0.8 | -0.2 | |
| | | $V_{DDA\_ADC}$=5.0 V | -0.8 | -0.2 | |
| $\|E_D\|$ | Differential linearity error(2) (3) | $V_{DDA\_ADC}$=3.3 V | 0.7 | 0.9 | |
| | | $V_{DDA\_ADC}$=5.0 V | 0.7 | 0.9 | |
| $\|E_L\|$ | Integral linearity error (2) (3) | $V_{DDA\_ADC}$=3.3 V | 0.6 | 0.8 | |
| | | $V_{DDA\_ADC}$=5.0 V | 0.6 | 0.8 | |

1. Calibration is needed once after each power-up.
2. Refer to *ADC accuracy vs. negative injection current on page 73*
3. ADC Accuracy vs. MCO (Main Clock Output): the ADC accuracy can be significantly degraded when activating the MCO on pin P0.01 while converting an analog channel (especially those which are close to the MCO pin). To avoid this, when an ADC conversion is launched, it is strongly recommended to disable the MCO.

**Figure 44. ADC accuracy characteristics**



# 8 Order codes

**Table 49. Order codes**

| Order code | Flash Prog. Memory (Bank 0) Kbytes | Package | CAN Periph | USB Periph | Nominal Temp. Range ($T_A$) |
|---|---|---|---|---|---|
| STR750FV0T6 | 64 | LQFP100 14x14 | Yes | Yes | -40 to +85°C |
| STR750FV1T6 | 128 | | | | |
| STR750FV2T6 | 256 | | | | |
| STR750FV0H6 | 64 | LFBGA100 10x10 | | | |
| STR750FV1H6 | 128 | | | | |
| STR750FV2H6 | 256 | | | | |
| STR751FR0T6 | 64 | LQFP64 10x10 | - | Yes | -40 to +85°C |
| STR751FR1T6 | 128 | | | | |
| STR751FR2T6 | 256 | | | | |
| STR751FR0H6 | 64 | LFBGA64 8x8 | | | |
| STR751FR1H6 | 128 | | | | |
| STR751FR2H6 | 256 | | | | |
| STR752FR0T6 | 64 | LQFP64 10x10 | Yes | - | -40 to +85°C |
| STR752FR1T6 | 128 | | | | |
| STR752FR2T6 | 256 | | | | |
| STR752FR0H6 | 64 | LFBGA64 8x8 | | | |
| STR752FR1H6 | 128 | | | | |
| STR752FR2H6 | 256 | | | | |
| STR752FR0T7 | 64 | LQFP64 10x10 | Yes | - | -40 to +105°C |
| STR752FR1T7 | 128 | | | | |
| STR752FR2T7 | 256 | | | | |
| STR752FR0H7 | 64 | LFBGA64 8x8 | | | |
| STR752FR1H7 | 128 | | | | |
| STR752FR2H7 | 256 | | | | |
| STR755FR0T6 | 64 | LQFP64 10x10 | - | - | -40 to +85°C |
| STR755FR1T6 | 128 | | | | |
| STR755FR2T6 | 256 | | | | |
| STR755FR0H6 | 64 | LFBGA64 8x8 | | | |
| STR755FR1H6 | 128 | | | | |
| STR755FR2H6 | 256 | | | | |