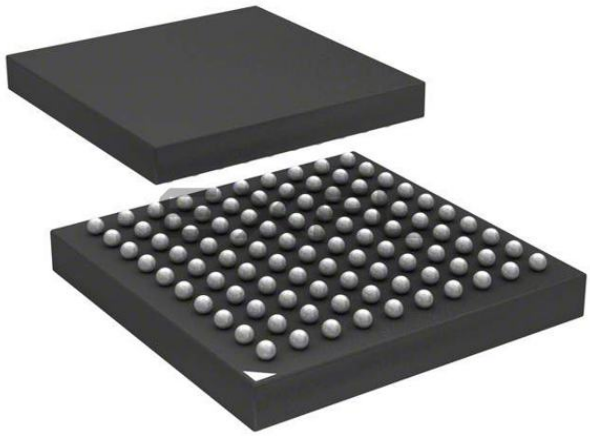

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, I²C, SPI, SSI, SSP, UART/USART, USB
Peripherals	DMA, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str750fv2h6

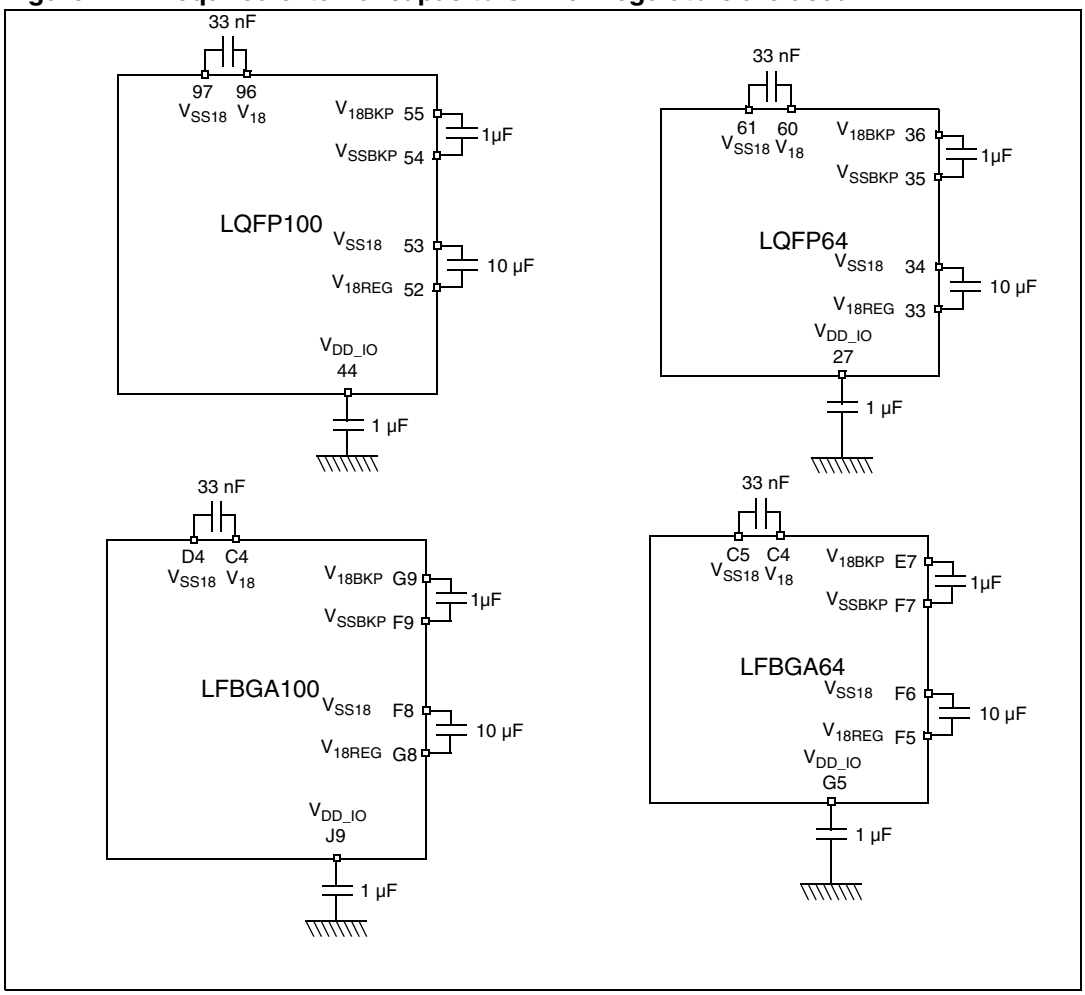
GPIOs (general purpose input/output)

Each of the 72 GPIO pins (38 GPIOs in 64-pin devices) can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as Peripheral Alternate Function. Port 1.15 is an exception, it can be used as general-purpose input only or wake-up from STANDBY mode (WKP_STDBY). Most of the GPIO pins are shared with digital or analog alternate functions.

68	A10			P1.02 / TIM2_OC2	I/O	T_T	**X**	X		O2	X	X	**Port 1.02**	TIM2: Output compare 2 (remappable to P0.06)(8)
69	D7	44	C6	VDD_IO	S								Supply Voltage for digital I/Os	
70	D8	45	D6	VDDA_ADC	S								Supply Voltage for A/D converter	
71	C9			P2.11	I/O	T_T	**X**	X		O2	X	X	**Port 2.11**	
72	B10			P2.10	I/O	T_T	**X**	X		O2	X	X	**Port 2.10**	
73	C8	46	D7	VSSA_ADC	S								Ground Voltage for A/D converter	
74	C7	47	C7	VSS_IO	S								Ground Voltage for digital I/Os	
75	E8	48	D5	VREG_DIS	I	T_T							Voltage Regulator Disable input	
76	A9	49	A8	P0.07 / SMI_DOUT / SSP0_MOSI	I/O	T_T	**X**	X	EIT2	O4	X	X	**Port 0.07**	Serial Memory Interface: data output / SSP0: Master out Slave in data
77	A8	50	A7	P0.06 / SMI_DIN / SSP0_MISO	I/O	T_T	**X**	X		O4	X	X	**Port 0.06**	Serial Memory Interface: data input / SSP0: Master in Slave out data
78	A7	51	A6	P0.05 / SSP0_SCLK / SMI_CK	I/O	T_T	**X**	X	EIT1	O4	X	X	**Port 0.05**	SSP0: Serial clock / Serial Memory Interface: Serial clock output
79	B7	52	B6	P0.04 / SMI_CS0 / SSP0_NSS	I/O	T_T	**X**	X		O4	X	X	**Port 0.04**	Serial Memory Interface: chip select output 0 / SSP0: Slave select input
80	C5	53	B7	P1.10 PWM_EMERGENCY	I/O	T_T	**X**	X	EIT10	O2	X	X	**Port 1.10**	PWM: Emergency input
81	B6	54	B5	P1.09 / PWM1	I/O	T_T	**X**	X	EIT9	O4	X	X	**Port 1.09**	PWM: PWM1 output
82	C6			P2.09 / PWM1N	I/O	T_T	**X**	X		O2	X	X	**Port 2.09**	PWM: PWM1 complementary output(4)

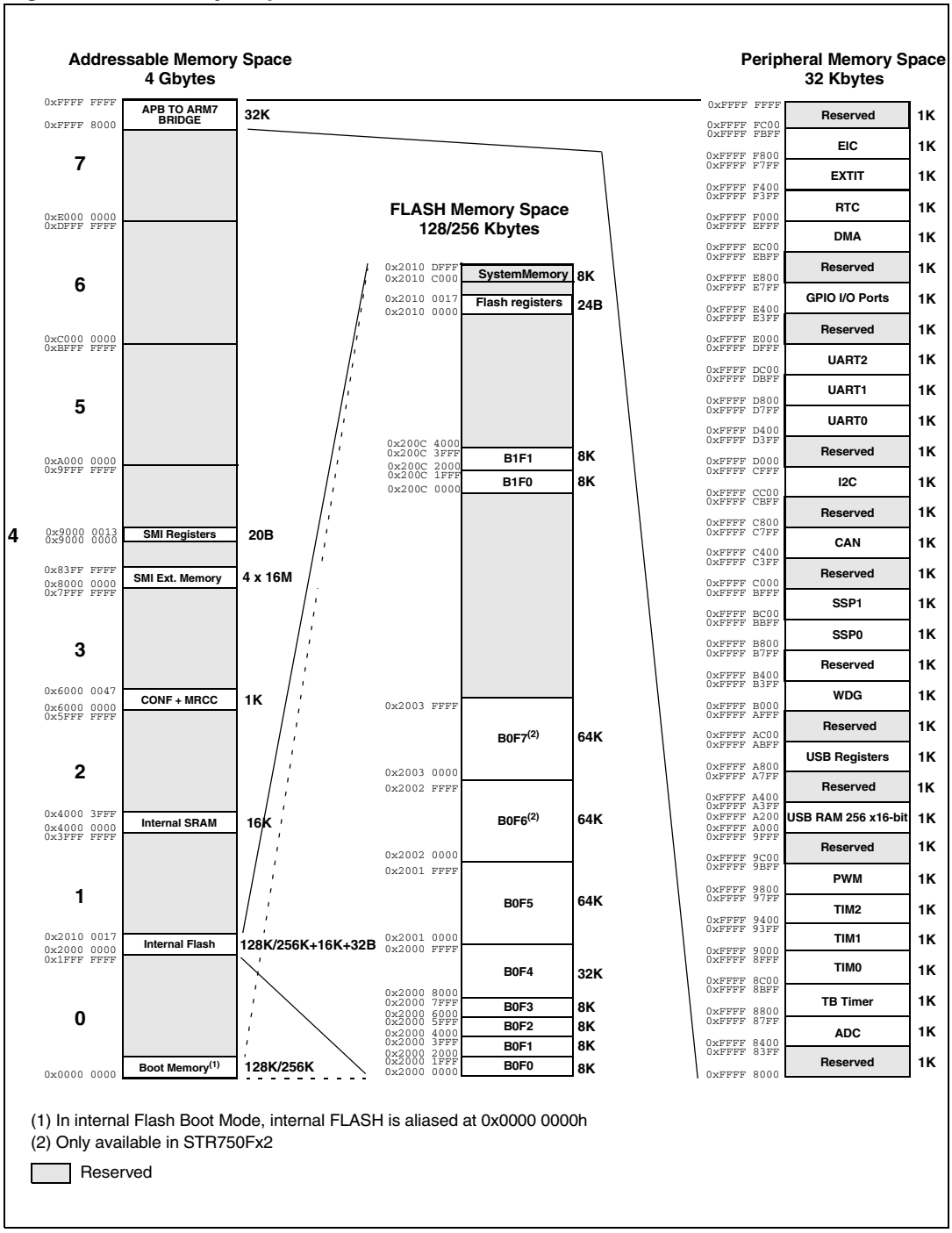
4.2 External components

Figure 4. Required external capacitors when regulators are used



5 Memory map

Figure 5. Memory map

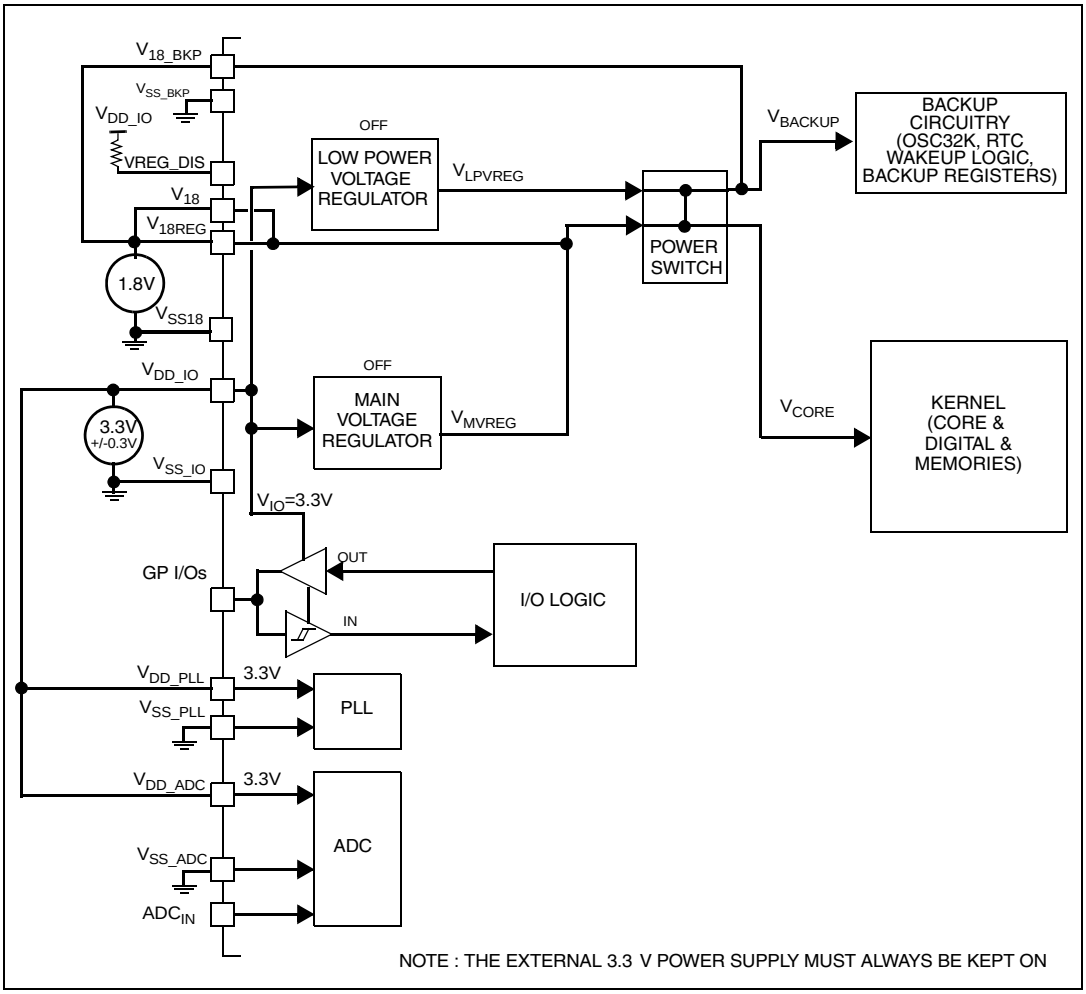


(1) In internal Flash Boot Mode, internal FLASH is aliased at 0x0000 0000h
(2) Only available in STR750Fx2

Reserved

Power supply scheme 2: Dual external 1.8V and 3.3V supply

Figure 9. Power supply scheme 2



6.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

6.2.1 Voltage characteristics

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD_x} - V_{SS_X} (1)	Including V_{DDA_ADC} and V_{DDA_PLL}	-0.3	6.5	V
V_{18} - V_{SS18}	Digital 1.8 V Supply voltage on all V_{18} power pins (when 1.8 V is provided externally)	-0.3	2.0	
V_{IN}	Input voltage on any pin (2)	V_{SS}-0.3 to V_{DD_IO}+0.3	V_{SS}-0.3 to V_{DD_IO}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different 3.3 V or 5.0 V power pins		50	mV
$\lvert\Delta V_{18x}\rvert$	Variations between different 1.8 V power pins(3)		25	
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 52*	see *: Absolute maximum ratings (electrical sensitivity) on page 52*	
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)			

1. All 3.3 V or 5.0 V power (V_{DD_IO}, V_{DDA_ADC}, V_{DDA_PLL}) and ground (V_{SS_IO}, V_{SSA_ADC}, V_{DDA_ADC}) pins must always be connected to the external 3.3V or 5.0V supply. When powered by 3.3V, I/Os are not 5V tolerant.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
3. Only when using external 1.8 V power supply. All the power (V_{18}, V_{18REG}, V_{18BKP}) and ground (V_{SS18}, V_{SSBKP}) pins must always be connected to the external 1.8 V supply.

6.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 11. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{VDD_IO}	V_{DD_IO} rise time rate		20			µs/V
					20	ms/V
t_{V18}	V_{18} rise time rate (1)	When 1.8 V power is supplied externally	20			µs/V
					20	ms/V

1. Data guaranteed by characterization, not tested in production.

6.3.3 Embedded voltage regulators

Subject to general operating conditions for V_{DD_IO}, and T_A

Table 12. Embedded voltage regulators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{MVREG}	MVREG power supply(1)	load <150 mA	1.65	1.80	1.95	V
V_{LPVREG}	LPVREG power supply(2)	load <10 mA	1.30	1.40	1.50	V
t_{VREG_PWRUP}(1)	Voltage Regulators start-up time (to reach 90% of final V_{18} value) at V_{DD_IO} power-up(3)	V_{DD_IO} rise slope = 20 µs/V		80		µs
		V_{DD_IO} rise slope = 20 ms/V		35		ms

1. V_{MVREG} is observed on the V_{18}, V_{18REG} and V_{18BKP} pins except in the following case:
   - In STOP mode with MVREG OFF (LP_PARAM13 bit). See note 2.
   - In STANDBY mo*de. See note 2.*
2. In STANDBY mode, V_{LPVREG} is observed on the V_{18BKP} pin
   In STOP mode, V_{LPVREG} is observed on the V_{18}, V_{18REG} and V_{18BKP} pins.
3. Once V_{DD_IO} has reached 3.0 V, the RSM (Regulator Startup Monitor) generates an internal RESET during this start-up time.

Figure 16. Power consumption in STOP mode in Single supply scheme (3.3 V range)

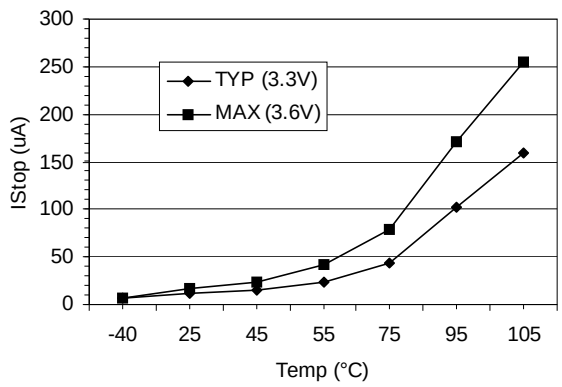


Figure 17. Power consumption in STOP mode Single supply scheme (5 V range)

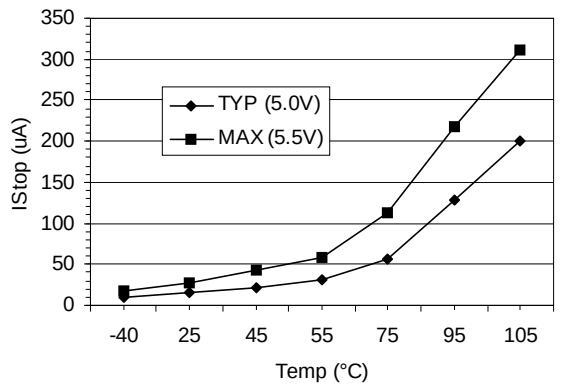


Figure 18. Power consumption in STANDBY mode (3.3 V range)

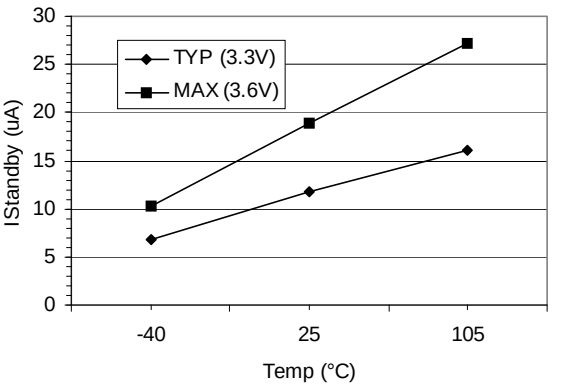


Figure 19. Power consumption in STANDBY mode (5 V range)

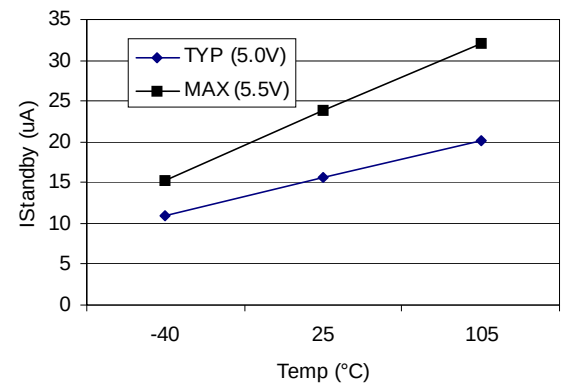


Table 16. Dual supply supply typical power consumption in Run, WFI, Slow and Slow-WFI modes

To calculate the power consumption in Dual supply mode, refer to the values given in *Table 15*. and consider that this consumption is split as follows:

$I_{DD(single\ supply)} \sim I_{DD(dual\ supply)} = I_{DD\_V18} + I_{DD(VDD\_IO)}$

For 3.3V range: $I_{DD(VDD\_IO)}$ ~ 1 to 2 mA

For 5V range: $I_{DD(VDD\_IO)}$ ~ 2 to 3 mA

Therefore most of the consumption is sunk on the V_{18} power supply

This formula does not apply in STOP and STANDBY modes, refer to *Table 17*.

Subject to general operating conditions for V_{DD_IO}, and T_A

Table 17. Typical power consumption in STOP and STANDBY modes

Symbol	Parameter	Conditions		3.3V Typ(1)	5V Typ(2)	Unit
I_{DD}(3)	Supply current in STOP mode(4)	LP_PARAM bits: ALL OFF(5)		12	15	µA
		LP_PARAM bits : MVREG ON, OSC4M OFF, FLASH OFF(6)		130	135	
		LP_PARAM bits: MVREG ON, OSC4M ON , FLASH OFF(6)		1950	1930	
		LP_PARAM bits: MVREG ON, OSC4M OFF, FLASH ON (6)		630	635	
		LP_PARAM bits: MVREG ON, OSC4M ON, FLASH ON (6)		2435	2425	
	Supply current in STOP mode(7)	LPPARAM bits: ALL OFF, with V_{18}=1.8 V	I_{DD_V18} I_{DD_V33}	5 <1	5 <1	µA
		LP_PARAM bits: OSC4M ON, FLASH OFF	I_{DD_V18} I_{DD_V33}	410 1475	410 1435	
		LP_PARAM bits: OSC4M OFF, FLASH ON	I_{DD_V18} I_{DD_V33}	550 <1	550 1	
		LP_PARAM bits: OSC4M ON, FLASH ON	I_{DD_V18} I_{DD_V33}	910 1475	910 1445	
	Supply current in STANDBY mode(4)	RTC OFF		11	14	µA
		RTC ON clocked by OSC32K		14	18	

1. Typical data are based on T_A=25°C, V_{DD_IO}=3.3 V and V_{18}=1.8 V unless otherwise indicated in the table.
2. Typical data are based on T_A=25°C, V_{DD_IO}=5.0 V and V_{18}=1.8 V unless otherwise indicated in the table.
3. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4 on page 36*.
4. Single supply scheme see *Figure 12*.
5. In this mode, the whole digital circuitry is powered internally by the LPVREG at approximately 1.4 V, which significantly reduces the leakage currents.
6. In this mode, the whole digital circuitry is powered internally by the MVREG at 1.8 V.
7. Dual supply scheme see *Figure 13*.

Supply and clock manager power consumption

Table 18. Supply and clock manager power consumption

Symbol	Parameter	Conditions[1]	3.3V Typ	5V Typ	Unit
$I_{DD(OSC4M)}$	Supply current of resonator oscillator in STOP or WFI mode (LP_PARAM bit: OSC4M ON)	External components specified in: *4/8 MHz crystal / ceramic resonator oscillator (XT1/XT2) on page 46*	1815	1795	µA
$I_{DD(FLASH)}$	FLASH static current consumption in STOP or WFI mode (LP_PARAM bit FLASH ON)		515	515	
$I_{DD(MVREG)}$	Main Voltage Regulator static current consumption in STOP mode (LP_PARAM bit: MVREG ON)		130	135	
$I_{DD(LPVREG)}$	Low Power Voltage Regulator + RSM current static current consumption	STOP mode includes leakage where V_{18} is internally set to 1.4 V	12	15	
		STANDBY mode where V_{18BKP} and V_{18} are internally set to 1.4 V and 0 V respectively	11	14	

1. Measurements performed in 3.3V single supply mode see *Figure 12*

OSC32K crystal / ceramic resonator oscillator

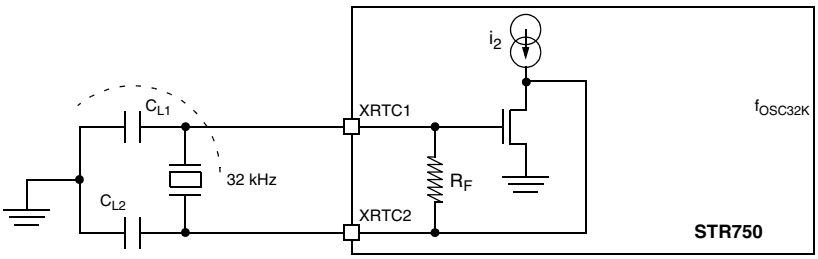
The STR7 RTC clock can be supplied with a 32.768 kHz Crystal/Ceramic resonator oscillator. All the information given in this paragraph are based on product characterisation with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

Table 23. OSC32K crystal / ceramic resonator oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC32K}	Oscillator Frequency			32.768		kHz
R_F	Feedback resistor	V_{DD_IO}=3.3 V or 5.0 V	270	310	370	kΩ
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal or ceramic resonator (R_S)(1)	R_S=40KΩ		12.5	15	pF
i_2	XT2 driving current	V_{DD_IO}=3.3 V or 5.0 V V_{IN}=V_{SS}	1		5	µA
$t_{SU(OSC32K)}$(2)	Startup time	V_{DD_IO} is stabilized		2.5		s

1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value. Refer to crystal/ceramic resonator manufacturer for more details
2. $t_{SU(OSC32K)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 32 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal/ceramic resonator manufacturer

Figure 22. Typical application with a 32.768 kHz crystal or ceramic resonator



PLL characteristics

PLL Jitter Terminology

- Self-referred single period jitter (period jitter)

  Period Jitter is defined as the difference of the maximum period (T_{max}) and minimum period (T_{min}) at the output of the PLL where T_{max} is the maximum time difference between 2 consecutive clock rising edges and T_{min} is the minimum time difference between 2 consecutive clock rising edges.

  See *Figure 23*

- Self-referred long term jitter (N period jitter)

  Self-referred long term Jitter is defined as the difference of the maximum period (T_{max}) and minimum period (T_{min}) at the output of the PLL where T_{max} is the maximum time

Output speed

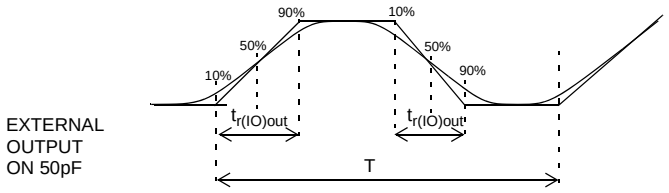
Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

Table 34. Output speed

I/O dynamic characteristics for V_{DD_IO} = 3.0 to 3.6V and EN33 bit =1 or V_{DD_IO} = 4.5 to 5.5V and EN33 bit =0							
I/O Type	**Symbol**	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
O2	$f_{max(IO)out}$	Maximum Frequency(1)	C_L=50 pF			10	MHz
	$t_{f(IO)out}$	Output high to low level fall time(2)	C_L=50 pF Between 10% and 90%			30	ns
	$t_{r(IO)out}$	Output low to high level rise time(2)				33	
O4	$f_{max(IO)out}$	Maximum Frequency(1)	C_L=50 pF			25	MHz
	$t_{f(IO)out}$	Output high to low level fall time(2)	C_L=50 pF Between 10% and 90%			12	ns
	$t_{r(IO)out}$	Output low to high level rise time(2)				14	
O8	$f_{max(IO)out}$	Maximum Frequency(1)	C_L=50pF			40	MHz
	$t_{f(IO)out}$	Output high to low level fall time(2)	C_L=50 pF Between 10% and 90%			6	ns
	$t_{r(IO)out}$	Output low to high level rise time(2)				6	

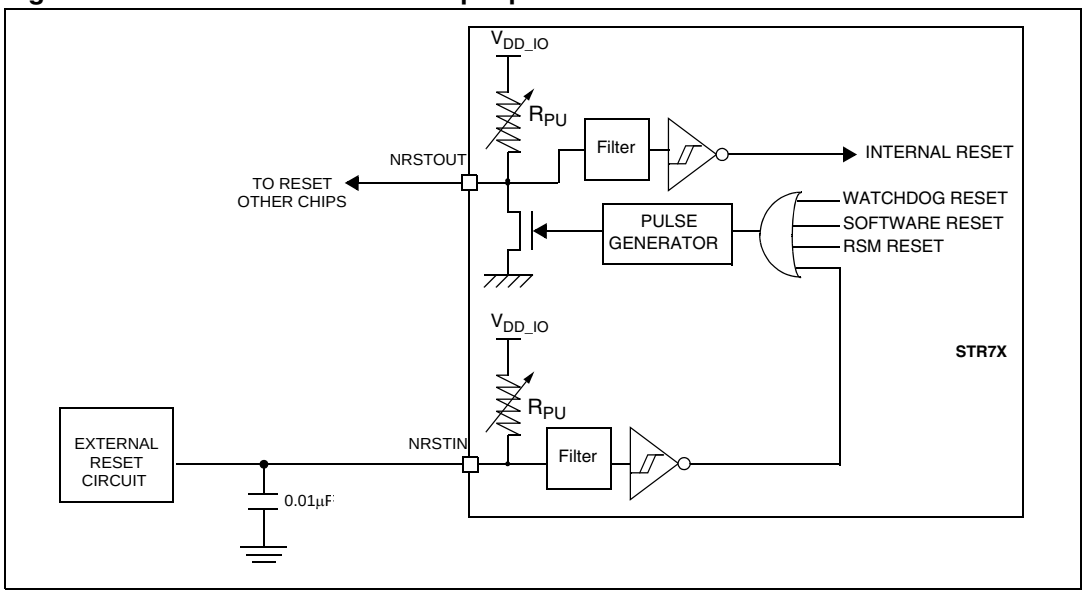
1. The maximum frequency is defined as described in *Figure 26*.
2. Data based on product characterisation, not tested in production.

Figure 26. I/O output speed definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by 50pF

Figure 27. Recommended NRSTIN pin protection



1. The user must ensure that the level on the NRSTIN pin can go below the $V_{IL(NRSTIN)}$ max. level specified in *NRSTIN and NRSTOUT pins on page 58*. Otherwise the reset will not be taken into account internally.

6.3.10 Communication interface characteristics

SSP synchronous serial peripheral in master mode (SPI or TI mode)

General operating conditions: V_{33}, 3.0V to 3.3V, V18 =1.8V, $C_L \approx 45$ pF.

Table 38. SSP master mode characteristics(1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK}	SPI clock frequency(2)		SSP0		16	MHz
			SSP1		8	
$t_{r(SCK)}$	SPI clock rise time		SSP0		14	ns
			SSP1		33	
$t_{f(SCK)}$	SPI clock fall time		SSP0		11	
			SSP1		30	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time		SSP0		19	
			SSP1		30	
t_{NSSLQV}	NSS low to Data Output MOSI valid time		SSP0		$0.5t_{SCK}$+15ns	
			SSP1		$0.5t_{SCK}$+30ns	
$t_{SCKNSSH}$	SCK last edge to NSS high	CPHA = 0	SSP0		$0.5t_{SCK}$+15ns	
			SSP1		$0.5t_{SCK}$+30ns	
		CPHA = 1	SSP0		t_{SCK}+15ns	
			SSP1		t_{SCK}+30ns	
t_{SCKQV}	SCK trigger edge to data output MOSI valid time		SSP0		15	
			SSP1		30	
t_{SCKQX}	SCK trigger edge to data output MOSI invalid time		SSP0	0		
			SSP1	0		
t_{su}	Data input (MISO) setup time w.r.t SCK sampling edge		SSP0	25		
			SSP1	25		
t_h	Data input (MISO) hold time w.r.t SCK sampling edge		SSP0	0		
			SSP1	0		

1. Data based on characterisation results, not tested in production.
2. Max frequency for the 2 SSPs is $f_{PCLK}/2$; f_{PCLK} max = 32 MHz. This takes into account the frequency limitation due to I/O speed capability. SSP0 uses IO4 type while SSP1 uses IO2 type I/Os.

Figure 34. SPI configuration - slave mode with CPHA=0, continuous transfer

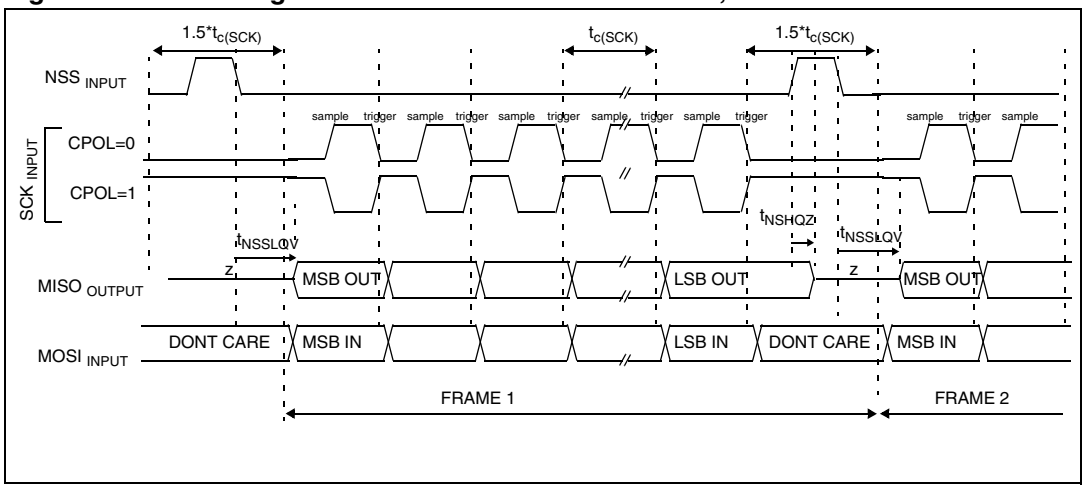


Figure 35. SPI configuration, slave mode with CPHA=1, single transfer

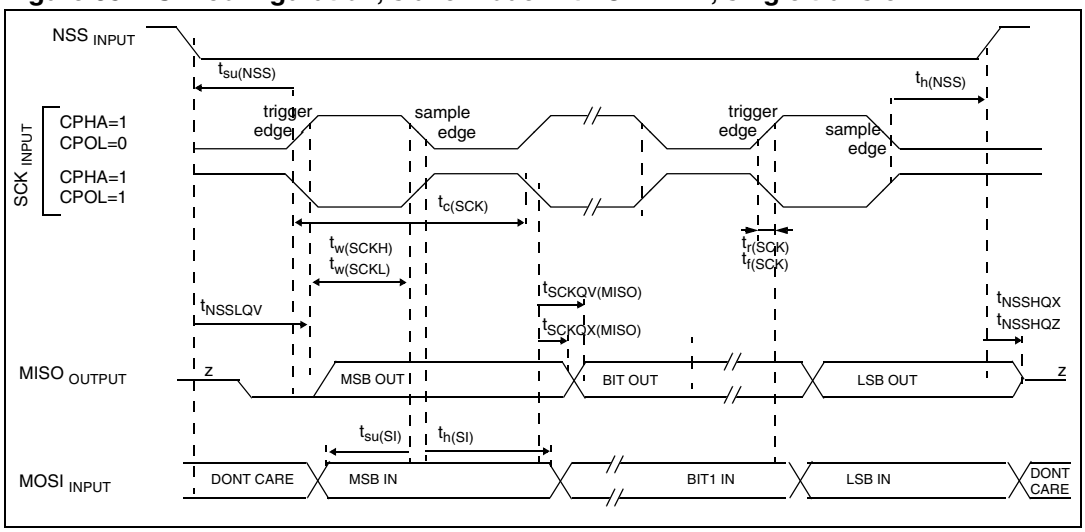


Figure 36. SPI configuration - slave mode with CPHA=1, continuous transfer

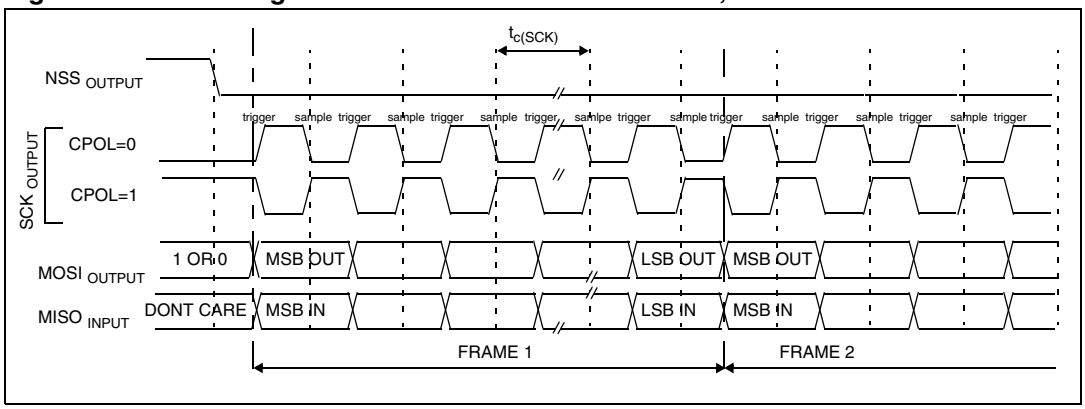


Figure 37. TI configuration - slave mode, single transfer

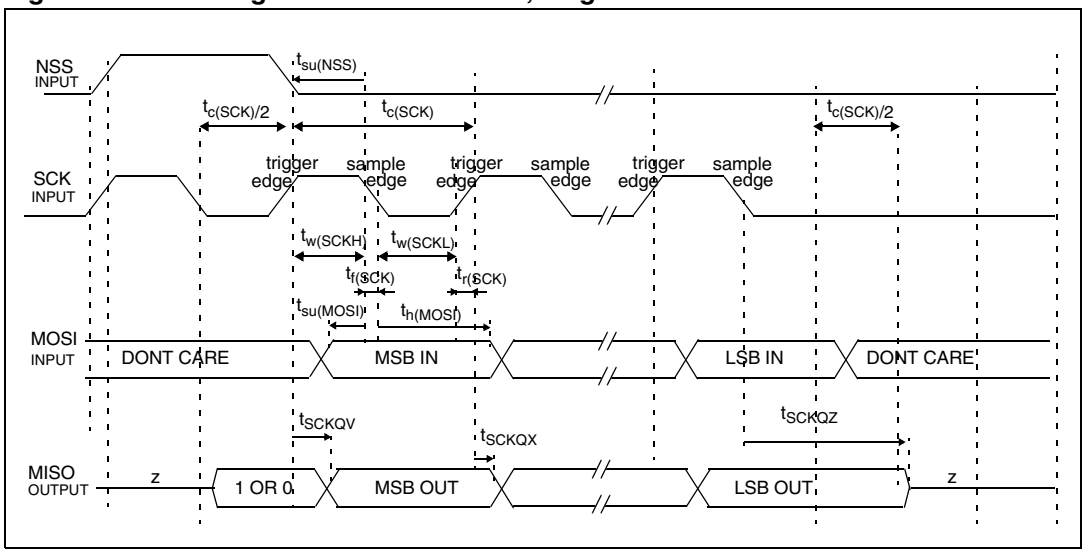
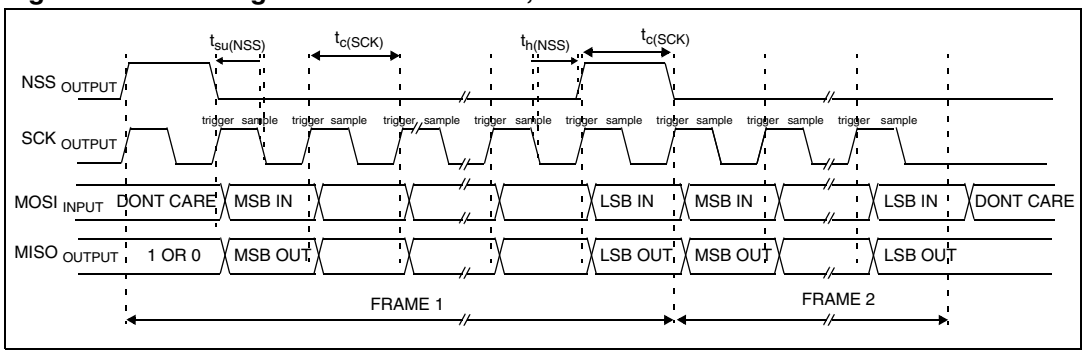


Figure 38. TI configuration - slave mode, continuous transfer



SMI - serial memory interface

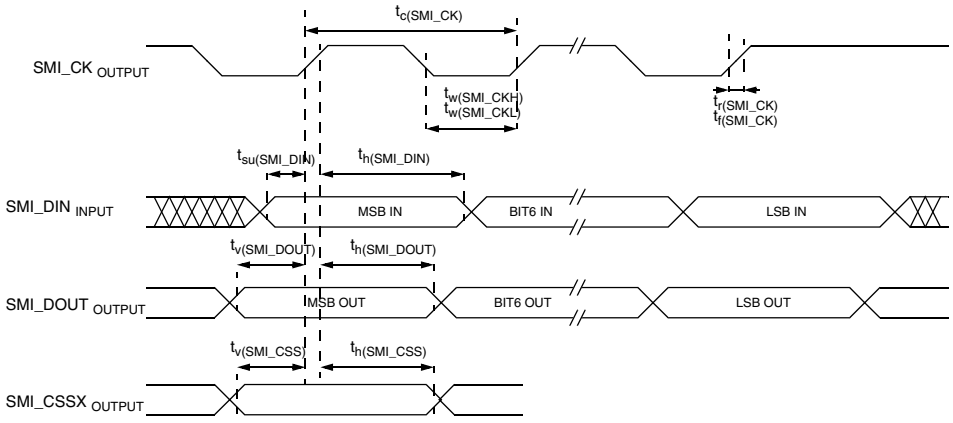
Subject to general operating conditions with $C_L \approx 30$ pF.

Table 40. SMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
f_{SMI_CK}	SMI clock frequency		32(2)(3)	MHz
			48(4)	
$t_{r(SMI\_CK)}$	SMI clock rise time		10	ns
$t_{f(SMI\_CK)}$	SMI clock fall time		8	
$t_{v(SMI\_DOUT)}$	Data output valid time		10	
$t_{h(SMI\_DOUT)}$	Data output hold time		0	
$t_{v(SMI\_CSSx)}$	CSS output valid time		10	
$t_{h(SMI\_CSSx)}$	CSS output hold time		0	
$t_{su(SMI\_DIN)}$	Data input setup time	0		
$t_{h(SMI\_DIN)}$	Data input hold time	5		

1. Data based on characterisation results, not tested in production.
2. Max. frequency = $f_{PCLK}/2 = 64/2 = 32$ MHz.
3. Valid for all temperature ranges: -40 to 105 °C, with 30 pF load capacitance.
4. Valid up to 60 °C, with 10 pF load capacitance.

Figure 39. SMI timing diagram



I²C - Inter IC control interface

Subject to general operating conditions for V_{DD_IO}, f_{PCLK}, and T_A unless otherwise specified.

The I²C interface meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Restriction: The I/O pins which SDA and SCL are mapped to are not “True” Open-Drain: when configured as open-drain, the PMOS connected between the I/O pin and V_{DD_IO} is disabled, but it is still present. Also, there is a protection diode between the I/O pin and V_{DD_IO}. Consequently, when using this I²C in a multi-master network, it is

Table 44. USB: Full speed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_{rfm}	Rise/ Fall Time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal Crossover Voltage		1.3	2.0	V

1. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

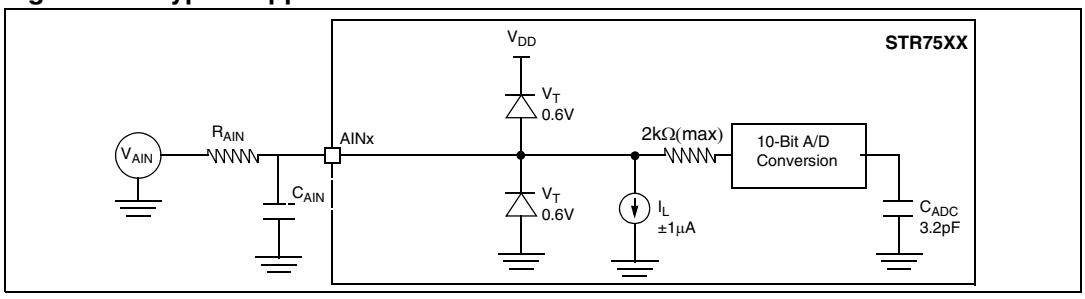
ADC accuracy vs. negative injection current

Injecting negative current on specific pins listed in *Table 46* (generally adjacent to the analog input pin being converted) should be avoided as this significantly reduces the accuracy of the conversion being performed. It is recommended to add a Schottky diode (pin to ground) to pins which may potentially inject negative current.

Table 46. List of adjacent pins

Analog input	Related adjacent pins
a	None
AIN1/P0.03	None
AIN2/P0.12	P0.11
AIN3/P0.17	P0.18 and P0.16
AIN4/P0.19	P0.24
AIN5/P0.22	None
AIN6/P0.23	P2.04
AIN7/P0.27	P1.11 and P0.26
AIN8/P0.29	P0.30 and P0.28
AIN9/P1.04	None
AIN10/P1.06	P1.05
AIN11/P1.08	P1.04 and P1.13
AIN12/P1.11	P2.17 and P0.27
AIN13/P1.12	None
AIN14/P1.13	P1.14 and P1.01
AIN15/P1.14	None

Figure 42. Typical application with ADC



Analog power supply and reference pins

The V_{DDA_ADC} and V_{SSA_ADC} pins are the analog power supply of the A/D converter cell.

Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see *: General PCB design guidelines on page 74*).

8 Order codes

Table 49. Order codes

Order code	Flash Prog. Memory (Bank 0) Kbytes	Package	CAN Periph	USB Periph	Nominal Temp. Range (T_A)
STR750FV0T6	64	LQFP100 14x14	Yes	Yes	-40 to +85°C
STR750FV1T6	128				
STR750FV2T6	256				
STR750FV0H6	64	LFBGA100 10x10			
STR750FV1H6	128				
STR750FV2H6	256				
STR751FR0T6	64	LQFP64 10x10	-	Yes	-40 to +85°C
STR751FR1T6	128				
STR751FR2T6	256				
STR751FR0H6	64	LFBGA64 8x8			
STR751FR1H6	128				
STR751FR2H6	256				
STR752FR0T6	64	LQFP64 10x10	Yes	-	-40 to +85°C
STR752FR1T6	128				
STR752FR2T6	256				
STR752FR0H6	64	LFBGA64 8x8			
STR752FR1H6	128				
STR752FR2H6	256				
STR752FR0T7	64	LQFP64 10x10	Yes	-	-40 to +105°C
STR752FR1T7	128				
STR752FR2T7	256				
STR752FR0H7	64	LFBGA64 8x8			
STR752FR1H7	128				
STR752FR2H7	256				
STR755FR0T6	64	LQFP64 10x10	-	-	-40 to +85°C
STR755FR1T6	128				
STR755FR2T6	256				
STR755FR0H6	64	LFBGA64 8x8			
STR755FR1H6	128				
STR755FR2H6	256				