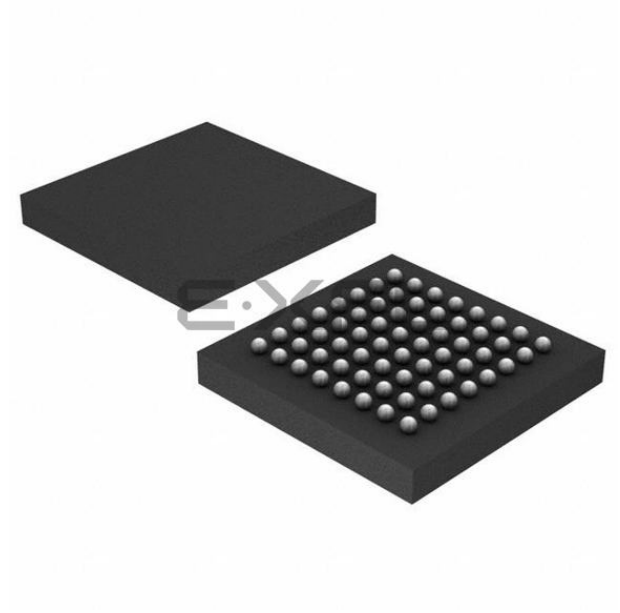

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, SPI, SSI, SSP, UART/USART, USB
Peripherals	DMA, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str751fr0h6

1 Description

The STR750 family of 32-bit microcontrollers combines the industry-standard ARM7TDMI® 32-bit RISC core, featuring high performance, very low power, and very dense code, with a comprehensive set of peripherals and ST's latest 0.18µ embedded Flash technology. The STR750 family comprises a range of devices integrating a common set of peripherals as well as USB, CAN and some key innovations like clock failure detection and an advanced motor control timer. It supports both 3.3V and 5V, and it is also available in an extended temperature range (-40 to +105°C). This makes it a genuine general purpose microcontroller family, suitable for a wide range of applications:

- Appliances, brushless motor drives
- USB peripherals, UPS, alarm systems
- Programmable logic controllers, circuit breakers, inverters
- Medical and portable equipment

2 Device overview

Table 2. Device overview

Features	STR755FR0 STR755FR1 STR755FR2	STR751FR0/ STR751FR1/ STR751FR2	STR752FR0/ STR752FR1/ STR752FR2	STR755FV0 STR755FV1/ STR755FV2	STR750FV0/ STR750FV1/ STR750FV2
Flash - Bank 0 (bytes)	64K/128K/256K				
Flash - Bank 1 (bytes)	16K RWW				
RAM (bytes)	16K				
Operating Temperature.	Ambient temp.:-40 to +85°C / -40 to +105°C (see *Table 49*) Junction temp. -40 to + 125 °C (see *Table 10*)				
Common Peripherals	3 UARTs, 2 SSPs, 1 I2C, 3 timers 1 PWM timer, 38 I/Os 13 Wake-up lines, 11 A/D Channels			3 UARTs, 2 SSPs, 1 I^2C, 3 timers 1 PWM timer, 72 I/Os 15 Wake-up lines, 16 A/D Channels	
USB/CAN peripherals	None	USB	CAN	None	USB+CAN
Operating Voltage	3.3V or 5V	3.3V	3.3V or 5V		
Packages (**x**)	**T**=LQFP64 10x10, **H**=LFBGA64			**T**=LQFP100 14x14, **H**=LFBGA100	

3 Introduction

This Datasheet contains the description of the STR750F family features, pinout, Electrical Characteristics, Mechanical Data and Ordering information.

For complete information on the Microcontroller memory, registers and peripherals. Please refer to the STR750F Reference Manual.

For information on the ARM7TDMI-S core please refer to the ARM7TDMI-S Technical Reference Manual available from Arm Ltd.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash Programming Reference Manual

For information on third-party development tools, please refer to the http://www.st.com/mcu website.

3.1 Functional description

The STR750F family includes devices in 2 package sizes: 64-pin and 100-pin. Both types have the following common features:

ARM7TDMI-S™ core with embedded Flash & RAM

STR750F family has an embedded ARM core and is therefore compatible with all ARM tools and software. It combines the high performance ARM7TDMI-S™ CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage FLASH memory and high-speed RAM.

Figure 1 shows the general block diagram of the device family.

Embedded Flash memory

Up to 256 KBytes of embedded Flash is available in Bank 0 for storing programs and data. An additional Bank 1 provides 16 Kbytes of RWW (Read While Write) memory allowing it to be erased/programmed on-the-fly. This partitioning feature is ideal for storing application parameters.

- When configured in burst mode, access to Flash memory is performed at CPU clock speed with 0 wait states for sequential accesses and 1 wait state for random access (maximum 60 MHz).
- When not configured in burst mode, access to Flash memory is performed at CPU clock speed with 0 wait states (maximum 32 MHz)

Embedded SRAM

16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

Enhanced interrupt controller (EIC)

In addition to the standard ARM interrupt controller, the STR750F embeds a nested interrupt controller able to handle up to 32 vectors and 16 priority levels. This additional hardware block provides flexible interrupt management features with minimal interrupt latency.

Figure 3. LQFP64 pinout

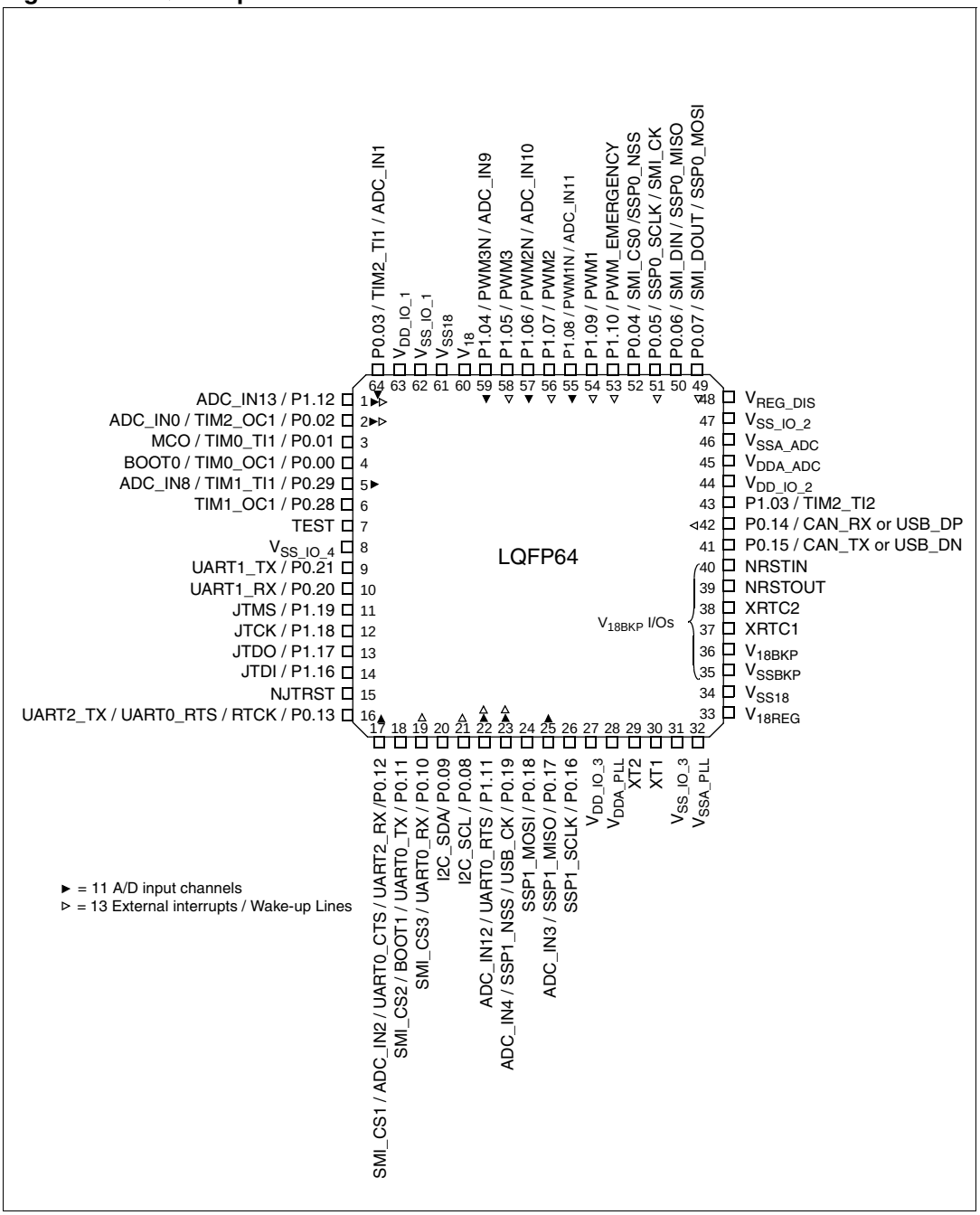


Table 4. LFBGA100 ball connections

	1	2	3	4	5	6	7	8	9	10
A	P0.03	P1.13	P1.14	P1.04	P1.06	P1.08	P0.05	P0.06	P0.07	P1.02
B	P1.12	P0.02	P0.01	P1.05	P1.07	P1.09	P0.04	P2.13	P1.03	P2.10
C	P0.31	P0.00	V_{DD_IO}	V_{18}	P1.10	P2.09	V_{SS_IO}	V_{SSA_ADC}	P2.11	USB_DP
D	P0.29	P0.30	V_{SS_IO}	V_{SS18}	P1.01	P1.15	V_{DD_IO}	V_{DDA_ADC}	P2.12	USB_DN
E	P0.28	P0.23	P0.22	V_{SS_IO}	TEST	P1.00	NRSTOUT	VREG_DIS	NRSTIN	P0.14
F	P2.03	P0.21	P0.20	P2.02	P2.04	P2.05	P2.06	V_{SS18}	V_{SSBKP}	P0.15
G	NJTRST	P1.18	P1.19	P2.01	P2.00	P2.07	2.08	V_{18REG}	V_{18BKP}	XRTC2
H	P0.13	P1.16	P1.17	P2.19	P2.18	P2.17	P0.24	P2.14	P2.16	XRTC1
J	P0.11	P0.12	P1.11	P0.27	P0.19	P0.26	P0.25	P2.15	V_{DD_IO}	V_{SS_IO}
K	P0.10	P0.09	P0.08	P0.18	P0.17	P0.16	XT1	XT2	V_{DDA_PLL}	V_{SSA_PLL}

Table 5. LFBGA64 ball connections

	1	2	3	4	5	6	7	8
A	P0.03	V_{SS_IO}	P1.04	P1.06	P1.08	P0.05	P0.06	P0.07
B	P1.12	V_{DD_IO}	P1.05	P1.07	P1.09	P0.04	P1.10	P1.03
C	P0.01	P0.02	P0.00	V_{18}	V_{SS18}	V_{DD_IO}	V_{SS_IO}	P0.14
D	P0.29	P0.28	TEST	V_{SS_IO}	VREG_DIS	V_{DDA_ADC}	V_{SSA_ADC}	P0.15
E	P1.18	P1.19	P0.20	P0.21	NRSTOUT	NRSTIN	V_{18BKP}	XRTC2
F	P0.13	NJTRST	P1.16	P1.17	V_{18REG}	V_{SS18}	V_{SSBKP}	XRTC1
G	P0.11	P0.12	P1.11	P0.19	V_{DD_IO}	V_{SS_IO}	V_{DDA_PLL}	V_{SSA_PLL}
H	P0.10	P0.09	P0.08	P0.17	P0.18	P0.16	XT2	XT1

Table 6. STR750F pin description (continued)

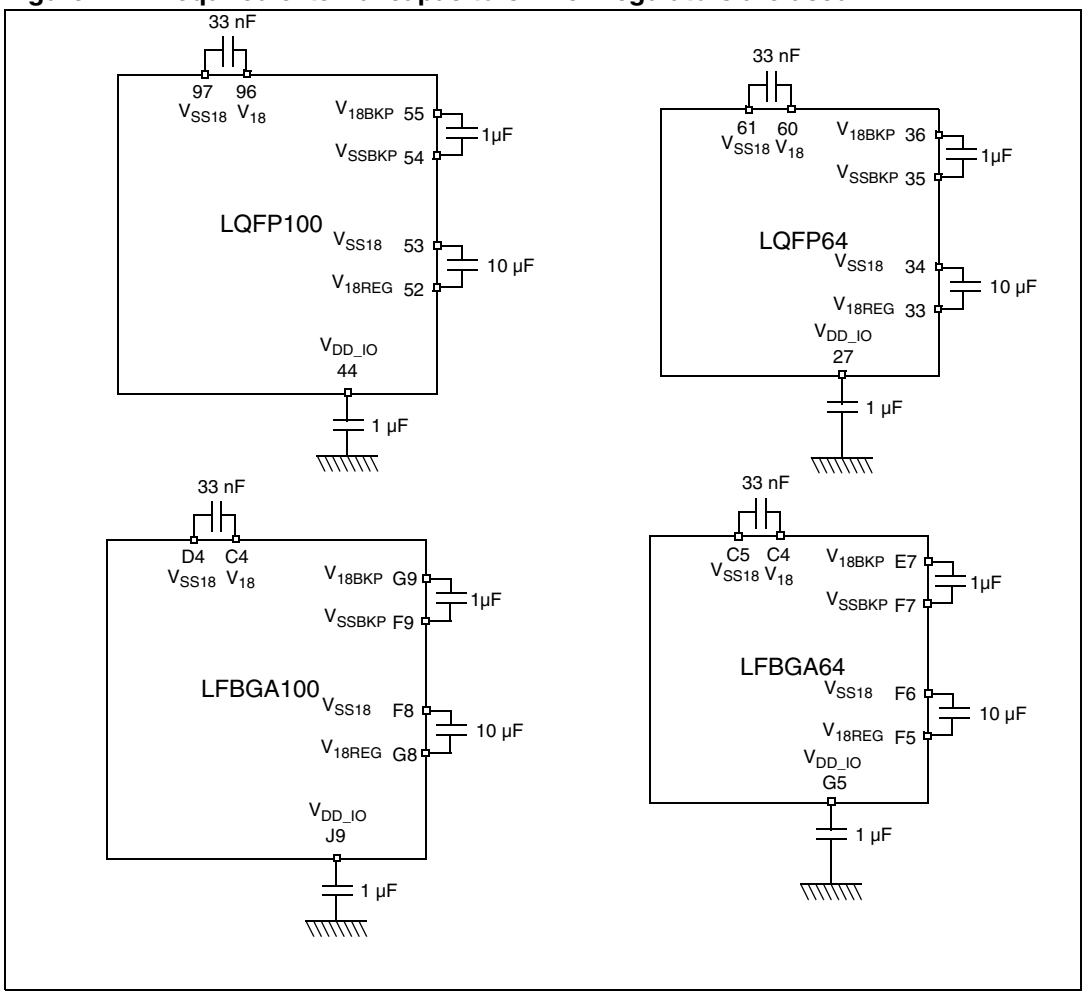
Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
7	D1	5	D1	P0.29 / TIM1_TI1 / ADC_IN8	I/O	T_T	**X**	X		O2	X	X		**Port 0.29**	TIM1: Input Capture 1	ADC: Analog input 8
8	E1	6	D2	P0.28 / TIM1_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 0.28**	TIM1: Output Compare 1	
9	E5	7	D3	TEST	I									Reserved, must be tied to ground		
10	E4	8	D4	VSS_IO	S									Ground Voltage for digital I/Os		
11	E2			P0.23 / UART1_RTS / ADC_IN6	I/O	T_T	**X**	X		O2	X	X		**Port 0.23**	UART1: Ready To Send output(4)	ADC analog input 6
12	F5			P2.04 / TIM2_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 2.04**	TIM2: Output Compare 1(4)	
13	F1			P2.03 / UART1_RTS	I/O	T_T	**X**	X		O2	X	X		**Port 2.03**	UART1: Ready To Send output(4)	
14	F4			P2.02	I/O	T_T	**X**	X		O2	X	X		**Port 2.02**		
15	E3			P0.22 / UART1_CTS / ADC_IN5	I/O	T_T	**X**	X		O2	X	X		**Port 0.22**	UART1: Clear To Send input	ADC: Analog input 5
16	F2	9	E4	P0.21 / UART1_TX	I/O	T_T	**X**	X		O2	X	X		**Port 0.21**	UART1: Transmit data output (remappable to P0.15)(4)	
17	F3	10	E3	P0.20 / UART1_RX	I/O	T_T	**X**	X		O2	X	X		**Port 0.20**	UART1: Receive data input (remappable to P0.14)(4)	
18	G3	11	E2	P1.19 / JTMS	I/O	T_T	X	X		O2	X	X		**JTAG mode selection input(6)**	Port 1.19	
19	G2	12	E1	P1.18 / JTCK	I/O	T_T	X	X		O2	X	X		**JTAG clock input(6)**	Port 1.18	
20	H3	13	F4	P1.17 / JTDO	I/O	T_T	X	X		O8	X	X		**JTAG data output(6)**	Port 1.17	
21	H2	14	F3	P1.16 / JTDI	I/O	T_T	X	X		O2	X	X		**JTAG data input(6)**	Port 1.16	
22	G1	15	F2	NJTRST	I	T_T								JTAG reset input(5)		
23	G4			P2.01	I/O	T_T	**X**	X		O2	X	X		**Port 2.01**		
24	G5			P2.00	I/O	T_T	**X**	X		O2	X	X		**Port 2.00**		
25	H1	16	F1	P0.13 / RTCK / UART0_RTS UART2_TX	I/O	T_T	X	X		O8	X	X		**JTAG return clock output(6)**	Port 0.13 / UART0: Ready To Send output(4)	UART2: Transmit Data output (when remapped)(8)

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
26	J2	17	G2	P0.12 / UART2_RX / UART0_CTS / ADC_IN2 / SMI_CS1	I/O	T_T	X	X		O4	X	X		**Port 0.12**	UART0: Clear To Send input	ADC: Analog input 2
															Serial Memory Interface: chip select output 1	UART2: Receive Data input (when remapped)(8)
27	J1	18	G1	P0.11 / UART0_TX / BOOT1 / SMI_CS2	I/O	T_T	X	X		O4	X	X		**Port 0.11/Boot mode selection input 1**	UART0: Transmit data output	Serial Memory Interface: chip select output 2
28	K1	19	H1	P0.10 / UART0_RX / SMI_CS3	I/O	T_T	X	X	EIT4	O2	X	X		**Port 0.10**	UART0: Receive Data input	Serial Memory Interface: chip select output 3
29	K2	20	H2	P0.09 / I2C_SDA	I/O	T_T	X	X		O4	X	X		**Port 0.09**	I2C: Serial Data	
30	K3	21	H3	P0.08 / I2C_SCL	I/O	T_T	X	X	EIT3	O4	X	X		**Port 0.08**	I2C: Serial clock	
31	H4			P2.19	I/O	T_T	X	X		O2	X	X		**Port 2.19**		
32	H5			P2.18	I/O	T_T	X	X		O2	X	X		**Port 2.18**		
33	H6			P2.17 / UART2_RTS	I/O	T_T	X	X		O2	X	X		**Port 2.17**	UART2: Ready To Send output(4)	
34	J3	22	G3	P1.11 /UART0_RTS ADC_IN12	I/O	T_T	X	X	EIT11	O8	X	X		**Port 1.11**	UART0: Ready To Send output(4)	ADC: Analog input 12
35	J4			P0.27 / UART2_RTS / ADC_IN7	I/O	T_T	X	X		O2	X	X		**Port 0.27**	UART2: Ready To Send output(8)	ADC: Analog input 7
36	J6			P0.26 / UART2_CTS	I/O	T_T	X	X		O2	X	X		**Port 0.26**	UART2: Clear To Send input	
37	J7			P0.25 / UART2_TX	I/O	T_T	X	X		O2	X	X		**Port 0.25**	UART2: Transmit data output (remappable to P0.13)(8)	
38	H7			P0.24 / UART2_RX	I/O	T_T	X	X		O2	X	X		**Port 0.24**	UART2: Receive data input (remappable to P0.12)(8)	
39	J5	23	G4	P0.19 / USB_CK / SSP1_NSS / ADC_IN4	I/O	T_T	X	X	EIT6	O2	X	X		**Port 0.19**	SSP1: Slave select input (remappable to P0.11)(8)	ADC: Analog input 4
															USB: 48 MHz Clock input	
40	K4	24	H5	P0.18 / SSP1_MOSI	I/O	T_T	X	X		O2	X	X		**Port 0.18**	SSP1: Master out/slave in data (remappable to P0.10)(8)	
41	K5	25	H4	P0.17 / SSP1_MISO / ADC_IN3	I/O	T_T	X	X		O2	X	X		**Port 0.17**	SSP1: Master in/slave out data (remappable to P0.09)(8)	ADC: Analog input 3
42	K6	26	H6	P0.16 / SSP1_SCLK	I/O	T_T	X	X		O2	X	X		**Port 0.16**	SSP1: serial clock (remappable to P0.08)(8)	

4.2 External components

Figure 4. Required external capacitors when regulators are used

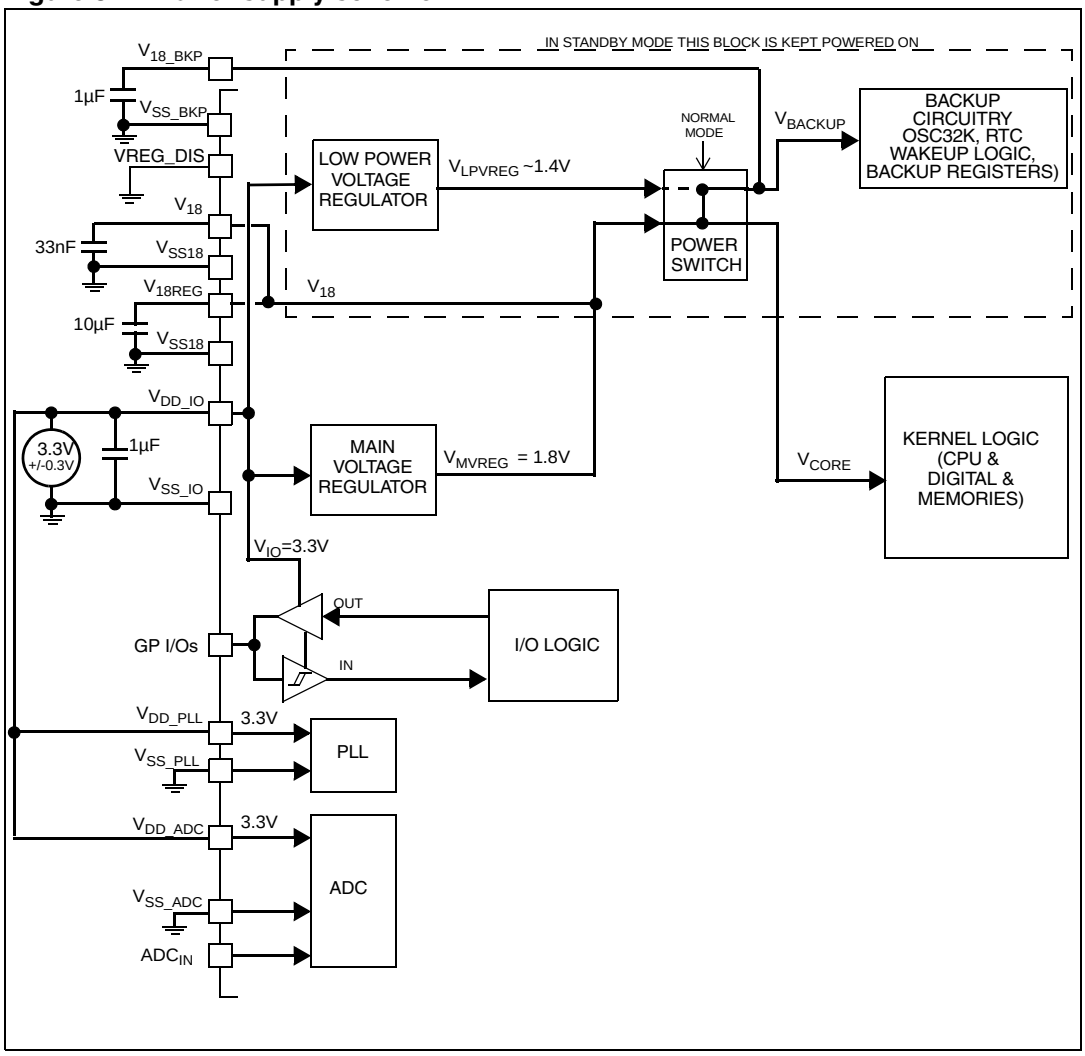


6.1.6 Power supply schemes

When mentioned, some electrical parameters can refer to a dedicated power scheme among the four possibilities. The four different power schemes are described below.

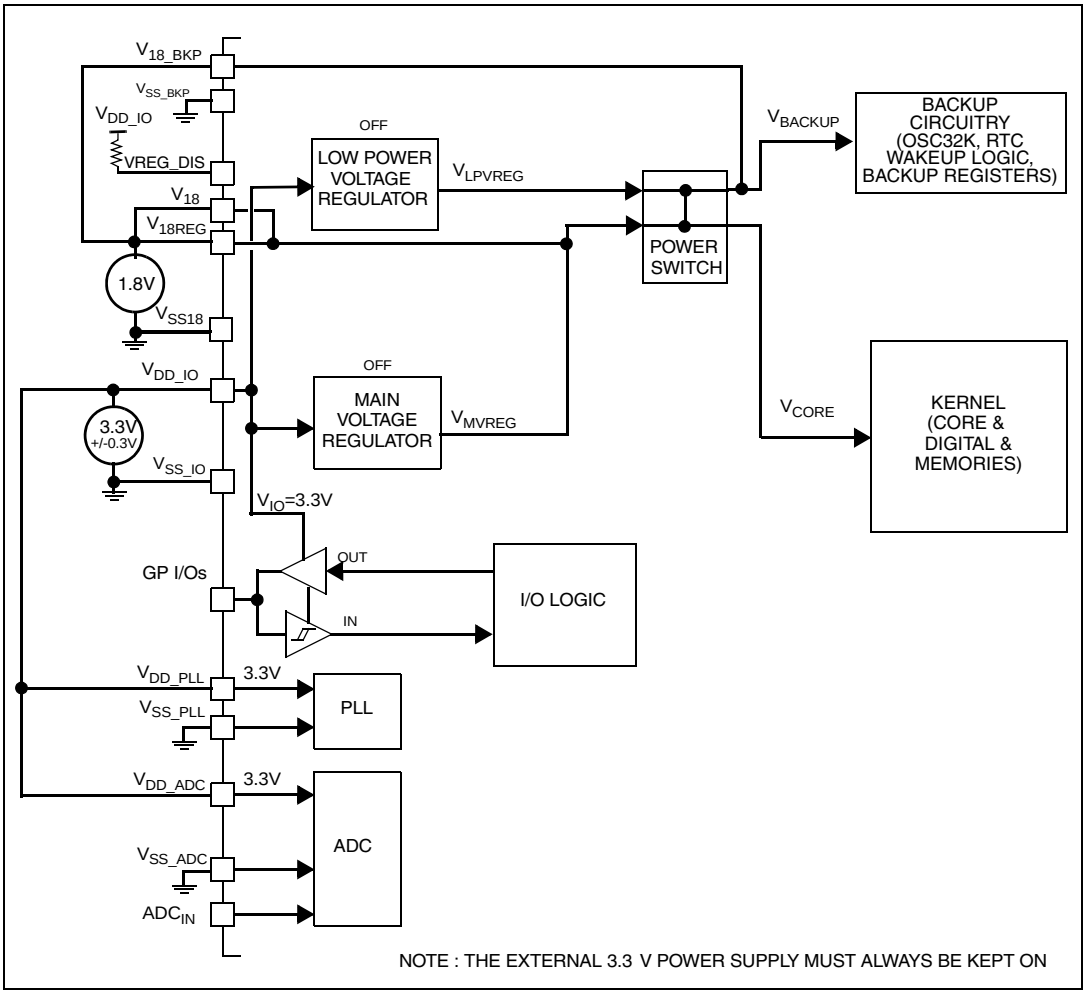
Power supply scheme 1: Single external 3.3 V power source

Figure 8. Power supply scheme 1



Power supply scheme 2: Dual external 1.8V and 3.3V supply

Figure 9. Power supply scheme 2



Typical power consumption

The following measurement conditions apply to *Table 15*, *Table 16* and *Table 17*.

In RUN mode:

- Program is executed from Flash (except if especially mentioned). The program consists of an infinite loop. When f_{HCLK} > 32 MHz, burst mode is activated.
- A standard 4 MHz crystal source is used.
- In all cases the PLL is used to multiply the frequency.
- All measurements are done in the single supply scheme with internal regulators used (see *Figure 12*)

In WFI Mode:

- In WFI Mode the measurement conditions are similar to RUN mode (OSC4M and PLL enabled). In addition, the Flash can be disabled depending on burst mode activation:
  - For AHB frequencies greater than 32 MHz, burst mode is activated and the Flash is kept enabled by setting the WFI_FLASH_EN bit (this bit cannot be reset when burst mode is activated).
  - For AHB frequencies less than or equal to 32 MHz, burst mode is deactivated, WFI_FLASH_EN is reset and the LP_PARAM14 bit is set (Flash is disabled in WFI mode).

In SLOW mode:

- The same program as in RUN mode is executed from Flash. The CPU is clocked by the FREEOSC, OSC4M, LPOSC or OSC32K. Only EXTIT peripheral is enabled in the MRCC_PCLKEN register.

In SLOW-WFI mode:

- In SLOW-WFI, the measurement conditions are similar to SLOW mode (CPU clocked by a low frequency clock). In addition, the LP_PARAM14 bit is set (FLASH is OFF). The WFI routine itself is executed from SRAM (it is not allowed to execute a WFI from the internal FLASH)

In STOP mode:

- Several measurements are given: in the single supply scheme with internal regulators used (see *Figure 12*): and in the dual supply scheme (see *Figure 13*).

In STANDBY mode:

- Three measurements are given:
  - The RTC is disabled, only the consumption of the LPVREG and RSM remain (almost no leakage currents)
  - The RTC is running, clocked by a standard 32.768 kHz crystal.
  - The RTC is running, clocked by the internal Low Power RC oscillator (LPOSC)
- STANDBY mode is only supported in the single supply scheme (see *Figure 12*)

Subject to general operating conditions for V_{DD_IO}, and T_A

Table 15. Single supply typical power consumption in Run, WFI, Slow and Slow-WFI modes

Symbol	Para meter	Conditions	3.3V typ(1)	5V typ(2)	Unit
I_{DD} (3)	Supply current in RUN mode(4)	Clocked by OSC4M with PLL multiplication, all peripherals enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz f_{HCLK}=56 MHz, f_{PCLK}=28 MHz f_{HCLK}=48 MHz, f_{PCLK}=24 MHz f_{HCLK}=32 MHz, f_{PCLK}=32 MHz f_{HCLK}=16 MHz, f_{PCLK}=16 MHz f_{HCLK}=8 MHz, f_{PCLK}=8 MHz	 80 75 65 59 34 20	 82 77 67 61 37 22	mA
		Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz f_{HCLK}=56 MHz, f_{PCLK}=28 MHz f_{HCLK}=48 MHz, f_{PCLK}=24 MHz f_{HCLK}=32 MHz, f_{PCLK}=32 MHz f_{HCLK}=16 MHz, f_{PCLK}=16 MHz f_{HCLK}=8 MHz, f_{PCLK}=8 MHz	 65 60 54 42 22 16	 67 62 55 44 24 18	mA
	Supply current in WFI mode(4)	Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz(5) f_{HCLK}=56 MHz, f_{PCLK}=28 MHz(5) f_{HCLK}=48 MHz, f_{PCLK}=24 MHz(5) f_{HCLK}=32 MHz, f_{PCLK}=32 MHz(6) f_{HCLK}=16 MHz, f_{PCLK}= 16 MHz (6) f_{HCLK}= 8 MHz, f_{PCLK}= 8 MHz(6)	 62 59 53 22 13 10	 63 60 54 23 15 11	mA
	Supply current in SLOW mode(4)	Clocked by FREEOSC: f_{HCLK}=f_{PCLK}=~5 MHz, Clocked by OSC4M: f_{HCLK}=f_{PCLK}=4 MHz Clocked by LPOSC: f_{HCLK}=f_{PCLK}=~300 kHz Clocked by OSC32K: f_{HCLK}=f_{PCLK}=32.768 kHz	9 8 3.65 3.5	10 9 3.9 4.2	mA
	Supply current in SLOW-WFI mode(4)(7)	Clocked by FREEOSC: f_{HCLK}=f_{PCLK}=~5 MHz Clocked by OSC4M: f_{HCLK}=f_{PCLK}=4 MHz Clocked by LPOSC: f_{HCLK}=f_{PCLK}=~300 kHz Clocked by OSC32K: f_{HCLK}=f_{PCLK}=32.768 kHz	3.5 3.1 1.15 0.98	4.0 3.75 1.65 1.5	mA

1. Typical data based on T_A=25° C and V_{DD_IO}=3.3V.
2. Typical data based on T_A=25° C and V_{DD_IO}=5.0V.
3. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4 on page 36*.
4. Single supply scheme see *Figure 14*.
5. Parameter setting BURST=1, WFI_FLASHEN=1
6. Parameter setting BURST=0, WFI_FLASHEN=0
7. Parameter setting WFI_FLASHEN=0, OSC4MOFF=1

XRTC1 external clock source

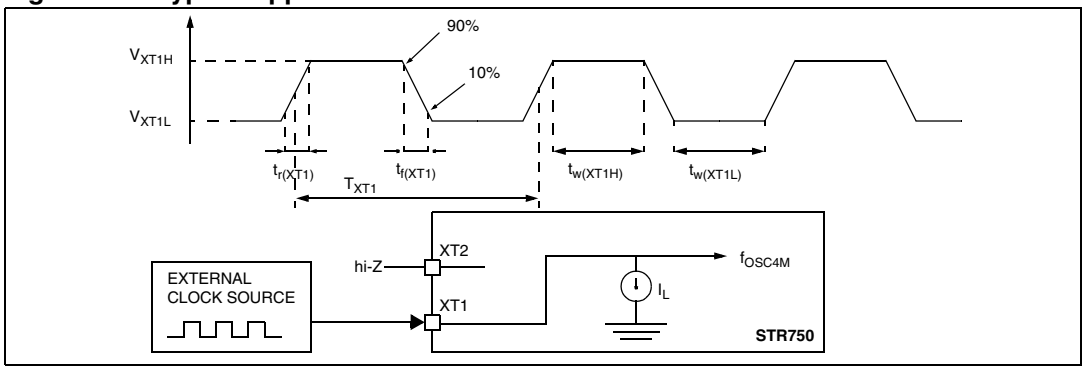
Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 21. XRTC1 external clock source

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
f_{XRTC1}	External clock source frequency	see *Figure 20*		32.768	500	kHz
V_{XRTC1H}	XRTC1 input pin high level voltage		$0.7xV_{DD\_IO}$		V_{DD_IO}	V
V_{XRTC1L}	XRTC1 input pin low level voltage		V_{SS}		$0.3xV_{DD\_IO}$	
$t_{w(XRTC1H)}$ $t_{w(XRTC1L)}$	XRTC1 high or low time(2)		900			ns
$t_{r(XRTC1)}$ $t_{f(XRTC1)}$	XRTC1 rise or fall time(2)				50	
I_L	XRTCx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD\_IO}$			±1	µA
$C_{IN(RTC1)}$	XRTC1 input capacitance(2)			5		pF
$DuCy_{(RTC1)}$	Duty cycle		30		70	%

1. Data based on typical application software.
2. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 20. Typical application with an external clock source



4/8 MHz crystal / ceramic resonator oscillator (XT1/XT2)

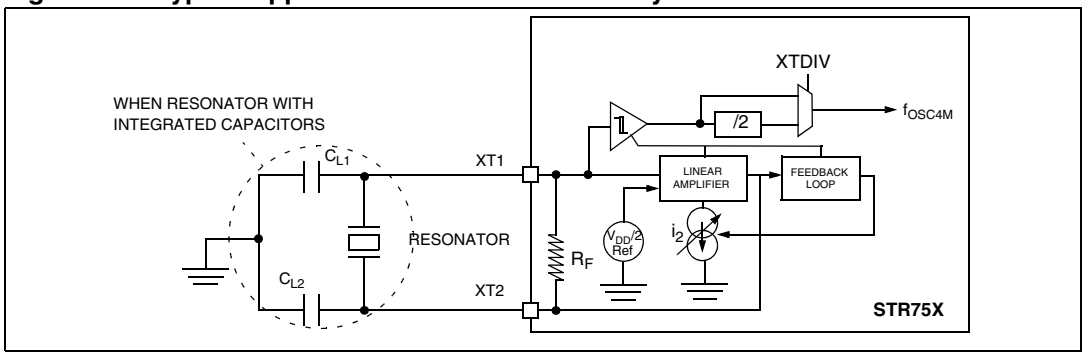
The STR750 system clock or the input of the PLL can be supplied by a OSC4M which is a 4 MHz clock generated from a 4 MHz or 8 MHz crystal or ceramic resonator. If using an 8 MHz oscillator, software set the XTDIV bit to enable a divider by 2 and generate a 4 MHz OSC4M clock. All the information given in this paragraph are based on product characterisation with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

Table 22. 4/8 MHz crystal / ceramic resonator oscillator (XT1/XT2)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC4M}	Oscillator frequency	4 MHz Crystal/Resonator Oscillator connected on XT1/XT2 XTDIV=0 or 8 MHz Crystal/Resonator Oscillator connected on XT1/XT2 XTDIV=1		4		MHz
R_F	Feedback resistor		200	240	270	kΩ
C_{L1}(2) C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal or ceramic resonator (R_S)(3)	R_S=200Ω			60	pF
i_2	XT2 driving current	V_{DD_IO}=3.3 V or 5.0 V		425		µA
$t_{SU(OSC4M)}$(4)	Startup time at V_{DD_IO} power-up			1		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5-pF to 25-pF range (typ.) designed for high-frequency applications and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included when sizing C_{L1} and C_{L2} (10 pF can be used as a rough estimate of the combined pin and board capacitance).
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(OSC4M)}$ is the typical start-up time measured from the moment V_{DD_IO} is powered (with a quick V_{DD_IO} ramp-up from 0 to 3.3V (<50µs) to a stabilized 4MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal/ceramic resonator manufacturer.

Figure 21. Typical application with a 4 or 8 MHz crystal or ceramic resonator



NRSTIN and NRSTOUT pins

NRSTIN Pin Input Driver is TTL/LVTTL as for all GP I/Os. A permanent pull-up is present which is the same as R_{PU} (see : General characteristics on page 54)

NRSTOUT Pin Output Driver is equivalent to the O2 type driver except that it works only as an open-drain (the P-MOS is de-activated). A permanent pull-up is present which is the same as R_{PU} (see : General characteristics on page 54)

Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

Table 35. NRSTIN and NRSTOUT pins

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
$V_{IL(NRSTIN)}$	NRSTIN Input low level voltage(1)					0.8	V
$V_{IH(NRSTIN)}$	NRSTIN Input high level voltage(1)			2			
$V_{hys(NRSTIN)}$	NRSTIN Schmitt trigger voltage hysteresis(2)				400		mV
$V_{OL(NRSTIN)}$	NRSTOUT Output low level voltage(3)	I_{IO}=+2 mA				0.4	V
$R_{PU(NRSTIN)}$	NRSTIN Weak pull-up equivalent resistor(4)	V_{IN}=V_{SS}	V_{DD_IO}=3.3 V	25	50	100	kΩ
			V_{DD_IO}=5 V	20	31	100	kΩ
$t_{w(RSTL)out}$	Generated reset pulse duration (visible at NRSTOUT pin)(5)	Internal reset source		15	20		µs
$t_{h(RSTL)in}$	External reset pulse hold time at NRSTIN pin(6)	At V_{DD_IO} power-up(5)		20			µs
		When V_{DD_IO} is established(5)		1			µs
$t_{g(RSTL)in}$	maximum negative spike duration filtered at NRSTIN pin(7)	The time between two spikes must be higher than 1/2 of the spike duration.			150		ns

1. Data based on product characterisation, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels.
3. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
4. The R_{PU} pull-up equivalent resistor are based on a resistive transistor
5. To guarantee the reset of the device, a minimum pulse of 15 µs has to be applied to the internal reset. At V_{DD_IO} power-up, the built-in reset stretcher may not generate the 15 µs pulse duration while once V_{DD_IO} is established, an external reset pulse will be internally stretched up to 15 µs thanks to the reset pulse stretcher.
6. The reset network (the resistor and two capacitors) protects the device against parasitic resets, especially in noisy environments.
7. In fact the filter is made to ignore all incoming pulses with short duration:
   - all negative spikes with a duration less than 150 ns are filtered
   - all trains of negative spikes with a ratio of 1/2 are filtered. This means that all spikes with a maximum duration of 150 ns with minimum interval between spikes of 75 ns are filtered.

   Data guaranteed by design, not tested in production.

SSP synchronous serial peripheral in slave mode (SPI or TI mode)

Subject to general operating conditions with $C_L \approx 45$ pF

Table 39. SSP slave mode characteristics(1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK}	SPI clock frequency		SSP0		2.66 MHz (f_{PLCK}/12)	MHz
			SSP1			
$t_{su(NSS)}$	NSS input setup time w.r.t SCK first edge		SSP0	0		ns
			SSP1	0		
$t_{h(NSS)}$	NSS input hold time w.r.t SCK last edge		SSP0	t_{PCLK}+15ns		
			SSP1	t_{PCLK}+15ns		
t_{NSSLQV}	NSS low to Data Output MISO valid time		SSP0	$2t_{PCLK}$	$3t_{PCLK}$+30 ns	
			SSP1	$2t_{PCLK}$	$3t_{PCLK}$+30 ns	
t_{NSSLQZ}	NSS low to Data Output MISO invalid time		SSP0	$2t_{PCLK}$	$3t_{PCLK}$+15 ns	
			SSP1	$2t_{PCLK}$	$3t_{PCLK}$+15 ns	
t_{SCKQV}	SCK trigger edge to data output MISO valid time		SSP0		15	
			SSP1		30	
t_{SCKQX}	SCK trigger edge to data output MISO invalid time		SSP0	$2t_{PCLK}$		
			SSP1	$2t_{PCLK}$		
$t_{su(MOSI)}$	MOSI setup time w.r.t SCK sampling edge		SSP0	0		
			SSP1	0		
$t_{h(MOSI)}$	MOSI hold time w.r.t SCK sampling edge		SSP0	$3t_{PCLK}$+15 ns		
			SSP1	$3t_{PCLK}$+15 ns		

1. Data based on characterisation results, not tested in production.

Figure 33. SPI configuration, slave mode with CPHA=0, single transfer

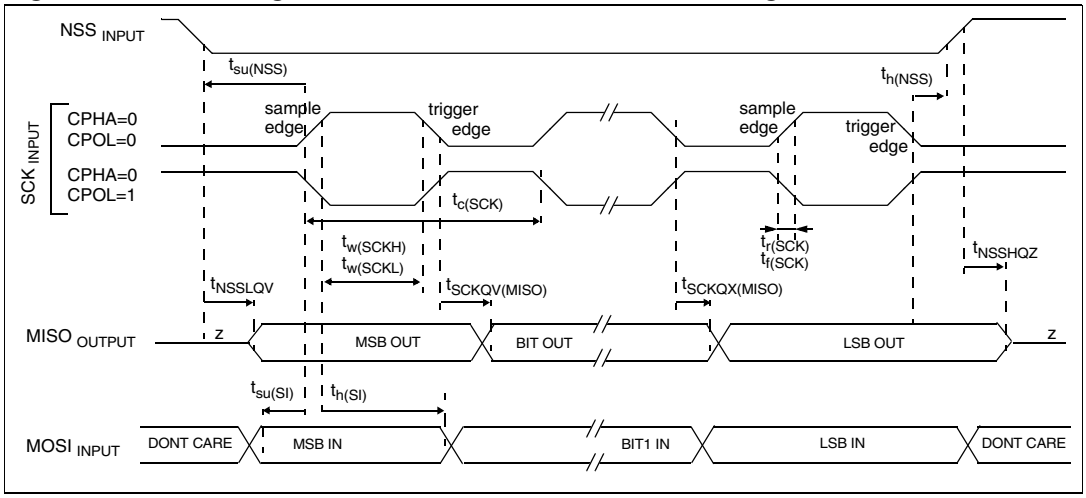


Figure 34. SPI configuration - slave mode with CPHA=0, continuous transfer

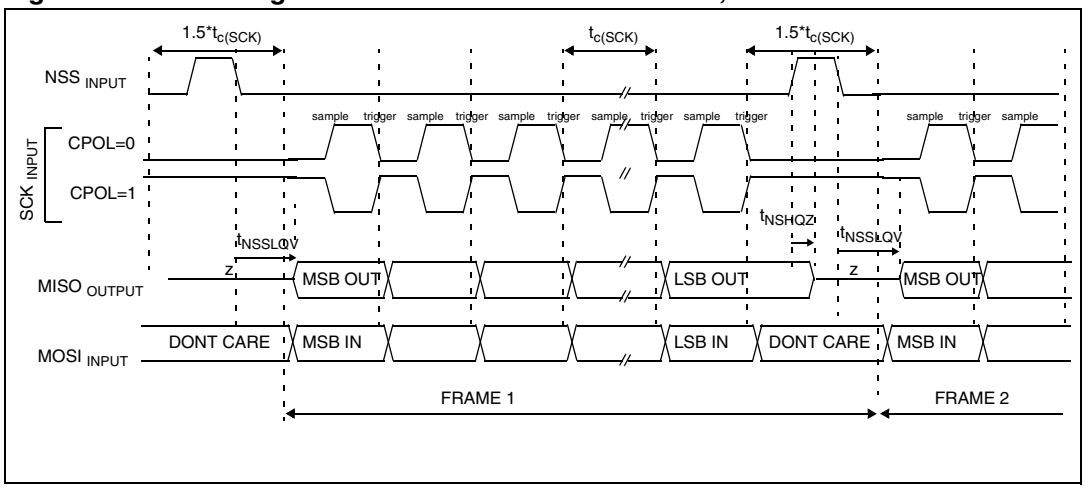


Figure 35. SPI configuration, slave mode with CPHA=1, single transfer

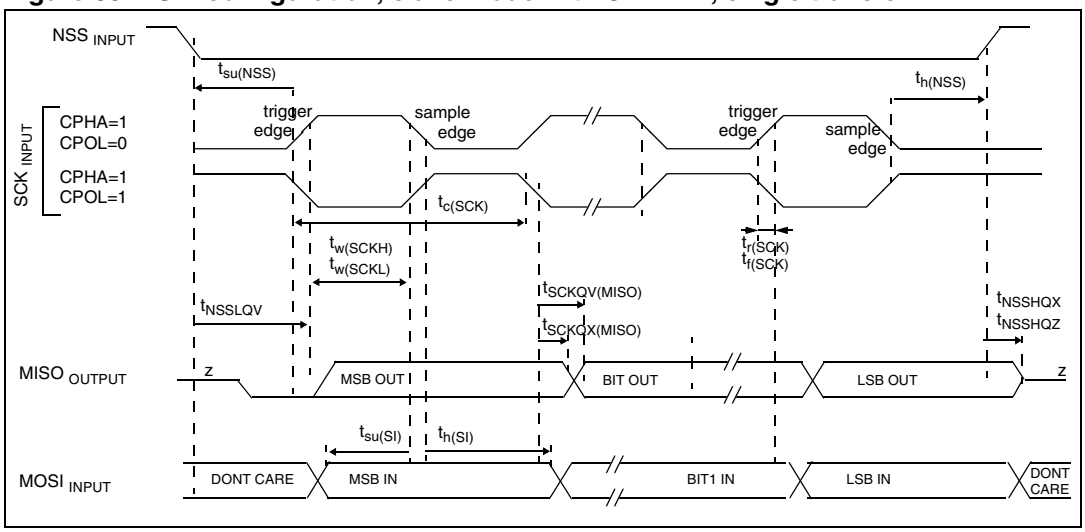
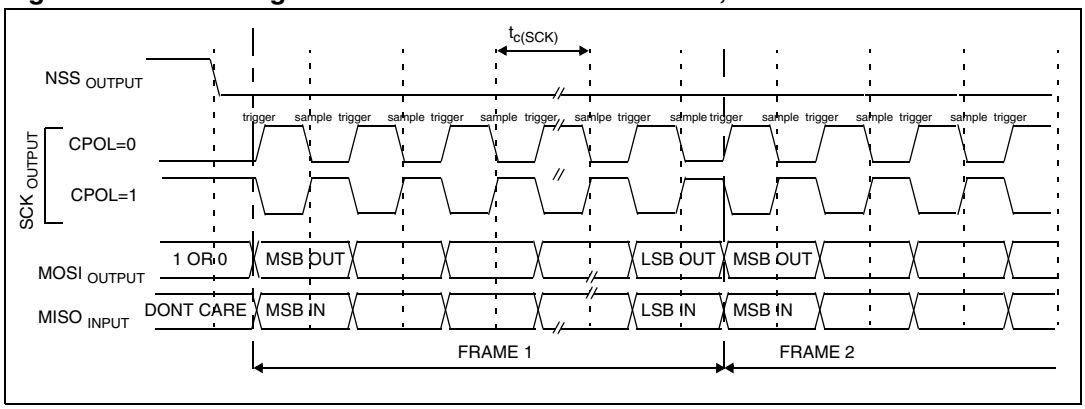


Figure 36. SPI configuration - slave mode with CPHA=1, continuous transfer



not possible to power off the STR7x while some another I^2C master node remains powered on: otherwise, the STR7x will be powered by the protection diode.

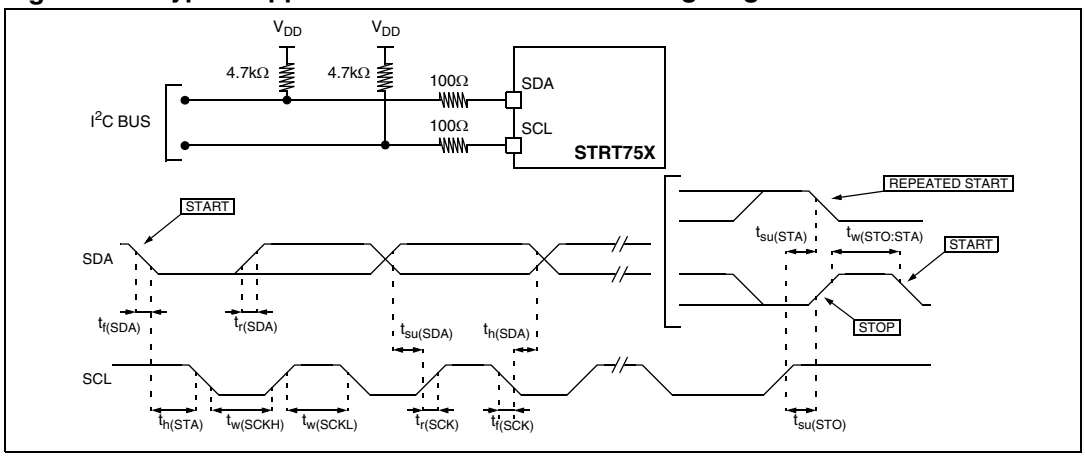
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 41. SDA and SCL characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20+0.1C_b	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20+0.1C_b	300	ns
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		µs
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. f_{PCLK}, must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
2. Data based on standard I^2C protocol requirement, not tested in production.
3. The maximum hold time $t_{h(SDA)}$ is not applicable
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 40. Typical application with I^2C bus and timing diagram



1. Measurement points are done at CMOS levels: 0.3xV_{DD} and 0.7xV_{DD}.

6.3.12 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA_ADC}, f_{PCLK}, and T_A unless otherwise specified.

Table 45. 10-bit ADC characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
f_{ADC}	ADC clock frequency		0.4		8	MHz
V_{AIN}	Conversion voltage range(2)		V_{SSA_ADC}		V_{DDA_ADC}	V
R_{AIN}	External input impedance(3)(4)				10	kΩ
C_{AIN}	External capacitor on analog input(3)(4)				6.8	pF
I_{lkg}	Induced input leakage current	+400 µA injected on any pin			1	µA
		-400 µA injected on any pin except specific adjacent pins in *Table 46*			1	µA
		-400µA injected on specific adjacent pins in *Table 46*		40		µA
C_{ADC}	Internal sample and hold capacitor			3.5		pF
t_{CAL}	Calibration Time	f_{CK_ADC}=8 MHz	725.25			µs
			5802			$1/f_{ADC}$
t_{CONV}	Total Conversion time (including sampling time)	f_{CK_ADC}=8 MHz	3.75			µs
			30 (11 for sampling + 19 for Successive Approximation)			$1/f_{ADC}$
I_{ADC}		Sunk on V_{DDA_ADC}		3.7		mA

1. Unless otherwise specified, typical data are based on T_A=25°C. They are given only as design guidelines and are not tested.
2. Calibration is needed once after each power-up.
3. $C_{PARASITIC}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
4. Depending on the input signal variation (f_{AIN}), C_{AIN} can be increased for stabilization time and reduced to allow the use of a larger serial resistor (R_{AIN}). It is valid for all f_{ADC} frequencies ≤ 8 MHz.

7.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 10: General operating conditions on page 34*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in ° C/W,
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$),
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum Power Dissipation on Output Pins.
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 48. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 100 - 14 x 14 mm / 0.5 mm pitch	46	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 100 - 10 x 10 x 1.7mm	41	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

8 Order codes

Table 49. Order codes

Order code	Flash Prog. Memory (Bank 0) Kbytes	Package	CAN Periph	USB Periph	Nominal Temp. Range (T_A)
STR750FV0T6	64	LQFP100 14x14	Yes	Yes	-40 to +85°C
STR750FV1T6	128				
STR750FV2T6	256				
STR750FV0H6	64	LFBGA100 10x10			
STR750FV1H6	128				
STR750FV2H6	256				
STR751FR0T6	64	LQFP64 10x10	-	Yes	-40 to +85°C
STR751FR1T6	128				
STR751FR2T6	256				
STR751FR0H6	64	LFBGA64 8x8			
STR751FR1H6	128				
STR751FR2H6	256				
STR752FR0T6	64	LQFP64 10x10	Yes	-	-40 to +85°C
STR752FR1T6	128				
STR752FR2T6	256				
STR752FR0H6	64	LFBGA64 8x8			
STR752FR1H6	128				
STR752FR2H6	256				
STR752FR0T7	64	LQFP64 10x10	Yes	-	-40 to +105°C
STR752FR1T7	128				
STR752FR2T7	256				
STR752FR0H7	64	LFBGA64 8x8			
STR752FR1H7	128				
STR752FR2H7	256				
STR755FR0T6	64	LQFP64 10x10	-	-	-40 to +85°C
STR755FR1T6	128				
STR755FR2T6	256				
STR755FR0H6	64	LFBGA64 8x8			
STR755FR1H6	128				
STR755FR2H6	256				