Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, SPI, SSI, SSP, UART/USART, USB
Peripherals	DMA, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str751fr1t6

Contents

Serial memory interface (SMI)

The Serial Memory interface is directly able to access up to 4 serial FLASH devices. It can be used to access data, execute code directly or boot the application from external memory. The memory is addressed as 4 banks of up to 16 Mbytes each.

Clocks and start-up

After RESET or when exiting from Low Power Mode, the CPU is clocked immediately by an internal RC oscillator (FREEOSC) at a frequency centered around 5 MHz, so the application code can start executing without delay. In parallel, the 4/8 MHz Oscillator is enabled and its stabilization time is monitored using a dedicated counter.

An oscillator failure detection is implemented: when the clock disappears on the XT1 pin, the circuit automatically switches to the FREEOSC oscillator and an interrupt is generated.

In Run mode, the AHB and APB clock speeds can be set at a large number of different frequencies thanks to the PLL and various prescalers: up to 60 MHz for AHB and up to 32 MHz for APB when fetching from Flash (64 MHz and 32 MHz when fetching from SRAM).

In SLOW mode, the AHB clock can be significantly decreased to reduce power consumption.

The built-in Clock Controller also provides the 48 MHz USB clock directly without any extra oscillators or PLL. For instance, starting from the 4 MHz crystal source, it is possible to obtain in parallel 60 MHz for the AHB clock, 48 MHz for the USB clock and 30 MHz for the APB peripherals.

Boot modes

At start-up, boot pins are used to select one of five boot options:

- Boot from internal flash
- Boot from external serial Flash memory
- Boot from internal boot loader
- Boot from internal SRAM

Booting from SMI memory allows booting from a serial flash. This way, a specific boot monitor can be implemented. Alternatively, the STR750F can boot from the internal boot loader that implements a boot from UART.

Power supply schemes

You can connect the device in any of the following ways depending on your application.

- **Power Scheme 1: Single external 3.3V power source**. In this configuration the V_{CORE} supply required for the internal logic is generated internally by the main voltage regulator and the V_{BACKUP} supply is generated internally by the low power voltage regulator. This scheme has the advantage of requiring only one 3.3V power source.
- **Power Scheme 2: Dual external 3.3V and 1.8V power sources.** In this configuration, the internal voltage regulators are switched off by forcing the VREG_DIS pin to high level. V_{CORE} is provided externally through the V_{18} and V_{18REG} power pins and V_{BACKUP} through the V_{18_BKP} pin. This scheme is intended to save power consumption for applications which already provide an 1.8V power supply.
- **Power Scheme 3: Single external 5.0V power source.** In this configuration the V_{CORE} supply required for the internal logic is generated internally by the main voltage

regulator and the V_{BACKUP} supply is generated internally by the low power voltage regulator. This scheme has the advantage of requiring only one 5.0V power source.

- **Power Scheme 4: Dual external 5.0V and 1.8V power sources.** In this configuration, the internal voltage regulators are switched off, by forcing the VREG_DIS pin to high level. V_{CORE} is provided externally through the V_{18} and V_{18REG} power pins and V_{BACKUP} through the V_{18_BKP} pin. This scheme is intended to provide 5V I/O capability.

Caution: When powered by 5.0V, the USB peripheral cannot operate.

Low power modes

The STR750F supports 5 low power modes, SLOW, PCG, WFI, STOP and STANDBY.

- SLOW MODE: the system clock speed is reduced. Alternatively, the PLL and the main oscillator can be stopped and the device is driven by a low power clock (f_{RTC}). The clock is either an external 32.768 kHz oscillator or the internal low power RC oscillator.
- PCG MODE (Peripheral Clock Gating MODE): When the peripherals are not used, their APB clocks are gated to optimize the power consumption.
- WFI MODE (Wait For Interrupts): only the CPU clock is stopped, all peripherals continue to work and can wake-up the CPU when IRQs occur.
- STOP MODE: all clocks/peripherals are disabled. It is also possible to disable the oscillators and the Main Voltage Regulator (In this case the V_{CORE} is entirely powered by V_{18_BKP}). This mode is intended to achieve the lowest power consumption with SRAM and registers contents retained. The system can be woken up by any of the external interrupts / wake-up lines or by the RTC timer which can optionally be kept running. The RTC can be clocked either by the 32.768 kHz Crystal or the Low Power RC Oscillator.
  Alternatively, STOP mode gives flexibility to keep the either main oscillator, or the Flash or the Main Voltage Regulator enabled when a fast start after wake-up is preferred (at the cost of some extra power consumption).
- STANDBY MODE: This mode (only available in single supply power schemes) is intended to achieve the lowest power consumption even when the temperature is increasing. The digital power supply (V_{CORE}) is completely removed (no leakage even at high ambient temperature). SRAM and all register contents are lost. Only the RTC remains powered by V_{18_BKP}. The STR750F can be switched back from STANDBY to RUN mode by a trigger event on the WKP_STDBY pin or an alarm timeout on the RTC counter.

Caution: It is important to bear in mind that it is forbidden to remove power from the V_{DD_IO} power supply in any of the Low Power Modes (even in STANDBY MODE).

DMA

The flexible 4-channel general-purpose DMA is able to manage memory to memory, peripheral to memory and memory to peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

The DMA can be used with the main peripherals: UART0, SSP0, Motor control PWM timer (PWM), standard timer TIM0 and ADC.

RTC (real-time clock)

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a

periodic interrupt. It is clocked by an external 32.768 kHz oscillator or the internal low power RC oscillator. The RC has a typical frequency of 300 kHz and can be calibrated.

WDG (watchdog timer)

The watchdog timer is based on a 16-bit downcounter and 8-bit prescaler. It can be used as watchdog to reset the device when a problem occurs, or as free running timer for application time out management.

Timebase timer (TB)

The timebase timer is based on a 16-bit auto-reload counter and not connected to the I/O pins. It can be used for software triggering, or to implement the scheduler of a real-time operating system.

Synchronizable standard timers (TIM2:0)

The three standard timers are based on a 16-bit auto-reload counter and feature up to 2 input captures and 2 output compares (for external triggering or time base / time out management). They can work together with the PWM timer via the Timer Link feature for synchronization or event chaining. In reset state, timer Alternate Function I/Os are connected to the same
I/O ports in both 64-pin and 100-pin devices. To optimize timer functions in 64-pin devices, timer Alternate Function I/Os can be connected, or “remapped”, to other I/O ports as summarized in *Table 3* and detailed in *Table 6*. This remapping is done by the application via a control register.

Table 3. Standard timer alternate function I/Os

Standard timer functions		Number of alternate function I/Os		
		100-pin package	64-pin package	
			Default mapping	Remapped
TIM 0	Input Capture	2	1	2
	Output Compare/PWM	2	1	2
TIM 1	Input Capture	2	1	1
	Output Compare/PWM	2	1	1
TIM 2	Input Capture	2	2	2
	Output Compare/PWM	2	1	2

Any of the standard timers can be used to generate PWM outputs. One timer (TIM0) is mapped to a DMA channel.

Motor control PWM timer (PWM)

The Motor Control PWM Timer (PWM) can be seen as a three-phase PWM multiplexed on 6 channels. The 16-bit PWM generator has full modulation capability (0...100%), edge or centre-aligned patterns and supports dead-time insertion. It has many features in common with the standard TIM timers which has the same architecture and it can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.The PWM timer is mapped to a DMA channel.

GPIOs (general purpose input/output)

Each of the 72 GPIO pins (38 GPIOs in 64-pin devices) can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as Peripheral Alternate Function. Port 1.15 is an exception, it can be used as general-purpose input only or wake-up from STANDBY mode (WKP_STDBY). Most of the GPIO pins are shared with digital or analog alternate functions.

Figure 12. Power consumption measurements in power scheme 1 (regulators enabled)

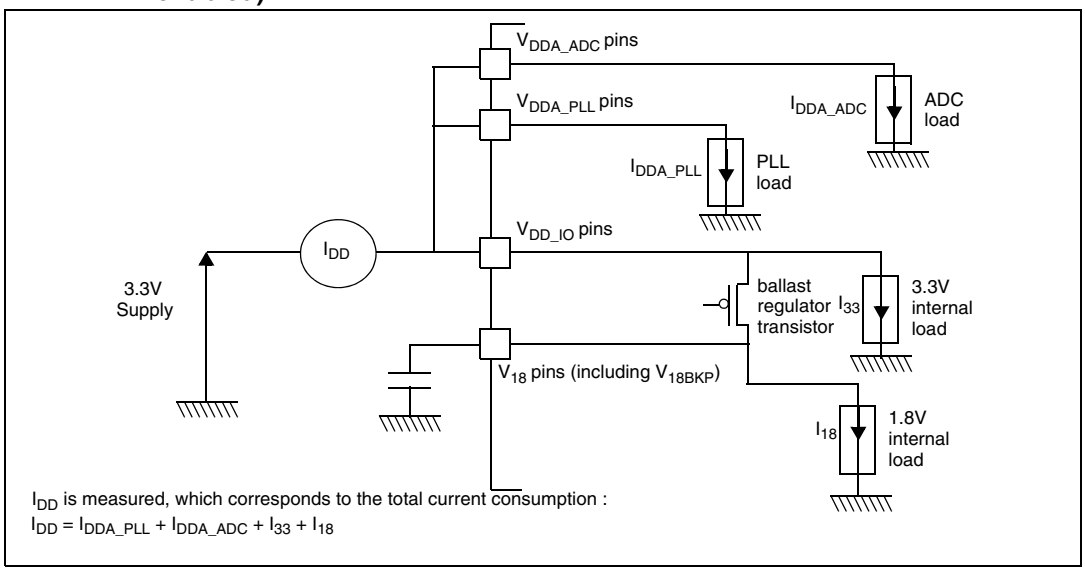


Figure 13. Power consumption measurements in power scheme 2 (regulators disabled)

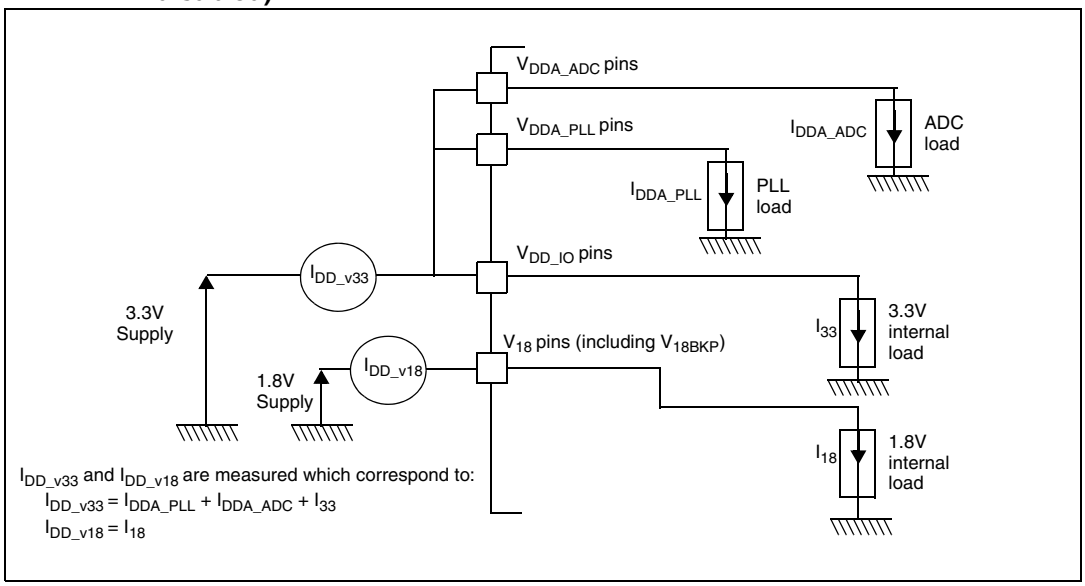


Figure 16. Power consumption in STOP mode in Single supply scheme (3.3 V range)

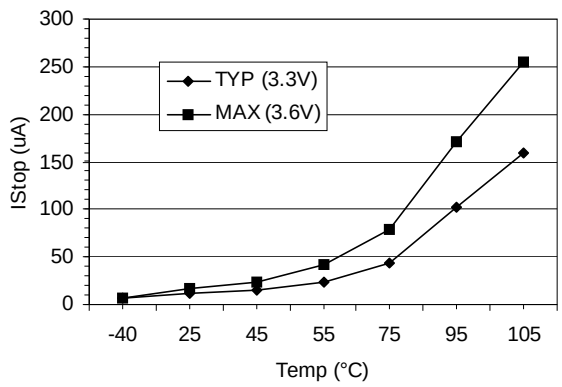


Figure 17. Power consumption in STOP mode Single supply scheme (5 V range)

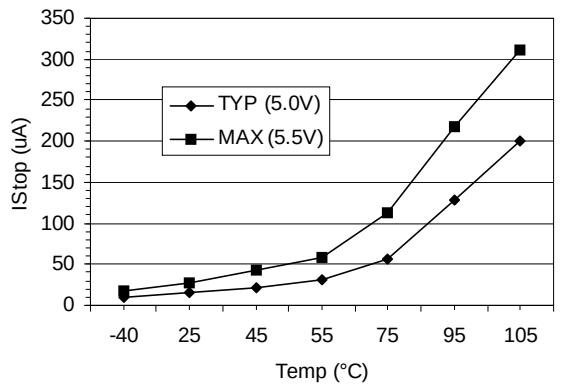


Figure 18. Power consumption in STANDBY mode (3.3 V range)

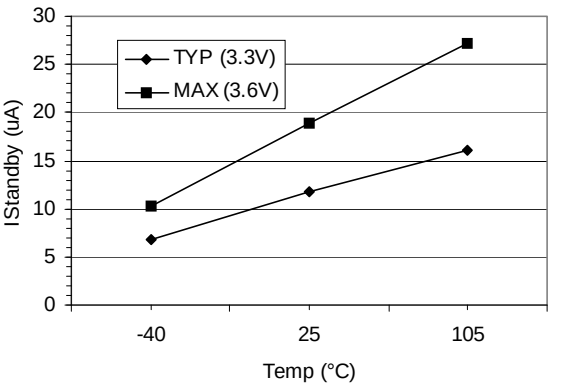
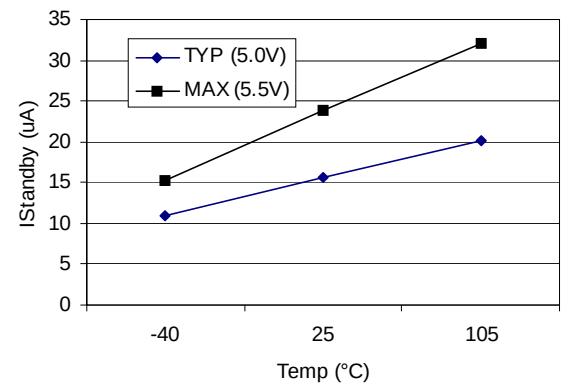


Figure 19. Power consumption in STANDBY mode (5 V range)



Subject to general operating conditions for V_{DD_IO}, and T_A

Table 15. Single supply typical power consumption in Run, WFI, Slow and Slow-WFI modes

Symbol	Para meter	Conditions	3.3V typ(1)	5V typ(2)	Unit
I_{DD} (3)	Supply current in RUN mode(4)	Clocked by OSC4M with PLL multiplication, all peripherals enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz f_{HCLK}=56 MHz, f_{PCLK}=28 MHz f_{HCLK}=48 MHz, f_{PCLK}=24 MHz f_{HCLK}=32 MHz, f_{PCLK}=32 MHz f_{HCLK}=16 MHz, f_{PCLK}=16 MHz f_{HCLK}=8 MHz, f_{PCLK}=8 MHz	 80 75 65 59 34 20	 82 77 67 61 37 22	mA
		Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz f_{HCLK}=56 MHz, f_{PCLK}=28 MHz f_{HCLK}=48 MHz, f_{PCLK}=24 MHz f_{HCLK}=32 MHz, f_{PCLK}=32 MHz f_{HCLK}=16 MHz, f_{PCLK}=16 MHz f_{HCLK}=8 MHz, f_{PCLK}=8 MHz	 65 60 54 42 22 16	 67 62 55 44 24 18	mA
	Supply current in WFI mode(4)	Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz(5) f_{HCLK}=56 MHz, f_{PCLK}=28 MHz(5) f_{HCLK}=48 MHz, f_{PCLK}=24 MHz(5) f_{HCLK}=32 MHz, f_{PCLK}=32 MHz(6) f_{HCLK}=16 MHz, f_{PCLK}= 16 MHz (6) f_{HCLK}= 8 MHz, f_{PCLK}= 8 MHz(6)	 62 59 53 22 13 10	 63 60 54 23 15 11	mA
	Supply current in SLOW mode(4)	Clocked by FREEOSC: f_{HCLK}=f_{PCLK}=~5 MHz, Clocked by OSC4M: f_{HCLK}=f_{PCLK}=4 MHz Clocked by LPOSC: f_{HCLK}=f_{PCLK}=~300 kHz Clocked by OSC32K: f_{HCLK}=f_{PCLK}=32.768 kHz	9 8 3.65 3.5	10 9 3.9 4.2	mA
	Supply current in SLOW-WFI mode(4)(7)	Clocked by FREEOSC: f_{HCLK}=f_{PCLK}=~5 MHz Clocked by OSC4M: f_{HCLK}=f_{PCLK}=4 MHz Clocked by LPOSC: f_{HCLK}=f_{PCLK}=~300 kHz Clocked by OSC32K: f_{HCLK}=f_{PCLK}=32.768 kHz	3.5 3.1 1.15 0.98	4.0 3.75 1.65 1.5	mA

1. Typical data based on T_A=25° C and V_{DD_IO}=3.3V.
2. Typical data based on T_A=25° C and V_{DD_IO}=5.0V.
3. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4 on page 36*.
4. Single supply scheme see *Figure 14*.
5. Parameter setting BURST=1, WFI_FLASHEN=1
6. Parameter setting BURST=0, WFI_FLASHEN=0
7. Parameter setting WFI_FLASHEN=0, OSC4MOFF=1

6.3.6 Memory characteristics

Flash memory

Subject to general operating conditions for V_{DD_IO} and V_{18}, T_A = -40 to 105 °C unless otherwise specified.

Table 26. Flash memory characteristics

Symbol	Parameter	Test Conditions	Value		Unit
			Typ	Max(1)	
t_{PW}	Word Program		35		µs
t_{PDW}	Double Word Program		60		µs
t_{PB0}	Bank 0 Program (256K)	Single Word programming of a checker-board pattern	2	4.9(2)	s
t_{PB1}	Bank 1 Program (16K)	Single Word programming of a checker-board pattern	125	224(2)	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed (all 1) Preprogrammed (all 0)	1.54 1.176	2.94(2) 2.38(2)	s
t_{ES}	Sector Erase (8K)	Not preprogrammed (all 1) Preprogrammed (all 0)	392 343	560(2) 532(2)	ms
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed (all 1) Preprogrammed (all 0)	8.0 6.6	13.7 11.2	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed (all 1) Preprogrammed (all 0)	0.9 0.8	1.5 1.3	s
t_{RPD}	Recovery when disabled			20	µs
t_{PSL}	Program Suspend Latency			10	µs
t_{ESL}	Erase Suspend Latency			300	µs

1. Data based on characterisation not tested in production
2. 10K program/erase cycles.

Table 27. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END_B0}	Endurance (Bank 0 sectors)		10			kcycles
N_{END_B1}	Endurance (Bank 1 sectors)		100			kcycles
Y_{RET}	Data Retention	T_A=85° C	20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

1. Data based on characterisation not tested in production.

Table 33. Output driving current

I/O Output drive characteristics for V_{DD_IO} = 3.0 to 3.6 V and EN33 bit =1 or V_{DD_IO} = 4.5 to 5.5 V and EN33 bit =0						
I/O Type	**Symbol**	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
O2	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+2 mA		0.4	V
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-2 mA	V_{DD_IO}-0.8		
O4	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+4 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-4 mA	V_{DD_IO}-0.8		
O8	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+8 mA		0.4	
		Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time	I_{IO}=+20 mA, $T_A \leq 85°C$ $T_A \geq 85°C$		1.3 1.5	
			I_{IO}=+8 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-8 mA	V_{DD_IO}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS_IO}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD_IO}.

6.3.9 TB and TIM timer characteristics

Subject to general operating conditions for V_{DD_IO}, f_{CK_SYS}, and T_A unless otherwise specified.

Refer to *Section 6.3.8: I/O port pin characteristics on page 54* for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

Table 36. TB and TIM timers

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time	TIM0,1,2		2			t_{CK_TIM}
$t_{res(TIM)}$	Timer resolution time(1)	TB	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	16.6(1)			ns
		TIM0,1,2	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60MHz	16.6(1)			ns
f_{EXT}	Timer external clock frequency on TI1 or TI2	TIM0,1,2	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	0		$f_{CK\_TIM}/4$	MHz
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0		15	MHz
Res_{TIM}	Timer resolution					16	bit
$t_{COUNTER}$	16-bit Counter clock period when internal clock is selected (16-bit Prescaler)	TB		1		65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0.0166		1092	µs
		TIM0,1,2		1		65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0.0166		1092	µs
t_{MAX_COUNT}	Maximum Possible Count	TB				65536x65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s
		TIM0,1,2				65536x65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s

1. Take into account the frequency limitation due to the I/O speed capability when outputting the PWM to I/O pin, described in *: Output speed on page 57*.

Figure 28. SPI configuration - master mode, single transfer

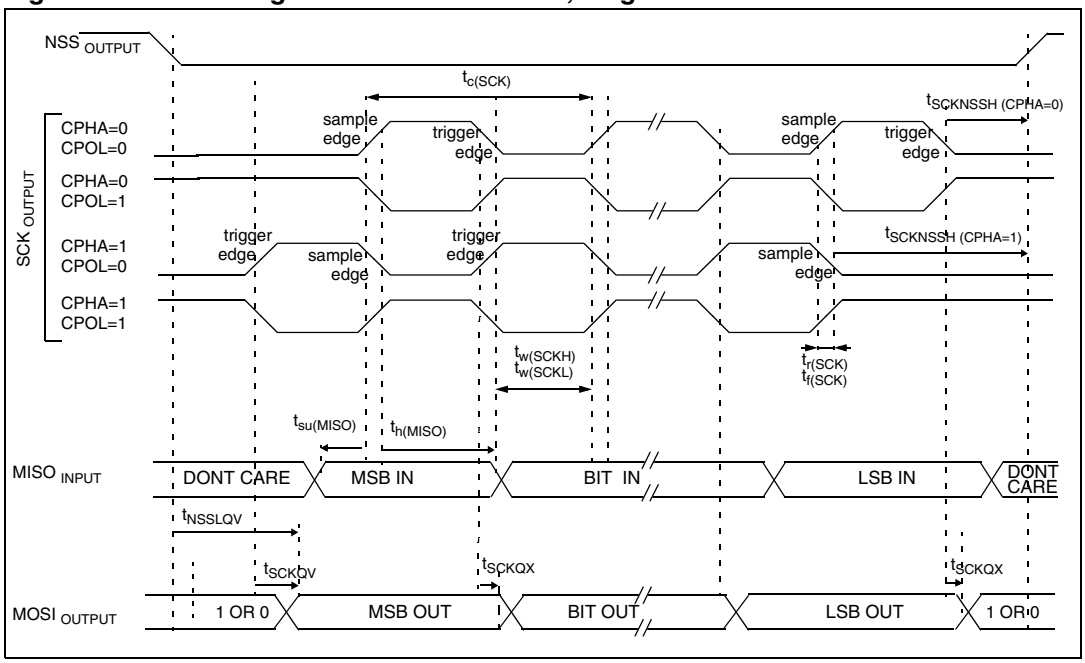


Figure 29. SPI configuration - master mode, continuous transfer, CPHA=0

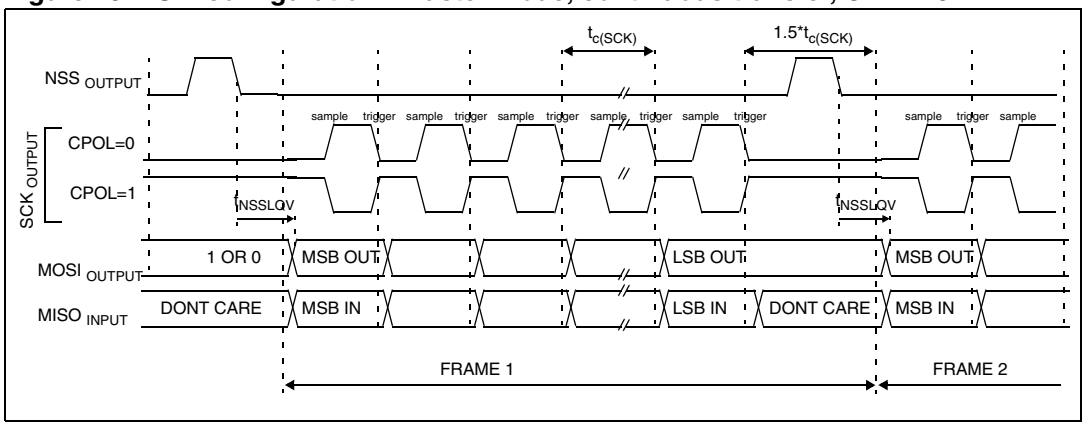


Figure 30. SPI configuration - master mode, continuous transfer, CPHA=1

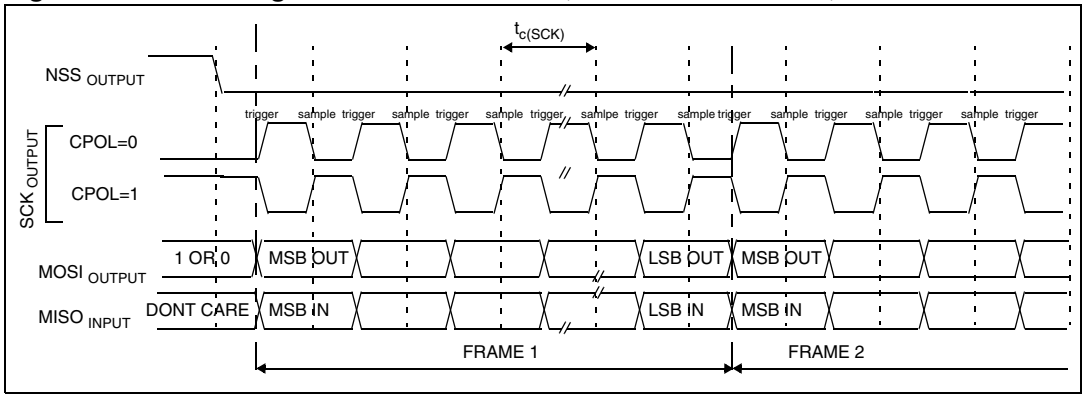


Figure 31. TI configuration - master mode, single transfer

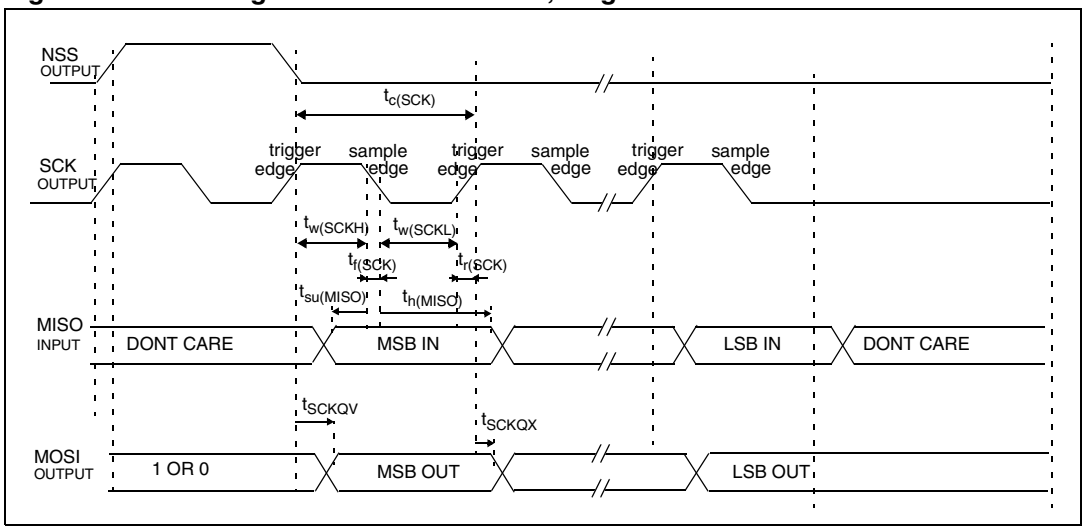
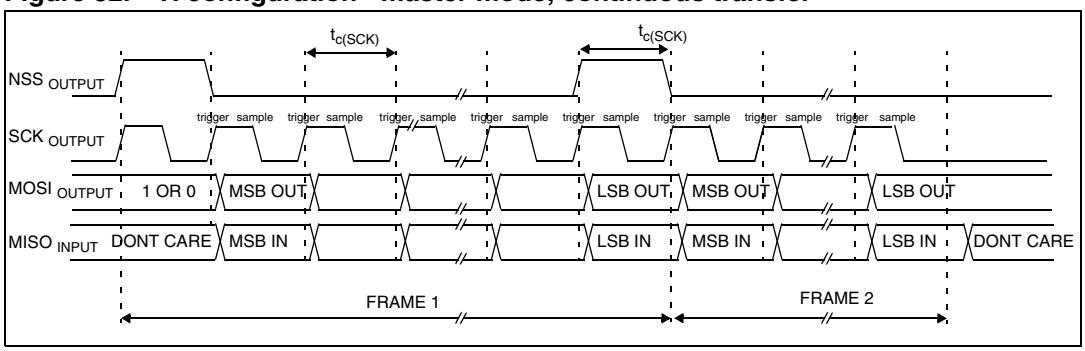


Figure 32. TI configuration - master mode, continuous transfer



6.3.11 USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 42. USB startup time

Symbol	Parameter	Conditions	Max	Unit
$t_{STARTUP}$	USB transceiver startup time		1	µs

Table 43. USB characteristics

USB DC Electrical Characteristics					
Symbol	**Parameter**	**Conditions**	**Min.(1)(2)**	**Max.(1)(2)**	**Unit**
Input Levels					
V_{DI}	Differential Input Sensitivity	I(DP, DM)	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	
V_{SE}	Single Ended Receiver Threshold		1.3	2.0	
Output Levels					
V_{OL}	Static Output Level Low	R_L of 1.5 kΩ to 3.6V(3)		0.3	V
V_{OH}	Static Output Level High	R_L of 15 kΩ to V_{SS}(3)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. It is important to be aware that the DP/DM pins are not 5 V tolerant. As a consequence, in case of a a shortcut with Vbus (typ: 5.0V), the protection diodes of the DP/DM pins will be direct biased . This will not damage the device if not more than 50 mA is sunk for longer than 24 hours but the reliability may be affected.
3. R_L is the load connected on the USB drivers

Figure 41. USB: data signal rise and fall time

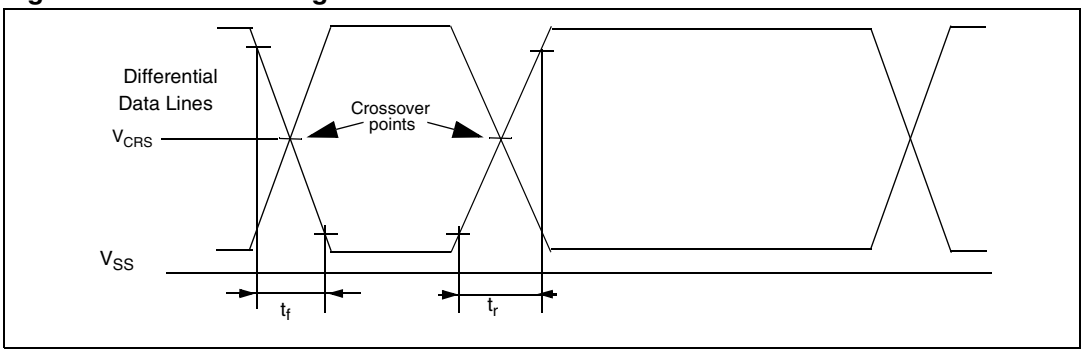


Table 44. USB: Full speed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Driver characteristics:					
t_r	Rise time(1)	C_L=50 pF	4	20	ns
t_f	Fall Time1)	C_L=50 pF	4	20	ns

General PCB design guidelines

To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 µF and optionally, if needed 10 pF capacitors as close as possible to the STR7 power supply pins and a 1 to 10 µF capacitor close to the power source (see *Figure 43*).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{DDA_ADC} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs near the A/D input being converted.

Software filtering of spurious conversion results

For EMC performance reasons, it is recommended to filter A/D conversion outliers using software filtering techniques.

Figure 43. Power supply filtering

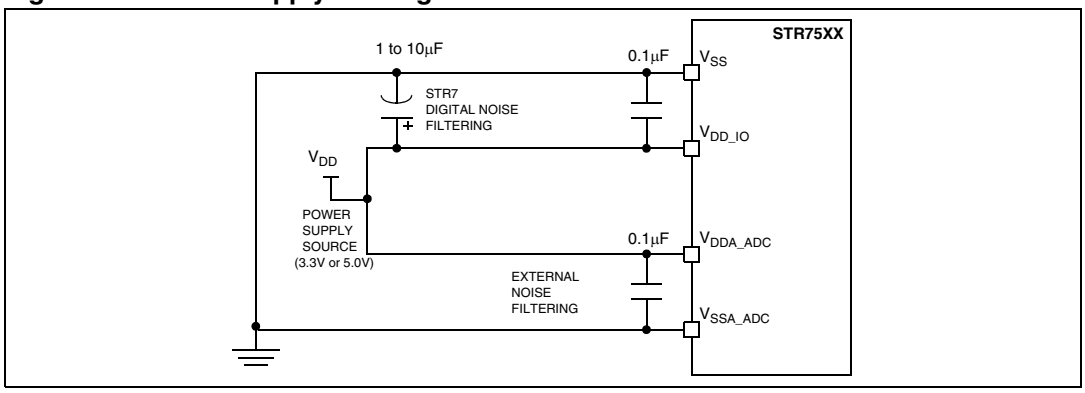
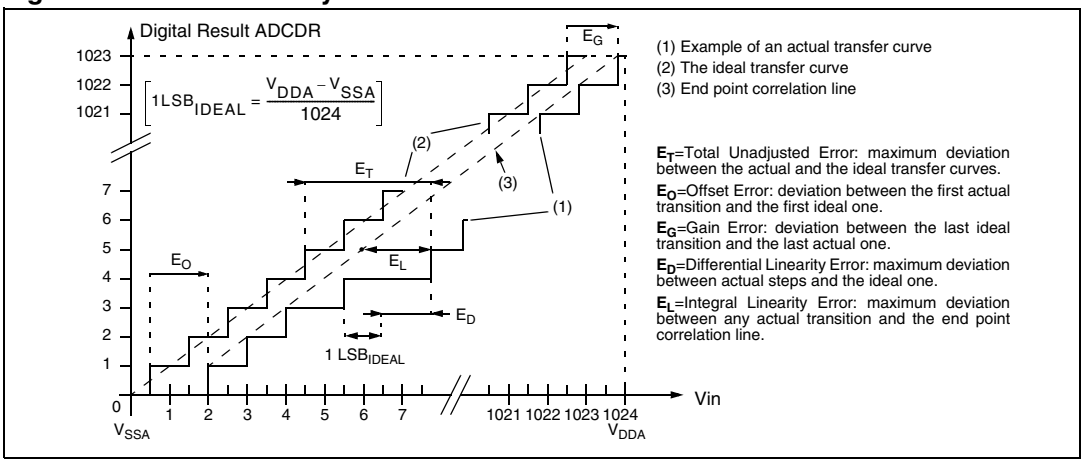


Table 47. ADC accuracy

ADC accuracy with f_{CK_SYS} = 20 MHz, f_{ADC}=8 MHz, R_{AIN} < 10 kΩ This assumes that the ADC is calibrated(1)					
Symbol	**Parameter**	**Conditions**	**Typ**	**Max**	**Unit**
$\|E_T\|$	Total unadjusted error (2) (3)	V_{DDA_ADC}=3.3 V	1	1.2	LSB
		V_{DDA_ADC}=5.0 V	1	1.2	
$\|E_O\|$	Offset error(2) (3)	V_{DDA_ADC}=3.3 V	0.15	0.5	
		V_{DDA_ADC}=5.0 V	0.15	0.5	
E_G	Gain Error (2) (3)	V_{DDA_ADC}=3.3 V	-0.8	-0.2	
		V_{DDA_ADC}=5.0 V	-0.8	-0.2	
$\|E_D\|$	Differential linearity error(2) (3)	V_{DDA_ADC}=3.3 V	0.7	0.9	
		V_{DDA_ADC}=5.0 V	0.7	0.9	
$\|E_L\|$	Integral linearity error (2) (3)	V_{DDA_ADC}=3.3 V	0.6	0.8	
		V_{DDA_ADC}=5.0 V	0.6	0.8	

1. Calibration is needed once after each power-up.
2. Refer to *ADC accuracy vs. negative injection current on page 73*
3. ADC Accuracy vs. MCO (Main Clock Output): the ADC accuracy can be significantly degraded when activating the MCO on pin P0.01 while converting an analog channel (especially those which are close to the MCO pin). To avoid this, when an ADC conversion is launched, it is strongly recommended to disable the MCO.

Figure 44. ADC accuracy characteristics



7.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 10: General operating conditions on page 34*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in ° C/W,
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$),
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum Power Dissipation on Output Pins.
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 48. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 100 - 14 x 14 mm / 0.5 mm pitch	46	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 100 - 10 x 10 x 1.7mm	41	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

Table 49. Order codes (continued)

Order code	Flash Prog. Memory (Bank 0) Kbytes	Package	CAN Periph	USB Periph	Nominal Temp. Range (T_A)
STR755FV0T6	64	LQFP100 14x14	-	-	-40 to +85°C
STR755FV1T6	128				
STR755FV2T6	256				
STR755FV0H6	64	LFBGA100 10x10			
STR755FV1H6	128				
STR755FV2H6	256				

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com