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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, SPI, SSI, SSP, UART/USART, USB
Peripherals	DMA, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str751fr2t6

I²C bus

The I²C bus interface can operate in multi-master and slave mode. It can support standard and fast modes (up to 400KHz).

High speed universal asynch. receiver transmitter (UART)

The three UART interfaces are able to communicate at speeds of up to 2 Mbit/s. They provide hardware management of the CTS and RTS signals and have LIN Master capability.

To optimize the data transfer between the processor and the peripheral, two FIFOs (receive/transmit) of 16 bytes each have been implemented.

One UART can be served by the DMA controller (UART0).

Synchronous serial peripheral (SSP)

The two SSPs are able to communicate up to 8 Mbit/s (SSP1) or up to 16 Mbit/s (SSP0) in standard full duplex 4-pin interface mode as a master device or up to 2.66 Mbit/s as a slave device. To optimize the data transfer between the processor and the peripheral, two FIFOs (receive/transmit) of 8 x 16 bit words have been implemented. The SSPs support the Motorola SPI or TI SSI protocols.

One SSP can be served by the DMA controller (SSP0).

Controller area network (CAN)

The CAN is compliant with the specification 2.0 part B (active) with a bit rate up to 1Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Up to 32 message objects are handled through an internal RAM buffer. In LQFP64 devices, CAN and USB cannot be connected simultaneously.

Universal serial bus (USB)

The STR750F embeds a USB device peripheral compatible with the USB Full speed 12Mbs. The USB interface implements a full speed (12 Mbit/s) function interface. It has software configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock source is generated from the internal main PLL. V_{DD} must be in the range 3.3V±10% for USB operation.

ADC (analog to digital converter)

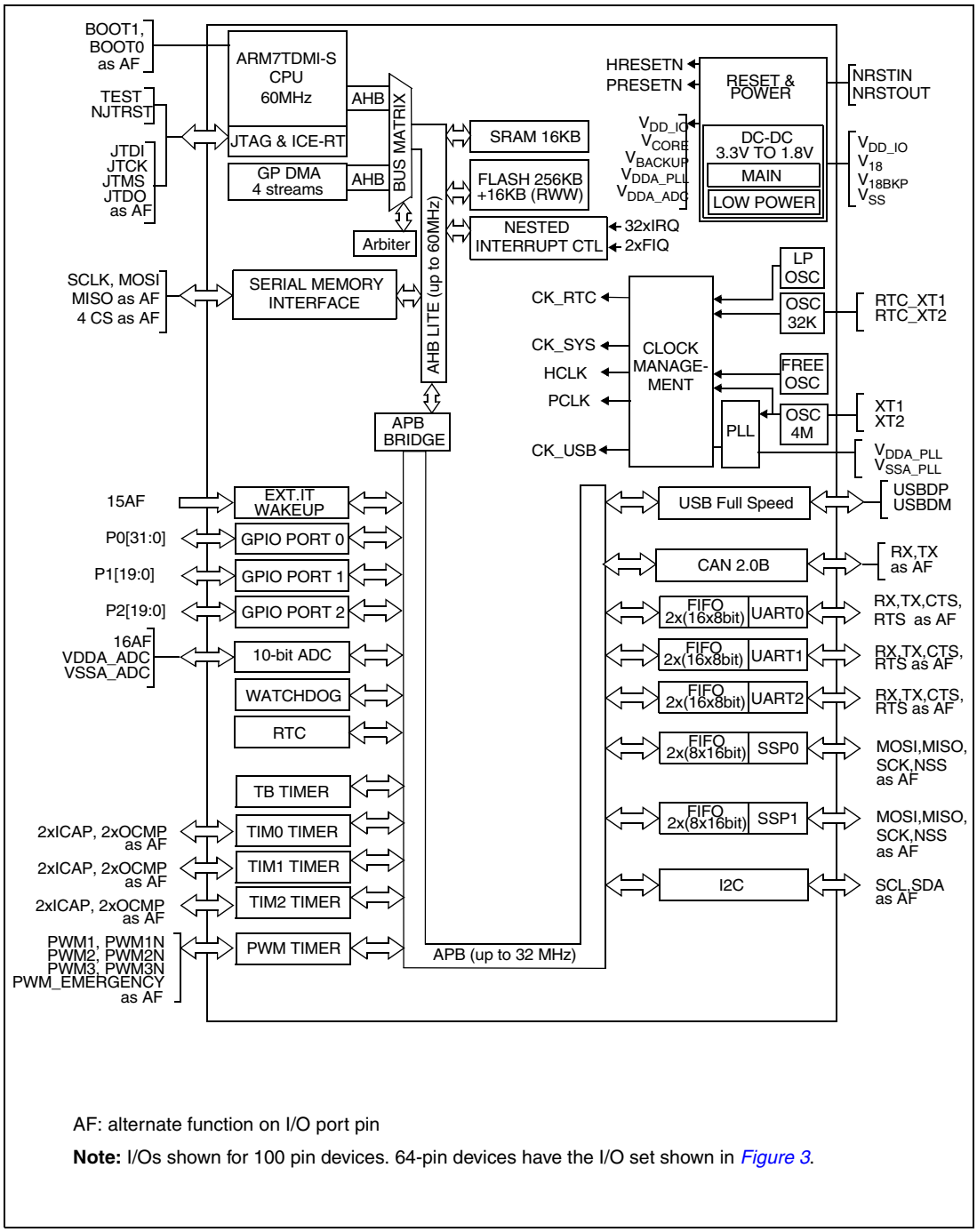
The 10-bit Analog to Digital Converter, converts up to 16 external channels (11 channels in 64-pin devices) in single-shot or scan modes. In scan mode, continuous conversion is performed on a selected group of analog inputs. The minimum conversion time is 3.75 µs (including the sampling time).
The ADC can be served by the DMA controller.

An analog watchdog feature allows you to very precisely monitor the converted voltage of up to four channels. An IRQ is generated when the converted voltage is outside the programmed thresholds.

The events generated by TIM0, TIM2 and PWM timers can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

3.2 Block diagram

Figure 1. STR750 block diagram



AF: alternate function on I/O port pin

Note: I/Os shown for 100 pin devices. 64-pin devices have the I/O set shown in *Figure 3*.

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
7	D1	5	D1	P0.29 / TIM1_TI1 / ADC_IN8	I/O	T_T	**X**	X		O2	X	X		**Port 0.29**	TIM1: Input Capture 1	ADC: Analog input 8
8	E1	6	D2	P0.28 / TIM1_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 0.28**	TIM1: Output Compare 1	
9	E5	7	D3	TEST	I									Reserved, must be tied to ground		
10	E4	8	D4	VSS_IO	S									Ground Voltage for digital I/Os		
11	E2			P0.23 / UART1_RTS / ADC_IN6	I/O	T_T	**X**	X		O2	X	X		**Port 0.23**	UART1: Ready To Send output(4)	ADC analog input 6
12	F5			P2.04 / TIM2_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 2.04**	TIM2: Output Compare 1(4)	
13	F1			P2.03 / UART1_RTS	I/O	T_T	**X**	X		O2	X	X		**Port 2.03**	UART1: Ready To Send output(4)	
14	F4			P2.02	I/O	T_T	**X**	X		O2	X	X		**Port 2.02**		
15	E3			P0.22 / UART1_CTS / ADC_IN5	I/O	T_T	**X**	X		O2	X	X		**Port 0.22**	UART1: Clear To Send input	ADC: Analog input 5
16	F2	9	E4	P0.21 / UART1_TX	I/O	T_T	**X**	X		O2	X	X		**Port 0.21**	UART1: Transmit data output (remappable to P0.15)(4)	
17	F3	10	E3	P0.20 / UART1_RX	I/O	T_T	**X**	X		O2	X	X		**Port 0.20**	UART1: Receive data input (remappable to P0.14)(4)	
18	G3	11	E2	P1.19 / JTMS	I/O	T_T	X	X		O2	X	X		**JTAG mode selection input(6)**	Port 1.19	
19	G2	12	E1	P1.18 / JTCK	I/O	T_T	X	X		O2	X	X		**JTAG clock input(6)**	Port 1.18	
20	H3	13	F4	P1.17 / JTDO	I/O	T_T	X	X		O8	X	X		**JTAG data output(6)**	Port 1.17	
21	H2	14	F3	P1.16 / JTDI	I/O	T_T	X	X		O2	X	X		**JTAG data input(6)**	Port 1.16	
22	G1	15	F2	NJTRST	I	T_T								JTAG reset input(5)		
23	G4			P2.01	I/O	T_T	**X**	X		O2	X	X		**Port 2.01**		
24	G5			P2.00	I/O	T_T	**X**	X		O2	X	X		**Port 2.00**		
25	H1	16	F1	P0.13 / RTCK / UART0_RTS UART2_TX	I/O	T_T	X	X		O8	X	X		**JTAG return clock output(6)**	Port 0.13 / UART0: Ready To Send output(4)	UART2: Transmit Data output (when remapped)(8)

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP			
43	H9			P2.16	I/O	T_T	X	X		O2	X	X		**Port 2.16**	
44	J9	27	G5	VDD_IO	S									Supply voltage for digital I/Os	
45	K9	28	G7	VDDA_PLL	S									Supply voltage for PLL	
46	K8	29	H7	XT2										4 MHz main oscillator	
47	K7	30	H8	XT1											
48	J10	31	G6	VSS_IO	S									Ground voltage for digital I/Os	
49	K10	32	G8	VSSA_PLL	S									Ground voltage for PLL	
50	J8			P2.15	I/O	T_T	X	X		O2	X	X		**Port 2.15**	
51	H8			P2.14	I/O	T_T	X	X		O2	X	X		**Port 2.14**	
52	G8	33	F5	V18REG	S									Stabilization for main voltage regulator. Requires external capacitors of at least 10µF between V18REG and VSS18. See *Figure 4.2*. To be connected to the 1.8V external power supply when embedded regulators are not used,	
53	F8	34	F6	VSS18	S									Ground Voltage for the main voltage regulator	
54	F9	35	F7	VSSBKP	S									Stabilization for low power voltage regulator.	
55	G9	36	E7	V18BKP	S									Ground Voltage for the low power voltage regulator. Requires external capacitors of at least 1µF between V18BKP and VSSBKP. See *Figure 4.2*. To be connected to the 1.8V external power supply when embedded regulators are not used,	
56	H10	37	F8	XRTC1									X	32 kHz oscillator for Realtime Clock	
57	G10	38	E8	XRTC2									X		
58	E7	39	E5	NRSTOUT	O								X	Reset output	
59	E9	40	E6	NRSTIN	I	T_T							X	Reset input	
60	D6			P1.15 / WKP_STDBY	I	T_T	X		EIT15				X	**Port 1.15**	Wake-up from STANDBY input pin
61	B8			P2.13	I/O	T_T	X	X		O2	X	X		**Port 2.13**	
62	D9			P2.12	I/O	T_T	X	X		O2	X	X		**Port 2.12**	
63	F10	41 (7)	D8 (7)	P0.15 / CAN_TX	I/O	T_T	X	X		O2	X	X		**Port 0.15**	CAN: Transmit data output
64	E10	42 (7)	C8 (7)	P0.14 / CAN_RX	I/O	T_T	X	X	EIT5	O2	X	X		**Port 0.14**	CAN: Receive data input
65	D10	41 (7)	D8 (7)	USB_DN	I/O									USB: bidirectional data (data -)	
66	C10	42 (7)	C8 (7)	USB_DP	I/O									USB: bidirectional data (data +)	
67	B9	43	B8	P1.03 / TIM2_TI2	I/O	T_T	X	X		O2	X	X		**Port 1.03**	TIM2: Input Capture / trigger / external clock 2 (remappable to P0.07)(8)

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
68	A10			P1.02 / TIM2_OC2	I/O	T_T	X	X		O2	X	X		**Port 1.02**	TIM2: Output compare 2 (remappable to P0.06)(8)	
69	D7	44	C6	VDD_IO	S									Supply Voltage for digital I/Os		
70	D8	45	D6	VDDA_ADC	S									Supply Voltage for A/D converter		
71	C9			P2.11	I/O	T_T	X	X		O2	X	X		**Port 2.11**		
72	B10			P2.10	I/O	T_T	X	X		O2	X	X		**Port 2.10**		
73	C8	46	D7	VSSA_ADC	S									Ground Voltage for A/D converter		
74	C7	47	C7	VSS_IO	S									Ground Voltage for digital I/Os		
75	E8	48	D5	VREG_DIS	I	T_T								Voltage Regulator Disable input		
76	A9	49	A8	P0.07 / SMI_DOUT / SSP0_MOSI	I/O	T_T	X	X	EIT2	O4	X	X		**Port 0.07**	Serial Memory Interface: data output	SSP0: Master out Slave in data
77	A8	50	A7	P0.06 / SMI_DIN / SSP0_MISO	I/O	T_T	X	X		O4	X	X		**Port 0.06**	Serial Memory Interface: data input	SSP0: Master in Slave out data
78	A7	51	A6	P0.05 / SSP0_SCLK / SMI_CK	I/O	T_T	X	X	EIT1	O4	X	X		**Port 0.05**	SSP0: Serial clock	Serial Memory Interface: Serial clock output
79	B7	52	B6	P0.04 / SMI_CS0 / SSP0_NSS	I/O	T_T	X	X		O4	X	X		**Port 0.04**	Serial Memory Interface: chip select output 0	SSP0: Slave select input
80	C5	53	B7	P1.10 PWM_EMERGENCY	I/O	T_T	X	X	EIT10	O2	X	X		**Port 1.10**	PWM: Emergency input	
81	B6	54	B5	P1.09 / PWM1	I/O	T_T	X	X	EIT9	O4	X	X		**Port 1.09**	PWM: PWM1 output	
82	C6			P2.09 / PWM1N	I/O	T_T	X	X		O2	X	X		**Port 2.09**	PWM: PWM1 complementary output(4)	
83	G7			P2.08 / PWM2	I/O	T_T	X	X		O2	X	X		**Port 2.08**	PWM: PWM2 output(4)	
84	G6			P2.07 / PWM2N	I/O	T_T	X	X		O2	X	X		**Port 2.07**	PWM: PWM2 complementary output(4)	
85	F7			P2.06 / PWM3	I/O	T_T	X	X		O2	X	X		**Port 2.06**	PWM: PWM3 output(4)	
86	F6			P2.05 / PWM3N	I/O	T_T	X	X		O2	X	X		**Port 2.05**	PWM: PWM3 complementary output(4)	
87	A6	55	A5	P1.08 / PWM1N / ADC_IN11	I/O	T_T	X	X		O4	X	X		**Port 1.08**	PWM: PWM1 complementary output(8)	ADC: analog input 11
88	B5	56	B4	P1.07 / PWM2	I/O	T_T	X	X	EIT8	O4	X	X		**Port 1.07**	PWM: PWM2 output(4)	
89	A5	57	A4	P1.06 / PWM2N / ADC_IN10	I/O	T_T	X	X		O4	X	X		**Port 1.06**	PWM: PWM2 complementary output(4)	ADC: analog input 10
90	B4	58	B3	P1.05 / PWM3	I/O	T_T	X	X	EIT7	O4	X	X		**Port 1.05**	PWM: PWM3 output(4)	

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
91	A4	59	A3	P1.04 / PWM3N / ADC_IN9	I/O	T_T	**X**	X		O4	X	X		**Port 1.04**	PWM: PWM3 complementary output(4)	ADC: analog input 9
92	A3			P1.14 / ADC_IN15	I/O	T_T	**X**	X		O8	X	X		**Port 1.14**	ADC: analog input 15	
93	A2			P1.13 / ADC_IN14	I/O	T_T	**X**	X	EIT13	O8	X	X		**Port 1.13**	ADC: analog input 14	
94	D5			P1.01 / TIM0_TI2	I/O	T_T	**X**	X		O2	X	X		**Port 1.01**	TIM0: Input Capture / trigger / external clock 2 (remappable to P0.05)(8)	
95	E6			P1.00 / TIM0_OC2	I/O	T_T	**X**	X		O2	X	X		**Port 1.00**	TIM0: Output compare 2 (remappable to P0.04)(8)	
96	C4	60	C4	V18	S									Stabilization for main voltage regulator. Requires external capacitors 33nF between V18 and VSS18. See *Figure 4.2*. To be connected to the 1.8V external power supply when embedded regulators are not used.		
97	D4	61	C5	VSS18	S									Ground Voltage for the main voltage regulator.		
98	D3	62	A2	VSS_IO	S									Ground Voltage for digital I/Os		
99	C3	63	B2	VDD_IO	S									Supply Voltage for digital I/Os		
100	A1	64	A1	P0.03 / TIM2_TI1 / ADC_IN1	I/O	T_T	**X**	X		O2	X	X		**Port 0.03**	TIM2: Input Capture / trigger / external clock 1	ADC: analog input 1

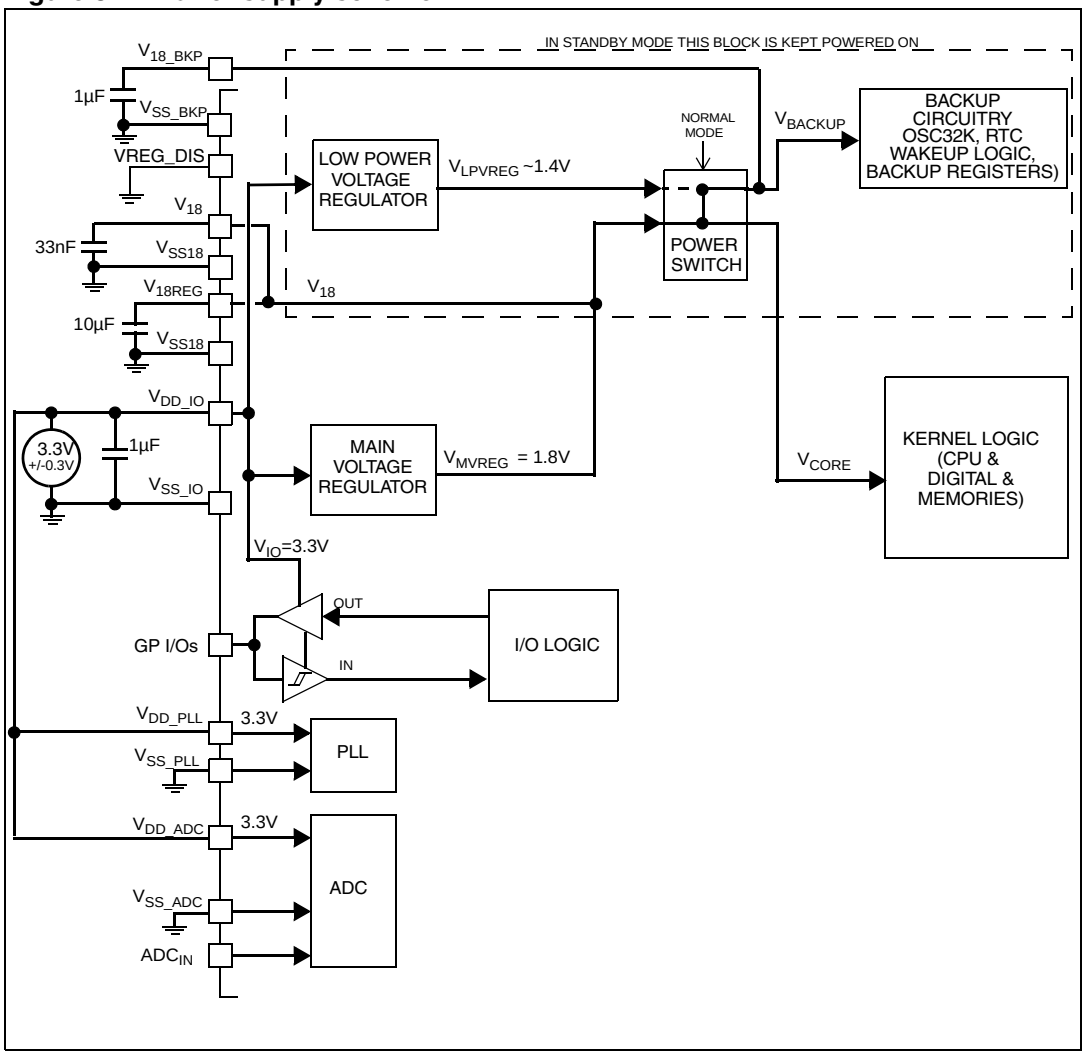
1. For STR755FVx part numbers, the USB pins must be left unconnected.
2. The non available pins on LQPFP64 and LFBGA64 packages are internally tied to low level.
3. None of the I/Os are True Open Drain: when configured as Open Drain, there is always a protection diode between the I/O pin and VDD_IO.
4. In the 100-pin package, this Alternate Function is duplicated on two ports. You can configure one port to use this AF, the other port is then free for general purpose I/O (GPIO), external interrupt/wake-up lines, or analog input (ADC_IN) where these functions are listed in the table.
5. It is mandatory that the NJTRST pin is reset to ground during the power-up phase. It is recommended to connect this pin to NRSTOUT pin (if available) or NRSTIN.
6. After reset, these pins are enabled as JTAG alternate function see (*Port reset state on page 16*). To use these ports as general purpose I/O (GPIO), the DBGOFF control bit in the GPIO_REMAP0R register must be set by software (in this case, debugging these I/Os via JTAG is not possible).
7. There are two different TQFP and BGA 64-pin packages: in the first one, pins 41 and 42 are mapped to USB DN/DP while for the second one, they are mapped to P0.15/CAN_TX and P0.14/CAN_RX.
8. For details on remapping these alternate functions, refer to the GPIO_REMAP0R register description.

6.1.6 Power supply schemes

When mentioned, some electrical parameters can refer to a dedicated power scheme among the four possibilities. The four different power schemes are described below.

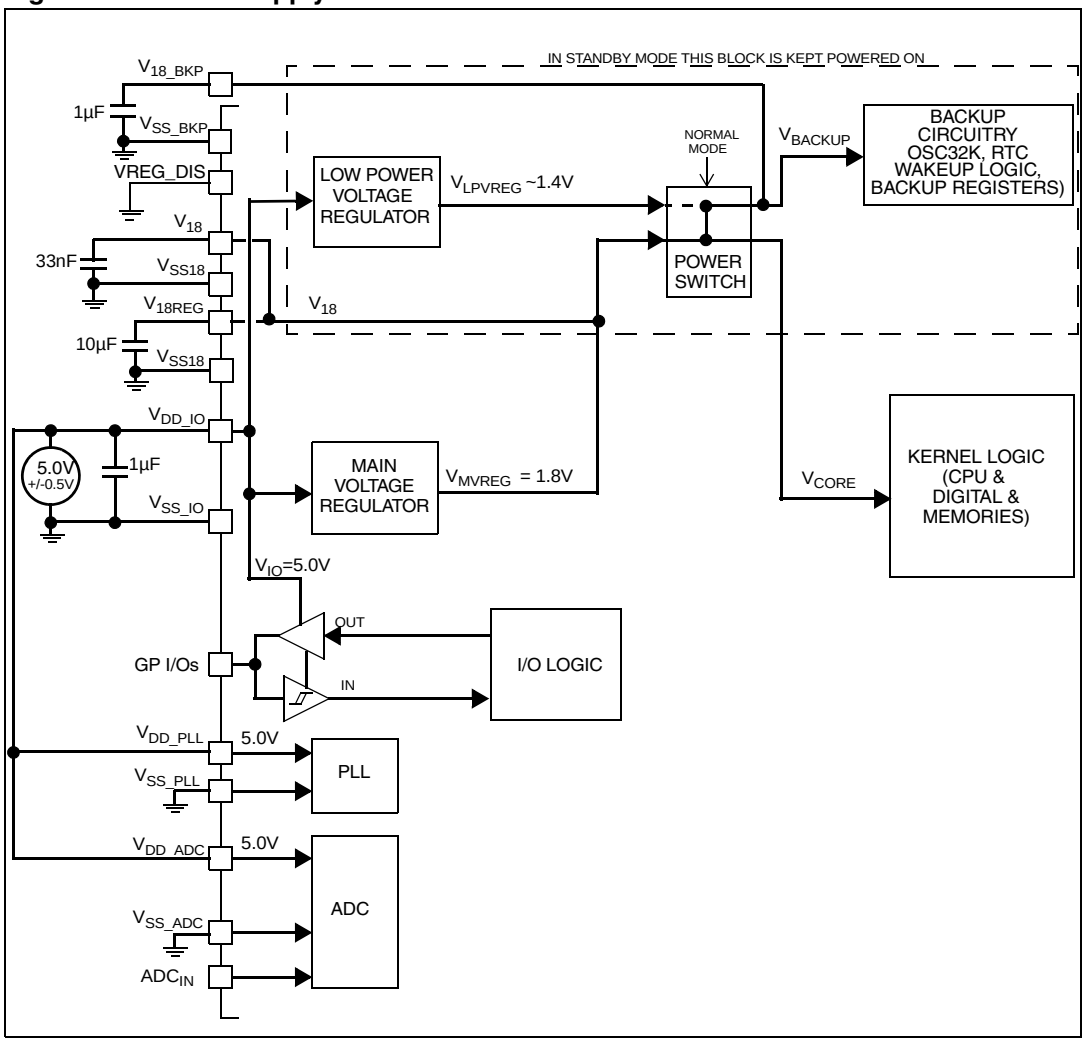
Power supply scheme 1: Single external 3.3 V power source

Figure 8. Power supply scheme 1



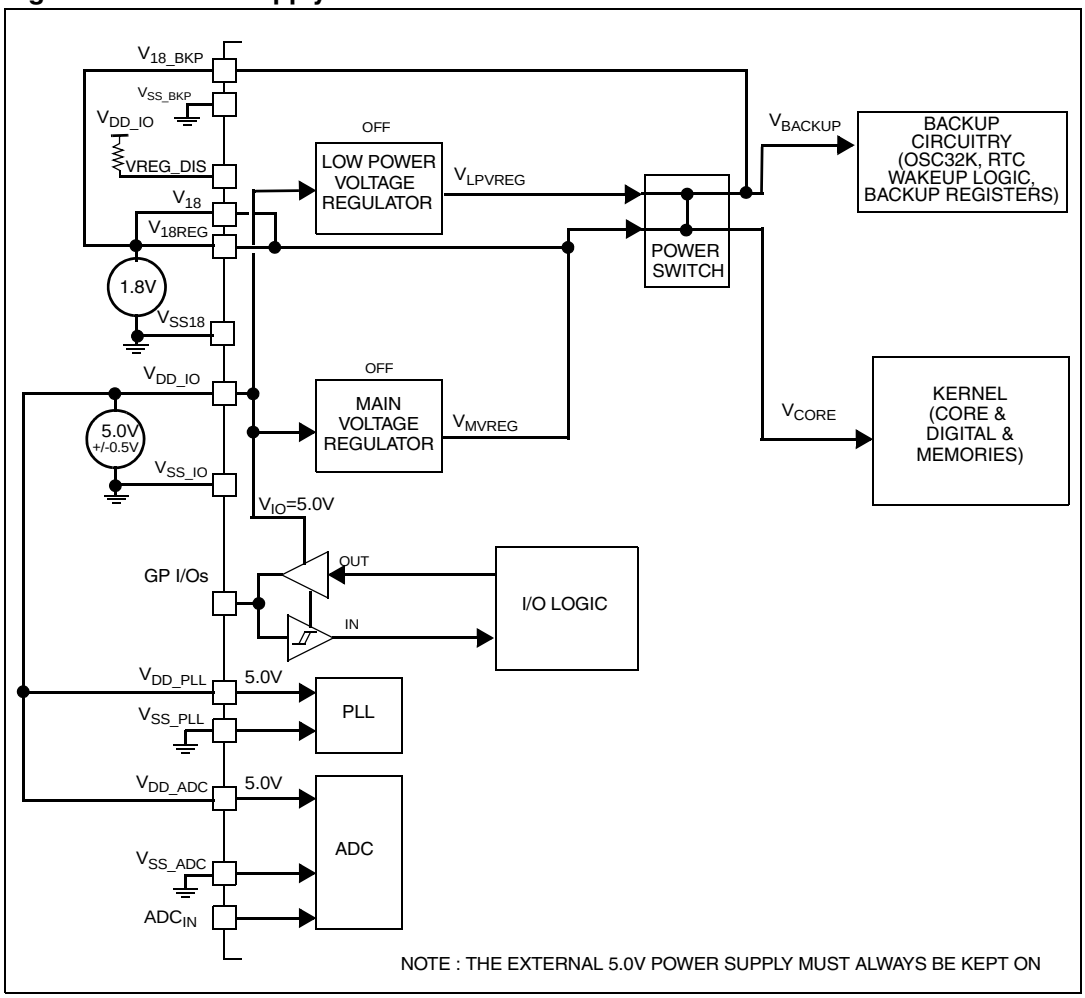
Power supply scheme 3: Single external 5 V power source

Figure 10. Power supply scheme 3



Power supply scheme 4: Dual external 1.8 V and 5.0 V supply

Figure 11. Power supply scheme 4



6.1.7 I/O characteristics versus the various power schemes (3.3V or 5.0V)

Unless otherwise mentioned, all the I/O characteristics are valid for both

- V_{DD_IO}=3.0 V to 3.6 V with bit EN33=1
- V_{DD_IO}=4.5 V to 5.5 V with bit EN33=0

When V_{DD_IO}=3.0 V to 3.6 V, I/Os are not 5V tolerant.

6.1.8 Current consumption measurements

All the current consumption measurements mentioned below refer to Power scheme 1 and 2 as described in *Figure 12* and *Figure 13*

6.2.2 Current characteristics

Table 8. Current characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD_IO} (1)	Total current into V_{DD_IO} power lines (source) (2)	150	mA
I_{VSS_IO} (1)	Total current out of V_{SS} ground lines (sink) (2)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ (3) & (4)	Injected current on NRSTIN pin	± 5	
	Injected current on XT1 and XT2 pins	± 5	
	Injected current on any other pin (5)	± 5	
$\Sigma I_{INJ(PIN)}$ (3)	Total injected current (sum of all I/O and control pins) (5)	± 25	

1. The user can use GPIOs to source or sink high current (up to 20 mA for O8 type High Sink I/Os). In this case, the user must ensure that these absolute max. values are not exceeded (taking into account the RUN power consumption) and must follow the rules described in *Section 6.3.8: I/O port pin characteristics on page 54*.
2. All 3.3 V or 5.0 V power (V_{DD_IO}, V_{DDA_ADC}, V_{DDA_PLL}) and ground (V_{SS_IO}, V_{SSA_ADC}, V_{DDA_ADC}) pins must always be connected to the external 3.3V or 5.0V supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Data based on T_A=25°C.
4. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.12: 10-bit ADC characteristics on page 72*.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

6.2.3 Thermal characteristics

Table 9. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 16. Dual supply supply typical power consumption in Run, WFI, Slow and Slow-WFI modes

To calculate the power consumption in Dual supply mode, refer to the values given in *Table 15*. and consider that this consumption is split as follows:

$I_{DD(single\ supply)} \sim I_{DD(dual\ supply)} = I_{DD\_V18} + I_{DD(VDD\_IO)}$

For 3.3V range: $I_{DD(VDD\_IO)}$ ~ 1 to 2 mA

For 5V range: $I_{DD(VDD\_IO)}$ ~ 2 to 3 mA

Therefore most of the consumption is sunk on the V_{18} power supply

This formula does not apply in STOP and STANDBY modes, refer to *Table 17*.

Subject to general operating conditions for V_{DD_IO}, and T_A

Table 17. Typical power consumption in STOP and STANDBY modes

Symbol	Parameter	Conditions		3.3V Typ(1)	5V Typ(2)	Unit
I_{DD}(3)	Supply current in STOP mode(4)	LP_PARAM bits: ALL OFF(5)		12	15	µA
		LP_PARAM bits : MVREG ON, OSC4M OFF, FLASH OFF(6)		130	135	
		LP_PARAM bits: MVREG ON, OSC4M ON , FLASH OFF(6)		1950	1930	
		LP_PARAM bits: MVREG ON, OSC4M OFF, FLASH ON (6)		630	635	
		LP_PARAM bits: MVREG ON, OSC4M ON, FLASH ON (6)		2435	2425	
	Supply current in STOP mode(7)	LPPARAM bits: ALL OFF, with V_{18}=1.8 V	I_{DD_V18} I_{DD_V33}	5 <1	5 <1	µA
		LP_PARAM bits: OSC4M ON, FLASH OFF	I_{DD_V18} I_{DD_V33}	410 1475	410 1435	
		LP_PARAM bits: OSC4M OFF, FLASH ON	I_{DD_V18} I_{DD_V33}	550 <1	550 1	
		LP_PARAM bits: OSC4M ON, FLASH ON	I_{DD_V18} I_{DD_V33}	910 1475	910 1445	
	Supply current in STANDBY mode(4)	RTC OFF		11	14	µA
		RTC ON clocked by OSC32K		14	18	

1. Typical data are based on T_A=25°C, V_{DD_IO}=3.3 V and V_{18}=1.8 V unless otherwise indicated in the table.
2. Typical data are based on T_A=25°C, V_{DD_IO}=5.0 V and V_{18}=1.8 V unless otherwise indicated in the table.
3. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4 on page 36*.
4. Single supply scheme see *Figure 12*.
5. In this mode, the whole digital circuitry is powered internally by the LPVREG at approximately 1.4 V, which significantly reduces the leakage currents.
6. In this mode, the whole digital circuitry is powered internally by the MVREG at 1.8 V.
7. Dual supply scheme see *Figure 13*.

PLL characteristics

Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 24. PLL characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock			4.0		MHz
	PLL input clock duty cycle		40		60	%
f_{PLL_OUT}	PLL multiplier output clock	f_{PLL_IN}x 24			165	MHz
f_{VCO}	VCO frequency range	When PLL operates (locked)	336		960	MHz
t_{LOCK}	PLL lock time				300	µs
$\Delta t_{JITTER1}$(2)(3)	Single period jitter (+/-3Σ peak to peak)	f_{PLL_IN} = 4 MHz(4) V_{DD_IO} is stable			+/-250	ps
$\Delta t_{JITTER2}$(2)(3)	Long term jitter (+/-3Σ peak to peak)	f_{PLL_IN} = 4 MHz(4) V_{DD_IO} is stable			+/-2.5	ns
$\Delta t_{JITTER3}$(2)(3)	Cycle to cycle jitter (+/-3Σ peak to peak)	f_{PLL_IN} = 4 MHz(4) V_{DD_IO} is stable			+/-500	ps

1. Data based on product characterisation, not tested in production.
2. Refer to jitter terminology in *: PLL characteristics on page 47* for details on how jitter is specified.
3. The jitter specification holds true only up to 50mV (peak-to-peak) noise on V_{DDA_PLL} and V_{18} supplies. Jitter will increase if the noise is more than 50mV. In addition, it assumes that the input clock has no jitter.
4. The PLL parameters (MX1, MX0, PRESC1, PRESC2) must respect the constraints described in*: PLL characteristics on page 47*.

Internal RC oscillators (FREEOSC & LPOSC)

Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 25. Internal RC oscillators (FREEOSC & LPOSC)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{CK\_FREEOSC}$	FREEOSC Oscillator Frequency		3	5	8	MHz
f_{CK_LPOSC}	LPOSC Oscillator Frequency		150	300	500	kHz

6.3.6 Memory characteristics

Flash memory

Subject to general operating conditions for V_{DD_IO} and V_{18}, T_A = -40 to 105 °C unless otherwise specified.

Table 26. Flash memory characteristics

Symbol	Parameter	Test Conditions	Value		Unit
			Typ	Max(1)	
t_{PW}	Word Program		35		µs
t_{PDW}	Double Word Program		60		µs
t_{PB0}	Bank 0 Program (256K)	Single Word programming of a checker-board pattern	2	4.9(2)	s
t_{PB1}	Bank 1 Program (16K)	Single Word programming of a checker-board pattern	125	224(2)	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed (all 1) Preprogrammed (all 0)	1.54 1.176	2.94(2) 2.38(2)	s
t_{ES}	Sector Erase (8K)	Not preprogrammed (all 1) Preprogrammed (all 0)	392 343	560(2) 532(2)	ms
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed (all 1) Preprogrammed (all 0)	8.0 6.6	13.7 11.2	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed (all 1) Preprogrammed (all 0)	0.9 0.8	1.5 1.3	s
t_{RPD}	Recovery when disabled			20	µs
t_{PSL}	Program Suspend Latency			10	µs
t_{ESL}	Erase Suspend Latency			300	µs

1. Data based on characterisation not tested in production
2. 10K program/erase cycles.

Table 27. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END_B0}	Endurance (Bank 0 sectors)		10			kcycles
N_{END_B1}	Endurance (Bank 1 sectors)		100			kcycles
Y_{RET}	Data Retention	T_A=85° C	20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

1. Data based on characterisation not tested in production.

Output speed

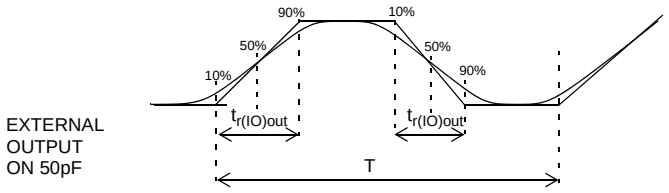
Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

Table 34. Output speed

I/O dynamic characteristics for V_{DD_IO} = 3.0 to 3.6V and EN33 bit =1 or V_{DD_IO} = 4.5 to 5.5V and EN33 bit =0							
I/O Type	**Symbol**	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
O2	$f_{max(IO)out}$	Maximum Frequency(1)	C_L=50 pF			10	MHz
	$t_{f(IO)out}$	Output high to low level fall time(2)	C_L=50 pF Between 10% and 90%			30	ns
	$t_{r(IO)out}$	Output low to high level rise time(2)				33	
O4	$f_{max(IO)out}$	Maximum Frequency(1)	C_L=50 pF			25	MHz
	$t_{f(IO)out}$	Output high to low level fall time(2)	C_L=50 pF Between 10% and 90%			12	ns
	$t_{r(IO)out}$	Output low to high level rise time(2)				14	
O8	$f_{max(IO)out}$	Maximum Frequency(1)	C_L=50pF			40	MHz
	$t_{f(IO)out}$	Output high to low level fall time(2)	C_L=50 pF Between 10% and 90%			6	ns
	$t_{r(IO)out}$	Output low to high level rise time(2)				6	

1. The maximum frequency is defined as described in *Figure 26*.
2. Data based on product characterisation, not tested in production.

Figure 26. I/O output speed definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by 50pF

6.3.10 Communication interface characteristics

SSP synchronous serial peripheral in master mode (SPI or TI mode)

General operating conditions: V_{33}, 3.0V to 3.3V, V18 =1.8V, $C_L \approx 45$ pF.

Table 38. SSP master mode characteristics(1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK}	SPI clock frequency(2)		SSP0		16	MHz
			SSP1		8	
$t_{r(SCK)}$	SPI clock rise time		SSP0		14	ns
			SSP1		33	
$t_{f(SCK)}$	SPI clock fall time		SSP0		11	
			SSP1		30	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time		SSP0		19	
			SSP1		30	
t_{NSSLQV}	NSS low to Data Output MOSI valid time		SSP0		$0.5t_{SCK}$+15ns	
			SSP1		$0.5t_{SCK}$+30ns	
$t_{SCKNSSH}$	SCK last edge to NSS high	CPHA = 0	SSP0		$0.5t_{SCK}$+15ns	
			SSP1		$0.5t_{SCK}$+30ns	
		CPHA = 1	SSP0		t_{SCK}+15ns	
			SSP1		t_{SCK}+30ns	
t_{SCKQV}	SCK trigger edge to data output MOSI valid time		SSP0		15	
			SSP1		30	
t_{SCKQX}	SCK trigger edge to data output MOSI invalid time		SSP0	0		
			SSP1	0		
t_{su}	Data input (MISO) setup time w.r.t SCK sampling edge		SSP0	25		
			SSP1	25		
t_h	Data input (MISO) hold time w.r.t SCK sampling edge		SSP0	0		
			SSP1	0		

1. Data based on characterisation results, not tested in production.
2. Max frequency for the 2 SSPs is $f_{PCLK}/2$; f_{PCLK} max = 32 MHz. This takes into account the frequency limitation due to I/O speed capability. SSP0 uses IO4 type while SSP1 uses IO2 type I/Os.

Figure 31. TI configuration - master mode, single transfer

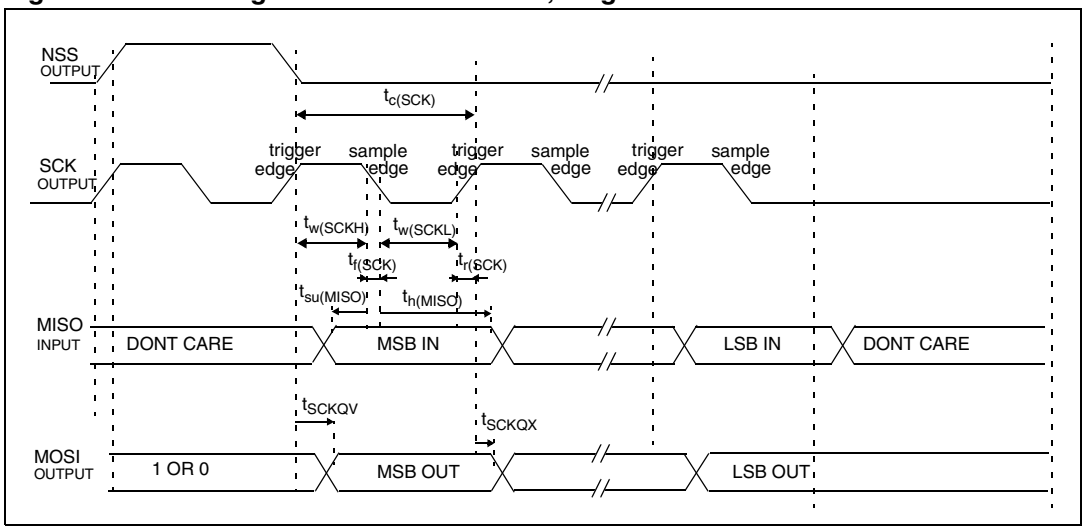


Figure 32. TI configuration - master mode, continuous transfer

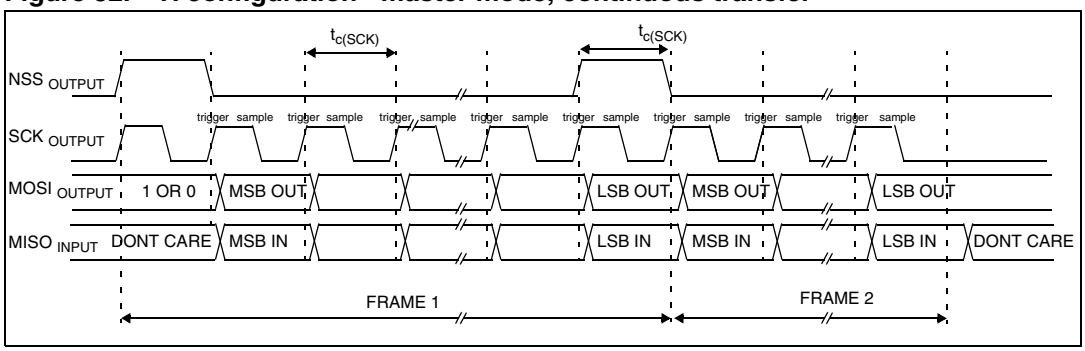


Figure 34. SPI configuration - slave mode with CPHA=0, continuous transfer

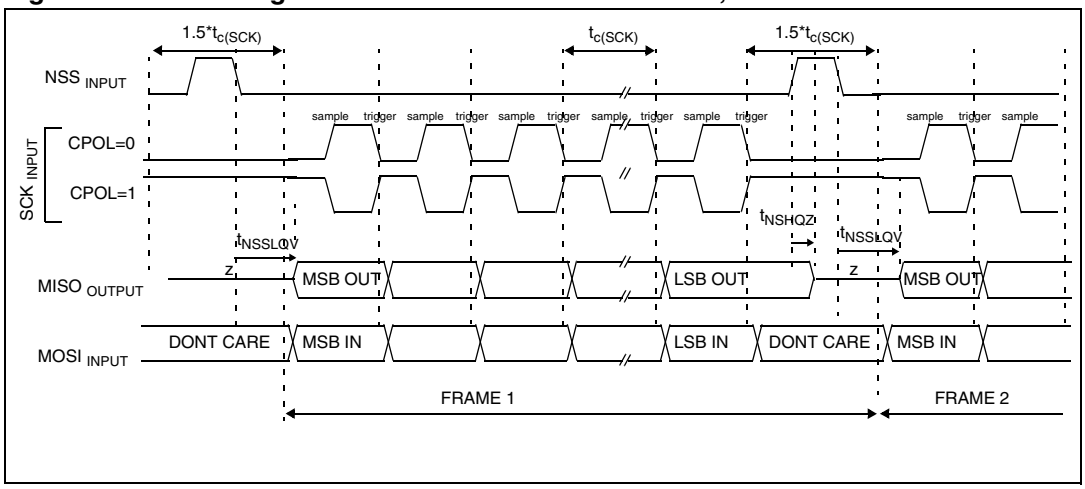


Figure 35. SPI configuration, slave mode with CPHA=1, single transfer

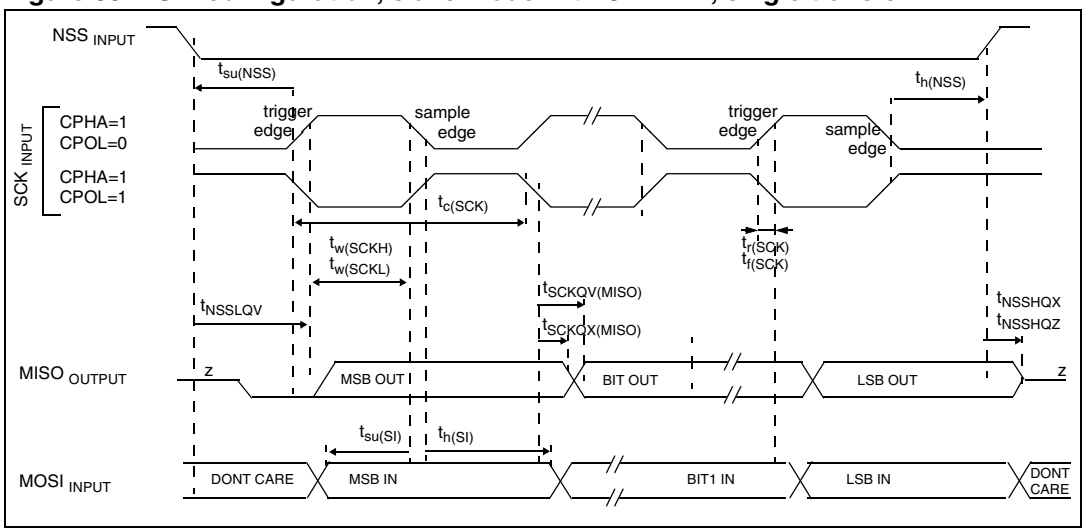
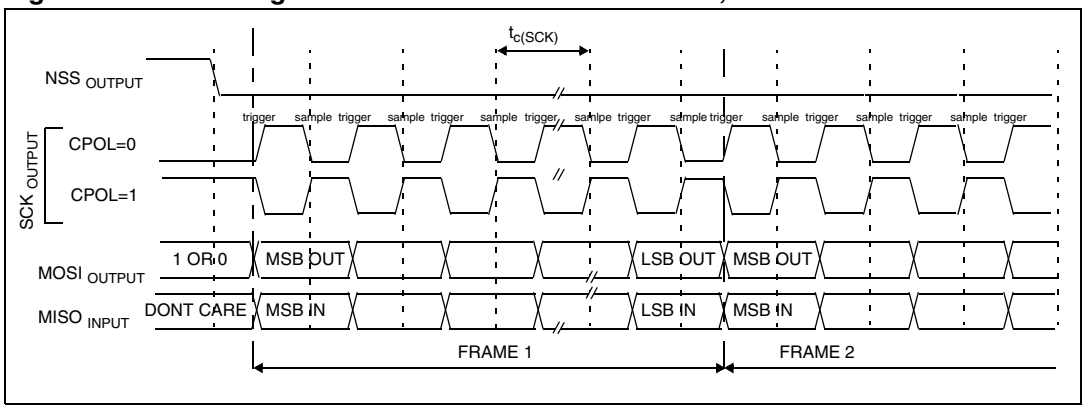


Figure 36. SPI configuration - slave mode with CPHA=1, continuous transfer



not possible to power off the STR7x while some another I^2C master node remains powered on: otherwise, the STR7x will be powered by the protection diode.

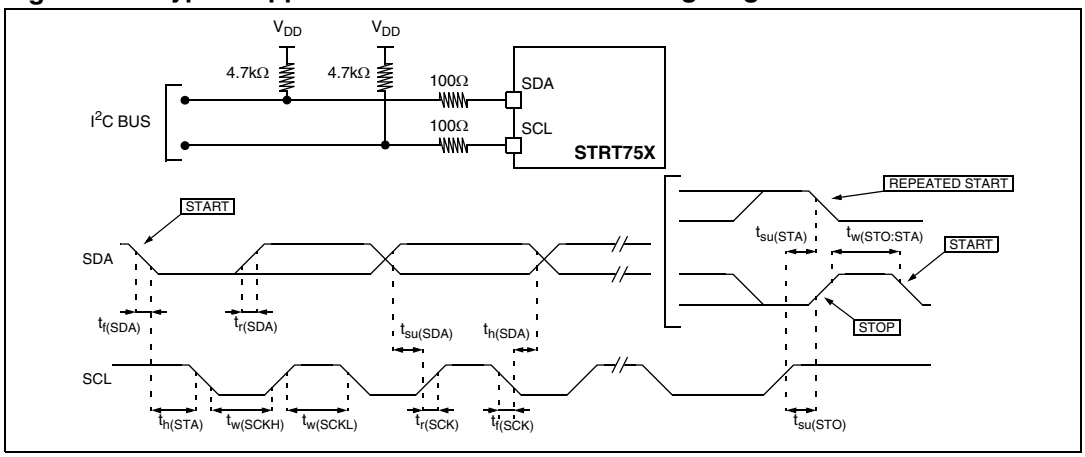
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 41. SDA and SCL characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20+0.1C_b	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20+0.1C_b	300	ns
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		µs
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. f_{PCLK}, must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
2. Data based on standard I^2C protocol requirement, not tested in production.
3. The maximum hold time $t_{h(SDA)}$ is not applicable
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 40. Typical application with I^2C bus and timing diagram



1. Measurement points are done at CMOS levels: 0.3xV_{DD} and 0.7xV_{DD}.

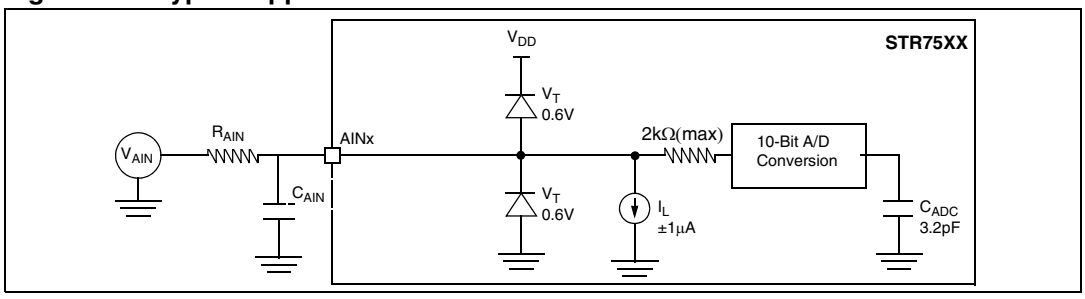
ADC accuracy vs. negative injection current

Injecting negative current on specific pins listed in *Table 46* (generally adjacent to the analog input pin being converted) should be avoided as this significantly reduces the accuracy of the conversion being performed. It is recommended to add a Schottky diode (pin to ground) to pins which may potentially inject negative current.

Table 46. List of adjacent pins

Analog input	Related adjacent pins
a	None
AIN1/P0.03	None
AIN2/P0.12	P0.11
AIN3/P0.17	P0.18 and P0.16
AIN4/P0.19	P0.24
AIN5/P0.22	None
AIN6/P0.23	P2.04
AIN7/P0.27	P1.11 and P0.26
AIN8/P0.29	P0.30 and P0.28
AIN9/P1.04	None
AIN10/P1.06	P1.05
AIN11/P1.08	P1.04 and P1.13
AIN12/P1.11	P2.17 and P0.27
AIN13/P1.12	None
AIN14/P1.13	P1.14 and P1.01
AIN15/P1.14	None

Figure 42. Typical application with ADC



Analog power supply and reference pins

The V_{DDA_ADC} and V_{SSA_ADC} pins are the analog power supply of the A/D converter cell.

Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see *: General PCB design guidelines on page 74*).

7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code *Table 49: Order codes on page 81*.

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax}= 82 °C (measured according to JESD51-2), I_{DDmax}=8 mA, V_{DD} = 5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

$$P_{INTmax} = 8 \text{ mA} \times 5 \text{ V} = 400 \text{ mW}$$

$$P_{IOmax} = 20 \times 8 \text{ mA} \times 0.4\text{V} = 64 \text{ mW}$$

This gives: P_{INTmax}= 400 mW and P_{IOmax} 64 mW:

$$P_{Dmax} = 400 \text{ mW} + 64 \text{ mW}$$

Thus: P_{Dmax} = 464 mW

Using the values obtained in *Table 48* T_{Jmax} is calculated as follows:

– For LQFP100, 46°C/W

T_{Jmax} = 82° C + (46° C/W x 464 mW) = 82°C + 21°C = 103° C

This is within the range of the suffix 6 version parts (-40 < T_J < 105° C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 49: Order codes on page 81*).

– For BGA64, 58°C/W

T_{Jmax} = 82° C + (58° C/W x 464 mW) = 82°C + 27°C = 109° C

This is within the range of the suffix 7 version parts (-40 < T_J < 125° C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 49: Order codes on page 81*).

Figure 50. LQFP100 P_{Dmax} vs T_A