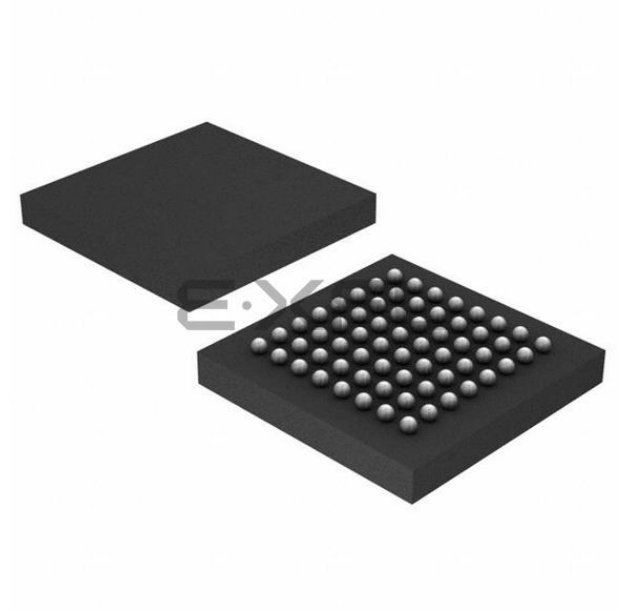

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, I²C, SPI, SSI, SSP, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str752fr0h6

I²C bus

The I²C bus interface can operate in multi-master and slave mode. It can support standard and fast modes (up to 400KHz).

High speed universal asynch. receiver transmitter (UART)

The three UART interfaces are able to communicate at speeds of up to 2 Mbit/s. They provide hardware management of the CTS and RTS signals and have LIN Master capability.

To optimize the data transfer between the processor and the peripheral, two FIFOs (receive/transmit) of 16 bytes each have been implemented.

One UART can be served by the DMA controller (UART0).

Synchronous serial peripheral (SSP)

The two SSPs are able to communicate up to 8 Mbit/s (SSP1) or up to 16 Mbit/s (SSP0) in standard full duplex 4-pin interface mode as a master device or up to 2.66 Mbit/s as a slave device. To optimize the data transfer between the processor and the peripheral, two FIFOs (receive/transmit) of 8 x 16 bit words have been implemented. The SSPs support the Motorola SPI or TI SSI protocols.

One SSP can be served by the DMA controller (SSP0).

Controller area network (CAN)

The CAN is compliant with the specification 2.0 part B (active) with a bit rate up to 1Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Up to 32 message objects are handled through an internal RAM buffer. In LQFP64 devices, CAN and USB cannot be connected simultaneously.

Universal serial bus (USB)

The STR750F embeds a USB device peripheral compatible with the USB Full speed 12Mbs. The USB interface implements a full speed (12 Mbit/s) function interface. It has software configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock source is generated from the internal main PLL. V_{DD} must be in the range 3.3V±10% for USB operation.

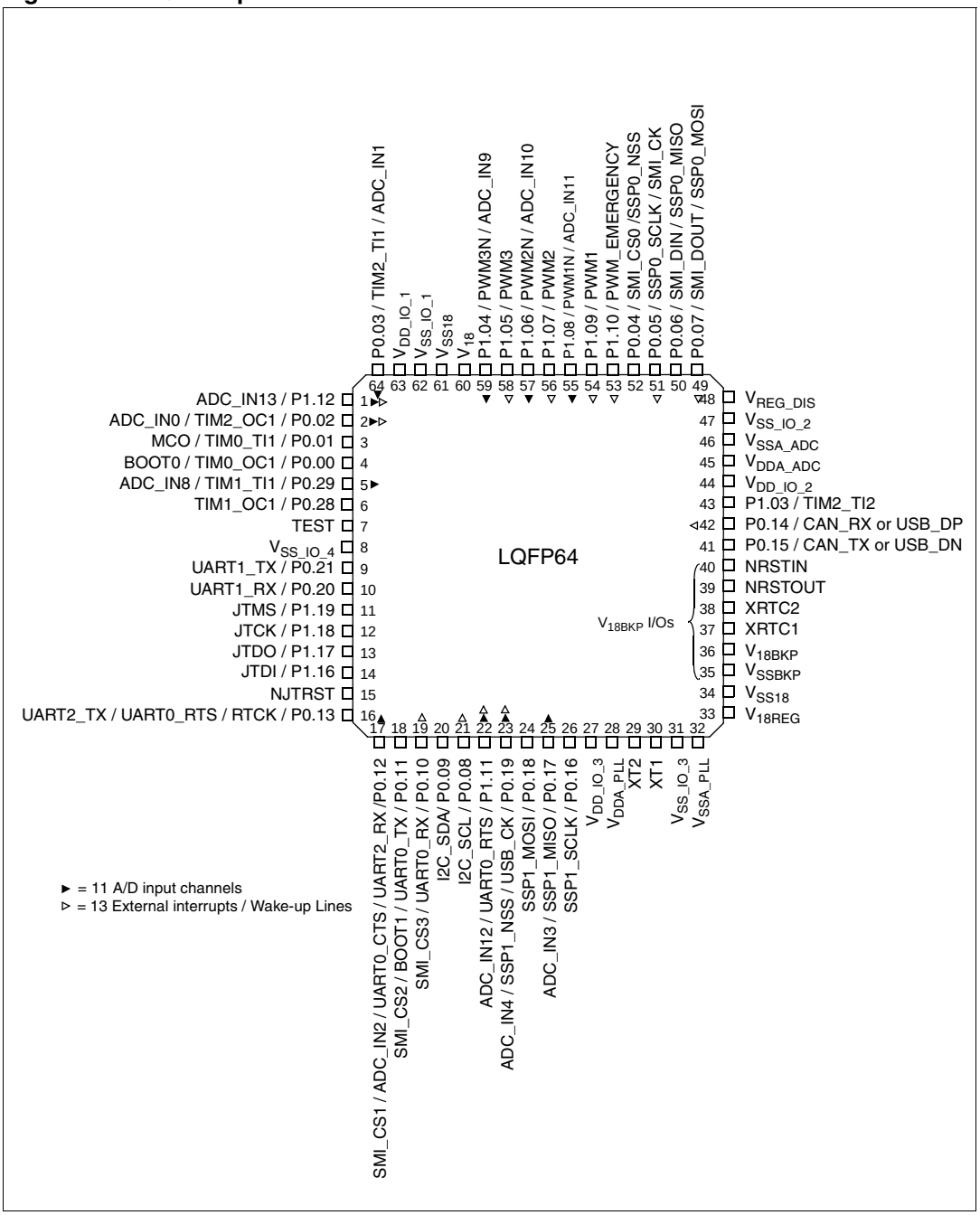
ADC (analog to digital converter)

The 10-bit Analog to Digital Converter, converts up to 16 external channels (11 channels in 64-pin devices) in single-shot or scan modes. In scan mode, continuous conversion is performed on a selected group of analog inputs. The minimum conversion time is 3.75 µs (including the sampling time).
The ADC can be served by the DMA controller.

An analog watchdog feature allows you to very precisely monitor the converted voltage of up to four channels. An IRQ is generated when the converted voltage is outside the programmed thresholds.

The events generated by TIM0, TIM2 and PWM timers can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

Figure 3. LQFP64 pinout



4.1 Pin description table

Legend / abbreviations for *Table 6*:

Type:	I = input, O = output, S = supply,
Input levels:	All Inputs are LVTTL at V_{DD_IO} = 3.3V+/-0.3V or TTL at V_{DD_IO} = 5V± 0.5V. In both cases, T_T means V_{ILmax} =0.8V V_{IHmin}=2.0V
Inputs:	All inputs can be configured as floating or with internal weak pull-up or pull down (pu/pd)
Outputs:	All Outputs can be configured as Open Drain (OD) or Push-Pull (PP) (see also note 6 below *Table 6*). There are 3 different types of Output with different drives and speed characteristics: – O8: f_{max} = 40 MHz on C_L=50pF and 8 mA static drive capability for V_{OL}=0.4V and up to 20 mA for V_{OL}=1.3V (see*Output driving current on page 55*) – O4: f_{max} = 20 MHz on C_L=50pF and 4 mA static drive capability for V_{OL}=0.4V (see*Output driving current on page 55*) – O2: f_{max} = 10 MHz on C_L=50pF and 2 mA static drive capability of for V_{OL}=0.4V (see*Output driving current on page 55*)
External interrupts/wake-up lines:	EITx

Port reset state

The reset state of the I/O ports is GPIO input floating. Exceptions are P1[19:16] and P0.13 which are configured as JTAG alternate functions:

- The JTAG inputs (JTDI, JTMS and JTDI) are configured as input floating and are ready to accept JTAG sequences.
- The JTAG output JTDO is configured as floating when idle (no JTAG operation) and is configured in output push-pull only when serial JTAG data must be output.
- The JTAG output RTCK is always configured as output push-pull. It outputs '0' level during the reset phase and then outputs the JTCK input signal resynchronized 3 times by the internal AHB clock.
- The GPIO_PCx registers do not control JTAG AF selection, so the reset values of GPIO_PCx for P1[19:16] and P0. 13 are the same as other ports. Refer to the GPIO section of the STR750 Reference Manual for the register description and reset values.
- P0.11 and P0.00 are sampled by the boot logic after reset, prior to fetching the first word of user code at address 0000 0000h.
- When booting from SMI (and only in this case), the reset state of the following GPIOs is "SMI alternate function output enabled":
  - P0.07 (SMI_DOUT)
  - P0.05 (SMI_CLK)
  - P0.04 (SMI_CS0)
  - P0.06 (SMI_DIN)

  Note that the other SMI pins: SMI_CS1,2,3 (P0.12, P0.11, P0.10) are not affected.

To avoid excess power consumption, unused I/O ports must be tied to ground.

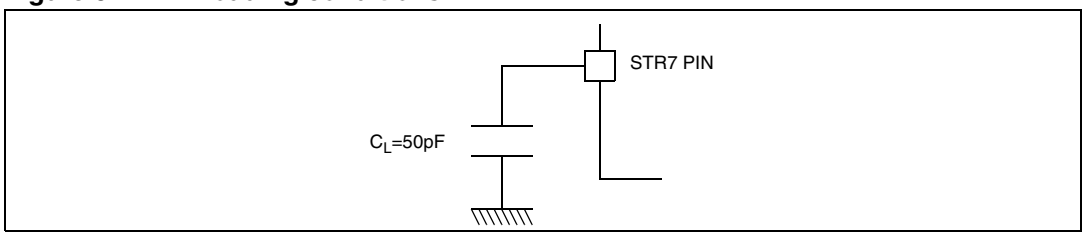
Table 6. STR750F pin description

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100[1]	LFBGA100[1]	LQFP64[2]	LFBGA64[2]			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD [3]	PP				
1	B1	1	B1	P1.12 / ADC_IN13	I/O	T_T	**X**	X	EIT12	O8	X	X		**Port 1.12**	ADC: Analog input 13	
2	B2	2	C2	P0.02 / TIM2_OC1 / ADC_IN0	I/O	T_T	**X**	X	EIT0	O8	X	X		**Port 0.02**	TIM2: Output Compare 1[4]	ADC: Analog input 0
3	B3	3	C1	P0.01 / TIM0_TI1 / MCO	I/O	T_T	**X**	X		O8	X	X		**Port 0.01**	TIM0: Input Capture / trigger / external clock 1	Main Clock Output
4	C2	4	C3	P0.00 / TIM0_OC1 / BOOT0	I/O	T_T	**X**	X		O8	X	X		**Port 0.00 / Boot mode selection input 0**	TIM0: Output Compare 1	
5	C1			P0.31 / TIM1_TI2	I/O	T_T	**X**	X		O2	X	X		**Port 0.31**	TIM1: Input Capture / trigger / external clock 2	
6	D2			P0.30 / TIM1_OC2	I/O	T_T	**X**	X		O2	X	X		**Port 0.30**	TIM1: Output Compare 2	

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

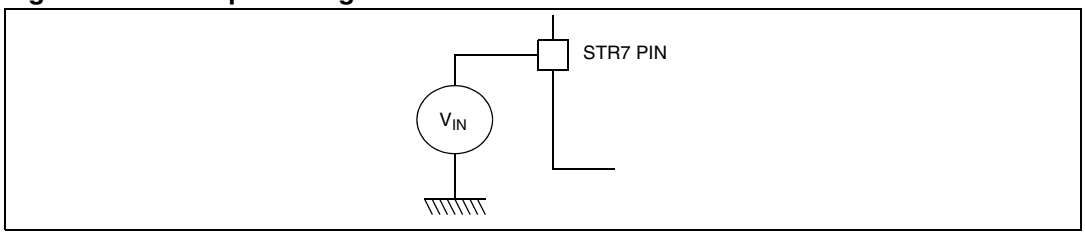
Figure 6. Pin loading conditions



6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 7. Pin input voltage

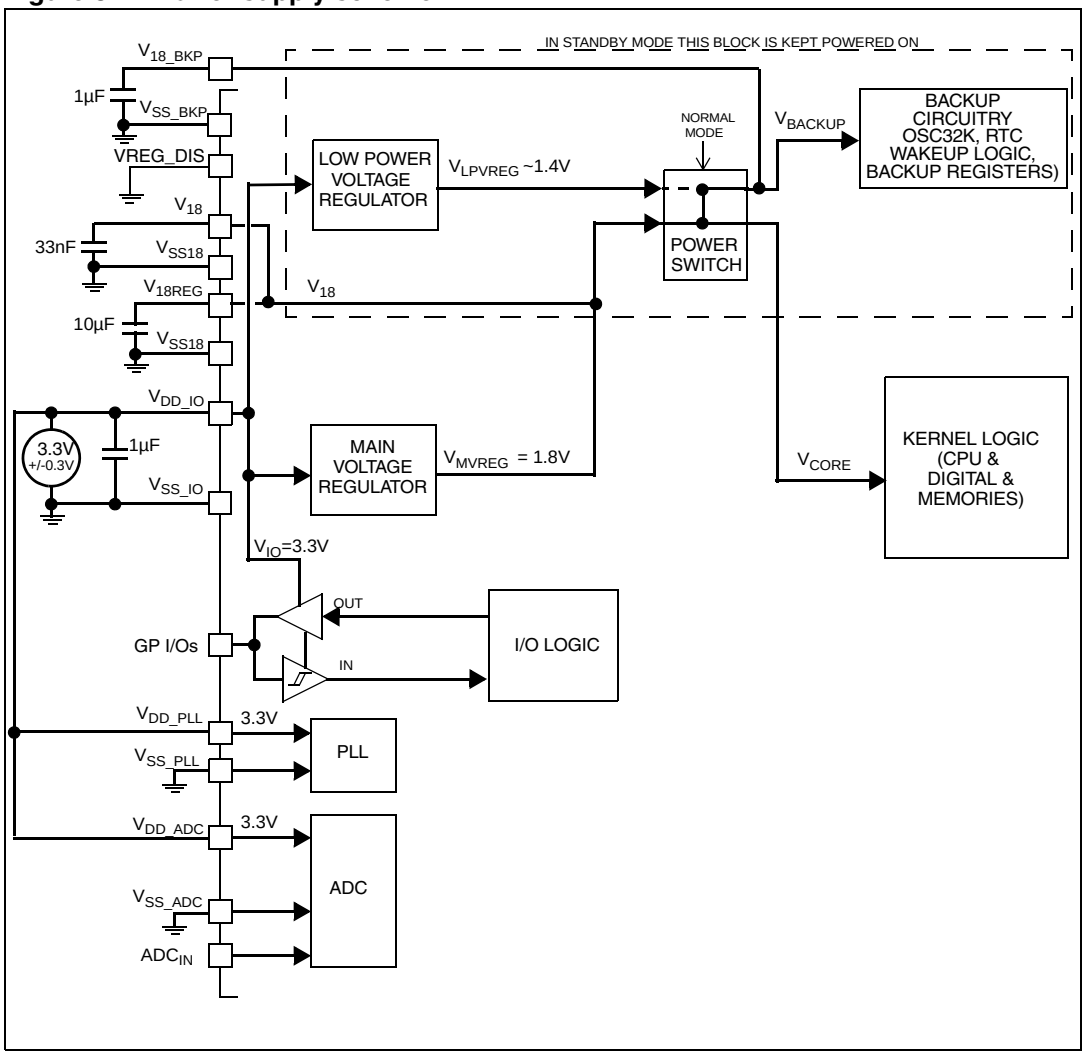


6.1.6 Power supply schemes

When mentioned, some electrical parameters can refer to a dedicated power scheme among the four possibilities. The four different power schemes are described below.

Power supply scheme 1: Single external 3.3 V power source

Figure 8. Power supply scheme 1



6.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

6.2.1 Voltage characteristics

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD_x} - V_{SS_X} (1)	Including V_{DDA_ADC} and V_{DDA_PLL}	-0.3	6.5	V
V_{18} - V_{SS18}	Digital 1.8 V Supply voltage on all V_{18} power pins (when 1.8 V is provided externally)	-0.3	2.0	
V_{IN}	Input voltage on any pin (2)	V_{SS}-0.3 to V_{DD_IO}+0.3	V_{SS}-0.3 to V_{DD_IO}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different 3.3 V or 5.0 V power pins		50	mV
$\lvert\Delta V_{18x}\rvert$	Variations between different 1.8 V power pins(3)		25	
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 52*	see *: Absolute maximum ratings (electrical sensitivity) on page 52*	
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)			

1. All 3.3 V or 5.0 V power (V_{DD_IO}, V_{DDA_ADC}, V_{DDA_PLL}) and ground (V_{SS_IO}, V_{SSA_ADC}, V_{DDA_ADC}) pins must always be connected to the external 3.3V or 5.0V supply. When powered by 3.3V, I/Os are not 5V tolerant.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
3. Only when using external 1.8 V power supply. All the power (V_{18}, V_{18REG}, V_{18BKP}) and ground (V_{SS18}, V_{SSBKP}) pins must always be connected to the external 1.8 V supply.

Figure 16. Power consumption in STOP mode in Single supply scheme (3.3 V range)

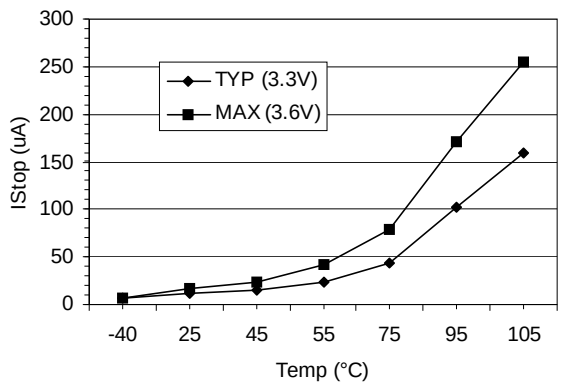


Figure 17. Power consumption in STOP mode Single supply scheme (5 V range)

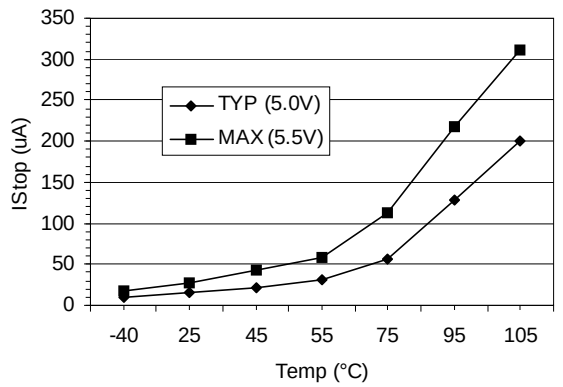


Figure 18. Power consumption in STANDBY mode (3.3 V range)

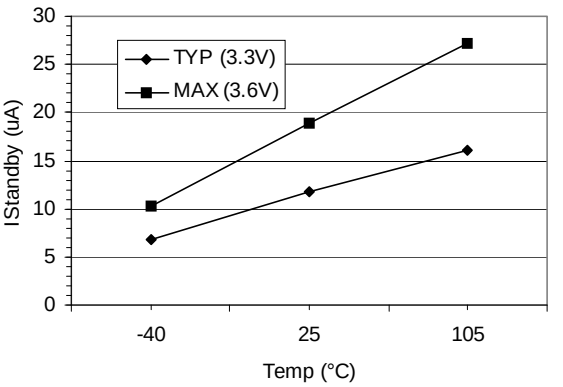
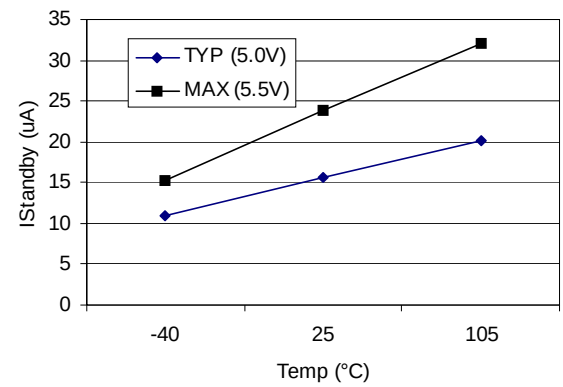


Figure 19. Power consumption in STANDBY mode (5 V range)



Subject to general operating conditions for V_{DD_IO}, and T_A

Table 15. Single supply typical power consumption in Run, WFI, Slow and Slow-WFI modes

Symbol	Para meter	Conditions	3.3V typ(1)	5V typ(2)	Unit
I_{DD} (3)	Supply current in RUN mode(4)	Clocked by OSC4M with PLL multiplication, all peripherals enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz f_{HCLK}=56 MHz, f_{PCLK}=28 MHz f_{HCLK}=48 MHz, f_{PCLK}=24 MHz f_{HCLK}=32 MHz, f_{PCLK}=32 MHz f_{HCLK}=16 MHz, f_{PCLK}=16 MHz f_{HCLK}=8 MHz, f_{PCLK}=8 MHz	 80 75 65 59 34 20	 82 77 67 61 37 22	mA
		Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz f_{HCLK}=56 MHz, f_{PCLK}=28 MHz f_{HCLK}=48 MHz, f_{PCLK}=24 MHz f_{HCLK}=32 MHz, f_{PCLK}=32 MHz f_{HCLK}=16 MHz, f_{PCLK}=16 MHz f_{HCLK}=8 MHz, f_{PCLK}=8 MHz	 65 60 54 42 22 16	 67 62 55 44 24 18	mA
	Supply current in WFI mode(4)	Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz(5) f_{HCLK}=56 MHz, f_{PCLK}=28 MHz(5) f_{HCLK}=48 MHz, f_{PCLK}=24 MHz(5) f_{HCLK}=32 MHz, f_{PCLK}=32 MHz(6) f_{HCLK}=16 MHz, f_{PCLK}= 16 MHz (6) f_{HCLK}= 8 MHz, f_{PCLK}= 8 MHz(6)	 62 59 53 22 13 10	 63 60 54 23 15 11	mA
	Supply current in SLOW mode(4)	Clocked by FREEOSC: f_{HCLK}=f_{PCLK}=~5 MHz, Clocked by OSC4M: f_{HCLK}=f_{PCLK}=4 MHz Clocked by LPOSC: f_{HCLK}=f_{PCLK}=~300 kHz Clocked by OSC32K: f_{HCLK}=f_{PCLK}=32.768 kHz	9 8 3.65 3.5	10 9 3.9 4.2	mA
	Supply current in SLOW-WFI mode(4)(7)	Clocked by FREEOSC: f_{HCLK}=f_{PCLK}=~5 MHz Clocked by OSC4M: f_{HCLK}=f_{PCLK}=4 MHz Clocked by LPOSC: f_{HCLK}=f_{PCLK}=~300 kHz Clocked by OSC32K: f_{HCLK}=f_{PCLK}=32.768 kHz	3.5 3.1 1.15 0.98	4.0 3.75 1.65 1.5	mA

1. Typical data based on T_A=25° C and V_{DD_IO}=3.3V.
2. Typical data based on T_A=25° C and V_{DD_IO}=5.0V.
3. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4 on page 36*.
4. Single supply scheme see *Figure 14*.
5. Parameter setting BURST=1, WFI_FLASHEN=1
6. Parameter setting BURST=0, WFI_FLASHEN=0
7. Parameter setting WFI_FLASHEN=0, OSC4MOFF=1

XRTC1 external clock source

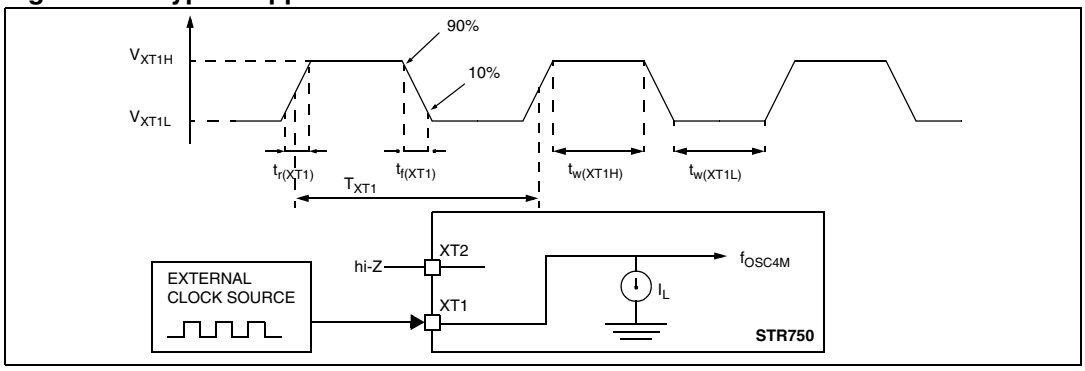
Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 21. XRTC1 external clock source

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
f_{XRTC1}	External clock source frequency	see *Figure 20*		32.768	500	kHz
V_{XRTC1H}	XRTC1 input pin high level voltage		$0.7xV_{DD\_IO}$		V_{DD_IO}	V
V_{XRTC1L}	XRTC1 input pin low level voltage		V_{SS}		$0.3xV_{DD\_IO}$	
$t_{w(XRTC1H)}$ $t_{w(XRTC1L)}$	XRTC1 high or low time(2)		900			ns
$t_{r(XRTC1)}$ $t_{f(XRTC1)}$	XRTC1 rise or fall time(2)				50	
I_L	XRTCx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD\_IO}$			±1	µA
$C_{IN(RTC1)}$	XRTC1 input capacitance(2)			5		pF
$DuCy_{(RTC1)}$	Duty cycle		30		70	%

1. Data based on typical application software.
2. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 20. Typical application with an external clock source



OSC32K crystal / ceramic resonator oscillator

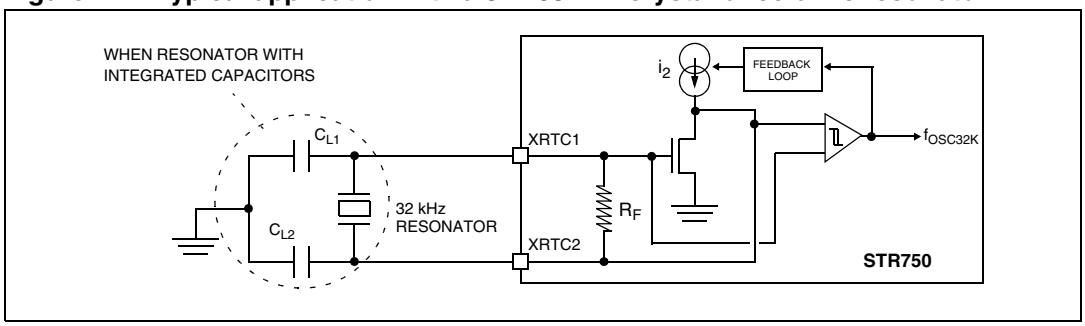
The STR7 RTC clock can be supplied with a 32.768 kHz Crystal/Ceramic resonator oscillator. All the information given in this paragraph are based on product characterisation with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

Table 23. OSC32K crystal / ceramic resonator oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC32K}	Oscillator Frequency			32.768		kHz
R_F	Feedback resistor	V_{DD_IO}=3.3 V or 5.0 V	270	310	370	kΩ
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal or ceramic resonator (R_S)(1)	R_S=40KΩ		12.5	15	pF
i_2	XT2 driving current	V_{DD_IO}=3.3 V or 5.0 V V_{IN}=V_{SS}	1		5	µA
$t_{SU(OSC32K)}$(2)	Startup time	V_{DD_IO} is stabilized		2.5		s

1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value. Refer to crystal/ceramic resonator manufacturer for more details
2. $t_{SU(OSC32K)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 32 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal/ceramic resonator manufacturer

Figure 22. Typical application with a 32.768 kHz crystal or ceramic resonator



PLL characteristics

PLL Jitter Terminology

- Self-referred single period jitter (period jitter)

  Period Jitter is defined as the difference of the maximum period (T_{max}) and minimum period (T_{min}) at the output of the PLL where T_{max} is the maximum time difference between 2 consecutive clock rising edges and T_{min} is the minimum time difference between 2 consecutive clock rising edges.

  See *Figure 23*

- Self-referred long term jitter (N period jitter)

  Self-referred long term Jitter is defined as the difference of the maximum period (T_{max}) and minimum period (T_{min}) at the output of the PLL where T_{max} is the maximum time

6.3.7 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electro magnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behaviour is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 28. EMC characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-2	Class A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-4	Class A

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 31. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A=+25° C T_A=+85° C T_A=+105° C	Class A
DLU	Dynamic latch-up class	V_{DD}= 5.5 V, f_{OSC4M}=4 MHz, f_{CK_SYS}=32 MHz, T_A=+25° C	Class A

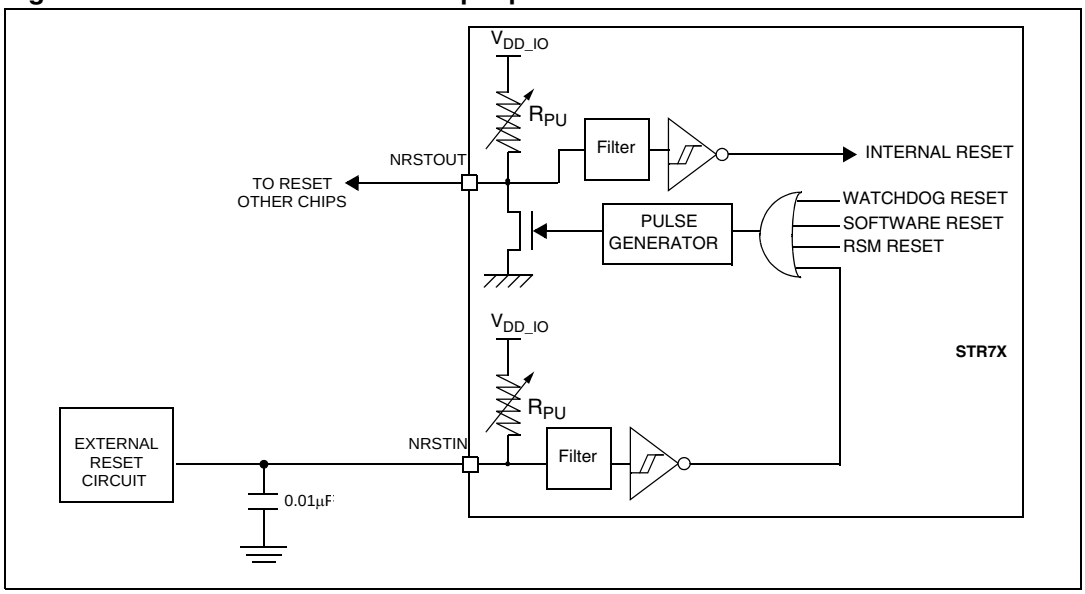
1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

Table 33. Output driving current

I/O Output drive characteristics for V_{DD_IO} = 3.0 to 3.6 V and EN33 bit =1 or V_{DD_IO} = 4.5 to 5.5 V and EN33 bit =0						
I/O Type	**Symbol**	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
O2	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+2 mA		0.4	V
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-2 mA	V_{DD_IO}-0.8		
O4	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+4 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-4 mA	V_{DD_IO}-0.8		
O8	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+8 mA		0.4	
		Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time	I_{IO}=+20 mA, $T_A \leq 85°C$ $T_A \geq 85°C$		1.3 1.5	
			I_{IO}=+8 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-8 mA	V_{DD_IO}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS_IO}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD_IO}.

Figure 27. Recommended NRSTIN pin protection



1. The user must ensure that the level on the NRSTIN pin can go below the $V_{IL(NRSTIN)}$ max. level specified in *NRSTIN and NRSTOUT pins on page 58*. Otherwise the reset will not be taken into account internally.

6.3.9 TB and TIM timer characteristics

Subject to general operating conditions for V_{DD_IO}, f_{CK_SYS}, and T_A unless otherwise specified.

Refer to *Section 6.3.8: I/O port pin characteristics on page 54* for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

Table 36. TB and TIM timers

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time	TIM0,1,2		2			t_{CK_TIM}
$t_{res(TIM)}$	Timer resolution time(1)	TB	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	16.6(1)			ns
		TIM0,1,2	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60MHz	16.6(1)			ns
f_{EXT}	Timer external clock frequency on TI1 or TI2	TIM0,1,2	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	0		$f_{CK\_TIM}/4$	MHz
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0		15	MHz
Res_{TIM}	Timer resolution					16	bit
$t_{COUNTER}$	16-bit Counter clock period when internal clock is selected (16-bit Prescaler)	TB		1		65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0.0166		1092	µs
		TIM0,1,2		1		65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0.0166		1092	µs
t_{MAX_COUNT}	Maximum Possible Count	TB				65536x65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s
		TIM0,1,2				65536x65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s

1. Take into account the frequency limitation due to the I/O speed capability when outputting the PWM to I/O pin, described in *: Output speed on page 57*.

6.3.11 USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 42. USB startup time

Symbol	Parameter	Conditions	Max	Unit
$t_{STARTUP}$	USB transceiver startup time		1	µs

Table 43. USB characteristics

USB DC Electrical Characteristics					
Symbol	**Parameter**	**Conditions**	**Min.(1)(2)**	**Max.(1)(2)**	**Unit**
Input Levels					
V_{DI}	Differential Input Sensitivity	I(DP, DM)	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	
V_{SE}	Single Ended Receiver Threshold		1.3	2.0	
Output Levels					
V_{OL}	Static Output Level Low	R_L of 1.5 kΩ to 3.6V(3)		0.3	V
V_{OH}	Static Output Level High	R_L of 15 kΩ to V_{SS}(3)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. It is important to be aware that the DP/DM pins are not 5 V tolerant. As a consequence, in case of a a shortcut with Vbus (typ: 5.0V), the protection diodes of the DP/DM pins will be direct biased . This will not damage the device if not more than 50 mA is sunk for longer than 24 hours but the reliability may be affected.
3. R_L is the load connected on the USB drivers

Figure 41. USB: data signal rise and fall time

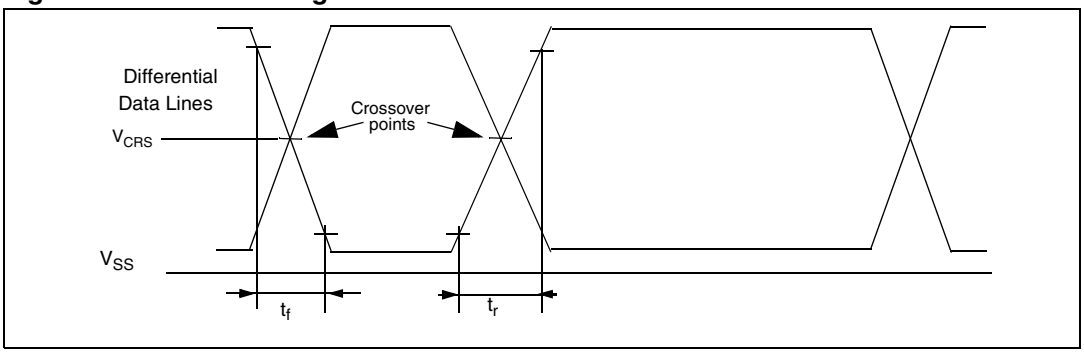


Table 44. USB: Full speed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Driver characteristics:					
t_r	Rise time(1)	C_L=50 pF	4	20	ns
t_f	Fall Time1)	C_L=50 pF	4	20	ns

6.3.12 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA_ADC}, f_{PCLK}, and T_A unless otherwise specified.

Table 45. 10-bit ADC characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
f_{ADC}	ADC clock frequency		0.4		8	MHz
V_{AIN}	Conversion voltage range(2)		V_{SSA_ADC}		V_{DDA_ADC}	V
R_{AIN}	External input impedance(3)(4)				10	kΩ
C_{AIN}	External capacitor on analog input(3)(4)				6.8	pF
I_{lkg}	Induced input leakage current	+400 µA injected on any pin			1	µA
		-400 µA injected on any pin except specific adjacent pins in *Table 46*			1	µA
		-400µA injected on specific adjacent pins in *Table 46*		40		µA
C_{ADC}	Internal sample and hold capacitor			3.5		pF
t_{CAL}	Calibration Time	f_{CK_ADC}=8 MHz	725.25			µs
			5802			$1/f_{ADC}$
t_{CONV}	Total Conversion time (including sampling time)	f_{CK_ADC}=8 MHz	3.75			µs
			30 (11 for sampling + 19 for Successive Approximation)			$1/f_{ADC}$
I_{ADC}		Sunk on V_{DDA_ADC}		3.7		mA

1. Unless otherwise specified, typical data are based on T_A=25°C. They are given only as design guidelines and are not tested.
2. Calibration is needed once after each power-up.
3. $C_{PARASITIC}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
4. Depending on the input signal variation (f_{AIN}), C_{AIN} can be increased for stabilization time and reduced to allow the use of a larger serial resistor (R_{AIN}). It is valid for all f_{ADC} frequencies ≤ 8 MHz.

7.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 10: General operating conditions on page 34*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in ° C/W,
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$),
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum Power Dissipation on Output Pins.
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 48. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 100 - 14 x 14 mm / 0.5 mm pitch	46	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 100 - 10 x 10 x 1.7mm	41	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

9 Revision history

Table 50. Document revision history

Date	Revision	Description of Changes
25-Sep-2006	1	Initial release
30-Oct-2006	2	Added power consumption data for 5V operation in *Section 6*
04-Jul-2007	3	Changed datasheet title from STR750F to STR750FXX STR751Fxx STR752Fxx STR755xx. Added *Table 1: Device summary on page 1* Added note 1 to *Table 6* Added STOP mode IDD max. values in *Table 14* Updated XT2 driving current in *Table 23.* Updated RPD in *Table 32* Updated *Table 21: XRTC1 external clock source on page 45* Updated *Table 34: Output speed on page 57* Added characteristics for *SSP synchronous serial peripheral in master mode (SPI or TI mode) on page 62* and *SSP synchronous serial peripheral in slave mode (SPI or TI mode) on page 65* Added characteristics for *SMI - serial memory interface on page 68* Added *Table 42: USB startup time on page 70*
23-Oct-2007	4	Updated *Section 6.2.3: Thermal characteristics on page 33* Updated P_D, T_J and T_A in *Section 6.3: Operating conditions on page 34* Updated *Table 20: XT1 external clock source on page 44* Updated *Table 21: XRTC1 external clock source on page 45* Updated *Section 7: Package characteristics on page 76* (inches rounded to 4 decimal digits instead of 3) Updated Ordering information *Section 8: Order codes on page 81*
17-Feb-2009	5	Modified note 3 below *Table 8: Current characteristics on page 33* Added AHB clock frequency for write access to Flash registers in *Table 10: General operating conditions on page 34* Modified note 3 below *Table 41: SDA and SCL characteristics on page 69*