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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, I²C, SPI, SSI, SSP, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str752fr0t6

periodic interrupt. It is clocked by an external 32.768 kHz oscillator or the internal low power RC oscillator. The RC has a typical frequency of 300 kHz and can be calibrated.

WDG (watchdog timer)

The watchdog timer is based on a 16-bit downcounter and 8-bit prescaler. It can be used as watchdog to reset the device when a problem occurs, or as free running timer for application time out management.

Timebase timer (TB)

The timebase timer is based on a 16-bit auto-reload counter and not connected to the I/O pins. It can be used for software triggering, or to implement the scheduler of a real-time operating system.

Synchronizable standard timers (TIM2:0)

The three standard timers are based on a 16-bit auto-reload counter and feature up to 2 input captures and 2 output compares (for external triggering or time base / time out management). They can work together with the PWM timer via the Timer Link feature for synchronization or event chaining. In reset state, timer Alternate Function I/Os are connected to the same
I/O ports in both 64-pin and 100-pin devices. To optimize timer functions in 64-pin devices, timer Alternate Function I/Os can be connected, or “remapped”, to other I/O ports as summarized in *Table 3* and detailed in *Table 6*. This remapping is done by the application via a control register.

Table 3. Standard timer alternate function I/Os

Standard timer functions		Number of alternate function I/Os		
		100-pin package	64-pin package	
			Default mapping	Remapped
TIM 0	Input Capture	2	1	2
	Output Compare/PWM	2	1	2
TIM 1	Input Capture	2	1	1
	Output Compare/PWM	2	1	1
TIM 2	Input Capture	2	2	2
	Output Compare/PWM	2	1	2

Any of the standard timers can be used to generate PWM outputs. One timer (TIM0) is mapped to a DMA channel.

Motor control PWM timer (PWM)

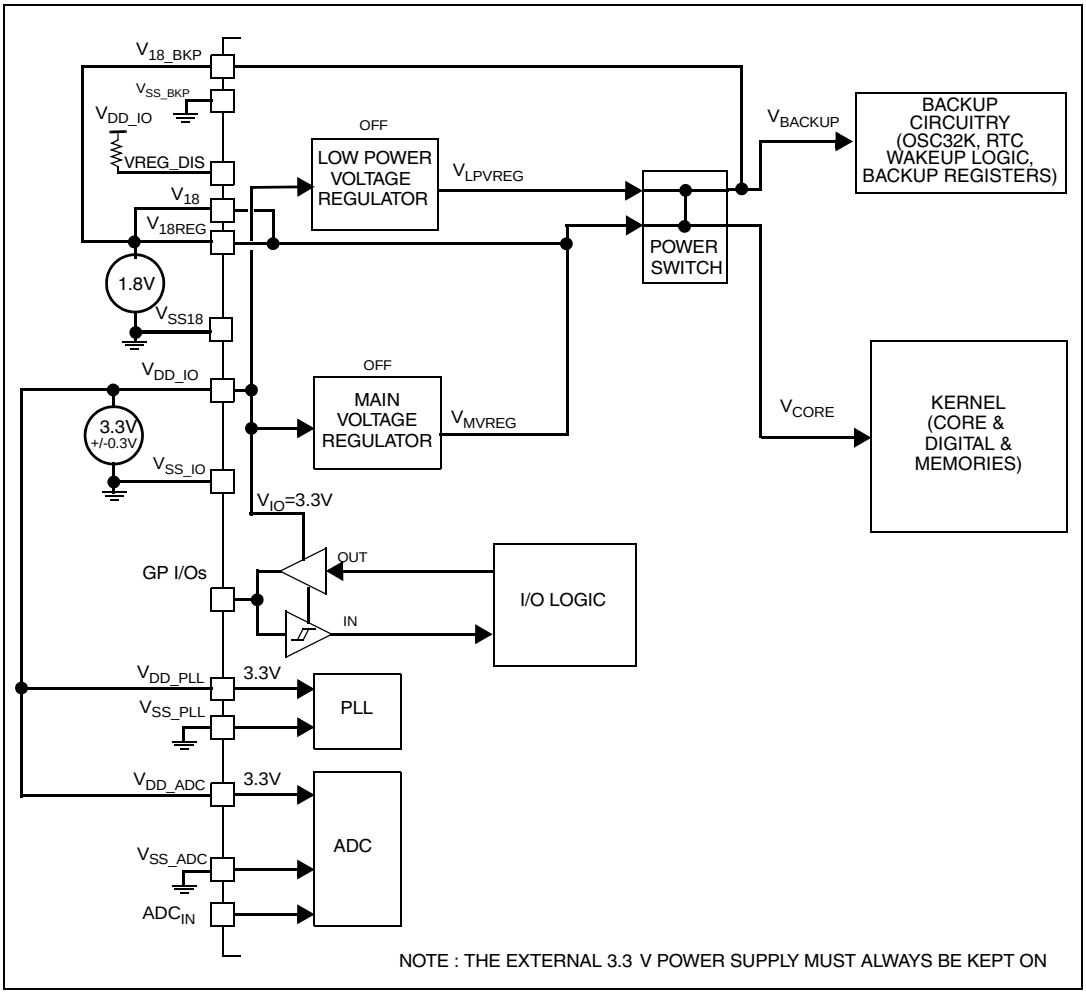
The Motor Control PWM Timer (PWM) can be seen as a three-phase PWM multiplexed on 6 channels. The 16-bit PWM generator has full modulation capability (0...100%), edge or centre-aligned patterns and supports dead-time insertion. It has many features in common with the standard TIM timers which has the same architecture and it can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.The PWM timer is mapped to a DMA channel.

GPIOs (general purpose input/output)

Each of the 72 GPIO pins (38 GPIOs in 64-pin devices) can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as Peripheral Alternate Function. Port 1.15 is an exception, it can be used as general-purpose input only or wake-up from STANDBY mode (WKP_STDBY). Most of the GPIO pins are shared with digital or analog alternate functions.

Power supply scheme 2: Dual external 1.8V and 3.3V supply

Figure 9. Power supply scheme 2



Power supply scheme 3: Single external 5 V power source

Figure 10. Power supply scheme 3

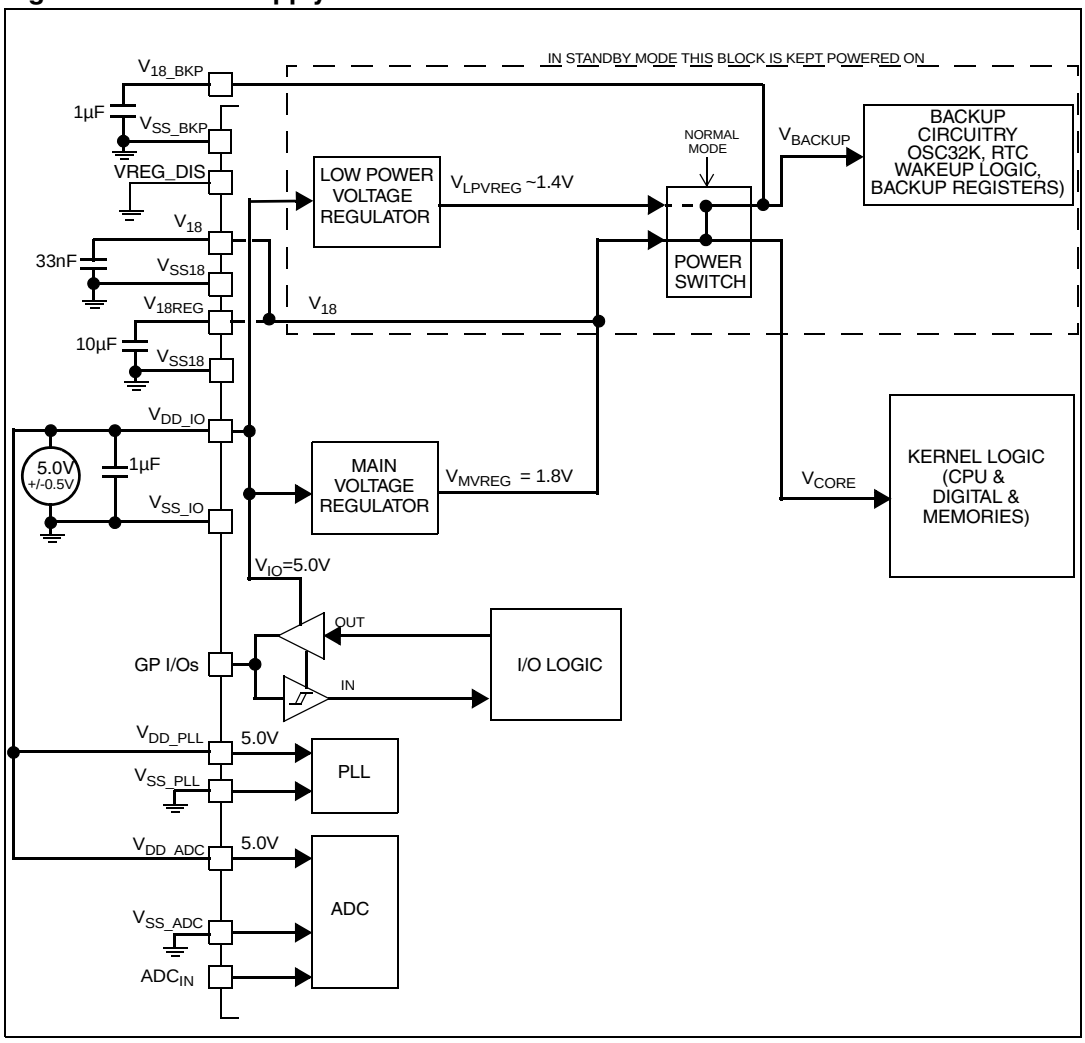


Figure 12. Power consumption measurements in power scheme 1 (regulators enabled)

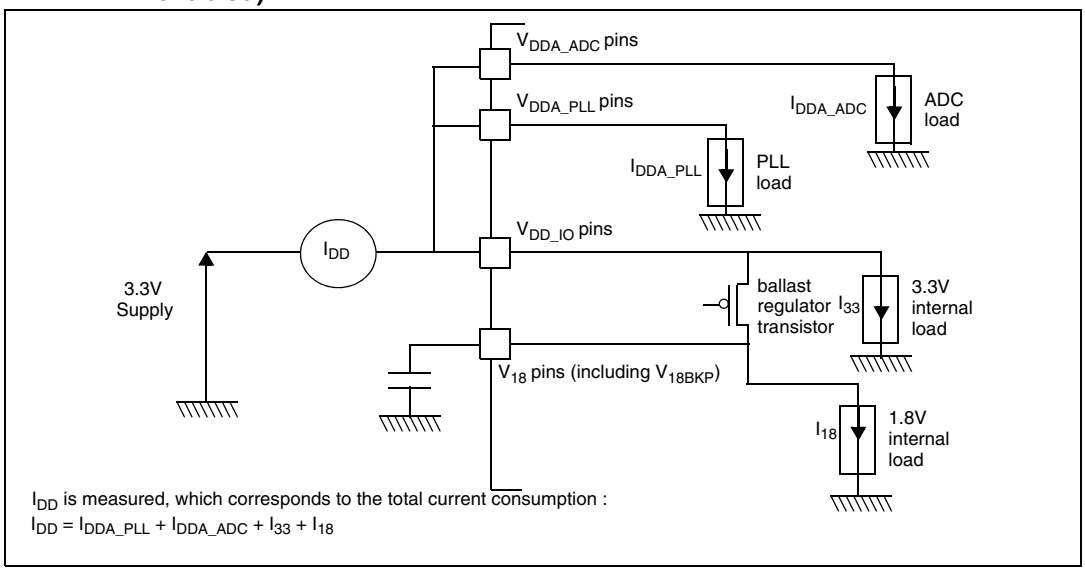
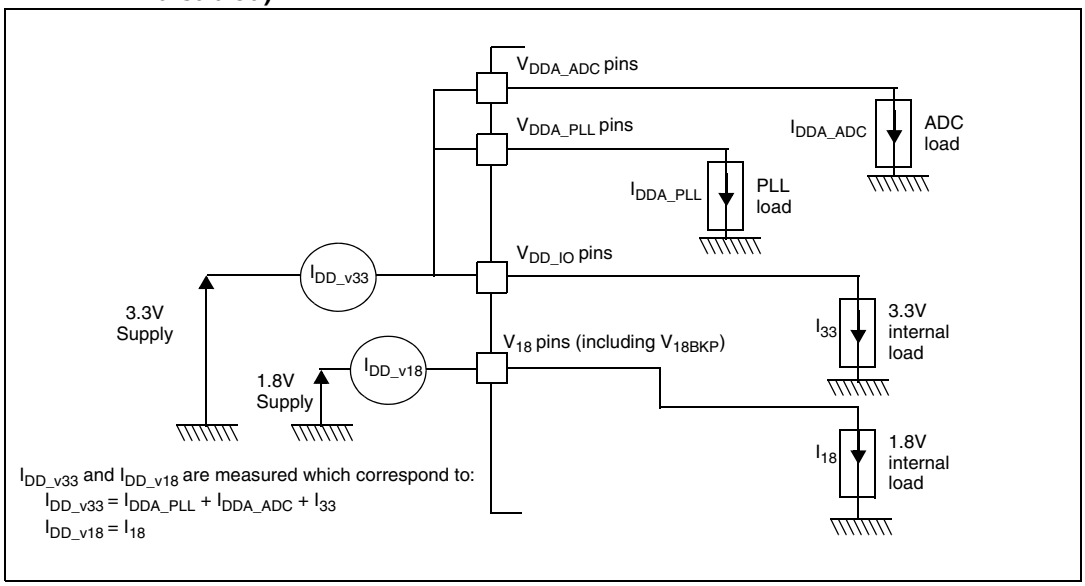


Figure 13. Power consumption measurements in power scheme 2 (regulators disabled)



6.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

6.2.1 Voltage characteristics

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD_x} - V_{SS_X} (1)	Including V_{DDA_ADC} and V_{DDA_PLL}	-0.3	6.5	V
V_{18} - V_{SS18}	Digital 1.8 V Supply voltage on all V_{18} power pins (when 1.8 V is provided externally)	-0.3	2.0	
V_{IN}	Input voltage on any pin (2)	V_{SS}-0.3 to V_{DD_IO}+0.3	V_{SS}-0.3 to V_{DD_IO}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different 3.3 V or 5.0 V power pins		50	mV
$\lvert\Delta V_{18x}\rvert$	Variations between different 1.8 V power pins(3)		25	
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 52*	see *: Absolute maximum ratings (electrical sensitivity) on page 52*	
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)			

1. All 3.3 V or 5.0 V power (V_{DD_IO}, V_{DDA_ADC}, V_{DDA_PLL}) and ground (V_{SS_IO}, V_{SSA_ADC}, V_{DDA_ADC}) pins must always be connected to the external 3.3V or 5.0V supply. When powered by 3.3V, I/Os are not 5V tolerant.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
3. Only when using external 1.8 V power supply. All the power (V_{18}, V_{18REG}, V_{18BKP}) and ground (V_{SS18}, V_{SSBKP}) pins must always be connected to the external 1.8 V supply.

6.3 Operating conditions

6.3.1 General operating conditions

Subject to general operating conditions for V_{DD_IO}, and T_A unless otherwise specified.

Table 10. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB Clock frequency	Accessing SRAM with 0 wait states	0	64	MHz
		Accessing Flash in burst mode, $T_A \leq 85°$ C	0	60	
		Accessing Flash in burst mode $T_A > 85°$ C		56	
		Accessing Flash with 0 wait states	0	32	
		Write access to Flash registers(1)	0	30	
		Accessing Flash in RWW mode	0	16	
f_{PCLK}	Internal APB Clock frequency		0	32	MHz
V_{DD_IO}	Standard Operating Voltage Power Scheme 1 & 2		3.0	3.6	V
	Standard Operating Voltage Power Scheme 3 & 4		4.5	5.5	
V_{18}	Standard Operating Voltage Power Scheme 2 & 4		1.65	1.95	
P_D	Power dissipation at $T_A = 85°$ C for suffix 6 or $T_A = 105°$ C for suffix 7(2)	LQFP100		434	mW
		LQFP64		444	
		LFBGA100		487	
		LFBGA64		344	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
		Low power dissipation(3)	-40	105	°C
	Ambient temperature for 7 suffix version	Maximum power dissipation	-40	105	°C
		Low power dissipation (3)	-40	125	°C
T_J	Junction temperature range	6 Suffix Version	-40	105	°C
		7 Suffix Version	-40	125	°C

1. Write access to Flash registers is either a program, erase, set protection or un-set protection operation.
2. If T_A is lower, higher PD values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.2: Thermal characteristics on page 79*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.2: Thermal characteristics on page 79*).

6.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 11. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{VDD_IO}	V_{DD_IO} rise time rate		20			µs/V
					20	ms/V
t_{V18}	V_{18} rise time rate (1)	When 1.8 V power is supplied externally	20			µs/V
					20	ms/V

1. Data guaranteed by characterization, not tested in production.

6.3.3 Embedded voltage regulators

Subject to general operating conditions for V_{DD_IO}, and T_A

Table 12. Embedded voltage regulators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{MVREG}	MVREG power supply(1)	load <150 mA	1.65	1.80	1.95	V
V_{LPVREG}	LPVREG power supply(2)	load <10 mA	1.30	1.40	1.50	V
t_{VREG_PWRUP}(1)	Voltage Regulators start-up time (to reach 90% of final V_{18} value) at V_{DD_IO} power-up(3)	V_{DD_IO} rise slope = 20 µs/V		80		µs
		V_{DD_IO} rise slope = 20 ms/V		35		ms

1. V_{MVREG} is observed on the V_{18}, V_{18REG} and V_{18BKP} pins except in the following case:
   - In STOP mode with MVREG OFF (LP_PARAM13 bit). See note 2.
   - In STANDBY mo*de. See note 2.*
2. In STANDBY mode, V_{LPVREG} is observed on the V_{18BKP} pin
   In STOP mode, V_{LPVREG} is observed on the V_{18}, V_{18REG} and V_{18BKP} pins.
3. Once V_{DD_IO} has reached 3.0 V, the RSM (Regulator Startup Monitor) generates an internal RESET during this start-up time.

XRTC1 external clock source

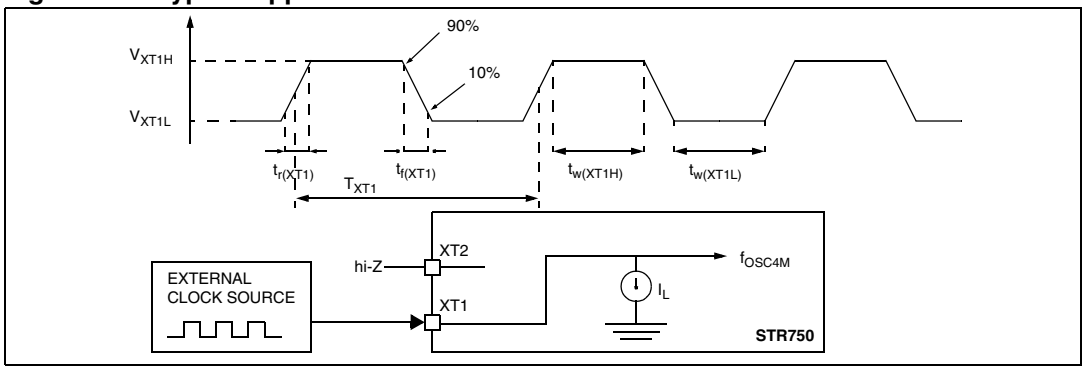
Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 21. XRTC1 external clock source

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
f_{XRTC1}	External clock source frequency	see *Figure 20*		32.768	500	kHz
V_{XRTC1H}	XRTC1 input pin high level voltage		$0.7xV_{DD\_IO}$		V_{DD_IO}	V
V_{XRTC1L}	XRTC1 input pin low level voltage		V_{SS}		$0.3xV_{DD\_IO}$	
$t_{w(XRTC1H)}$ $t_{w(XRTC1L)}$	XRTC1 high or low time(2)		900			ns
$t_{r(XRTC1)}$ $t_{f(XRTC1)}$	XRTC1 rise or fall time(2)				50	
I_L	XRTCx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD\_IO}$			±1	µA
$C_{IN(RTC1)}$	XRTC1 input capacitance(2)			5		pF
$DuCy_{(RTC1)}$	Duty cycle		30		70	%

1. Data based on typical application software.
2. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 20. Typical application with an external clock source



6.3.7 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electro magnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behaviour is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 28. EMC characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-2	Class A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-4	Class A

6.3.8 I/O port pin characteristics

General characteristics

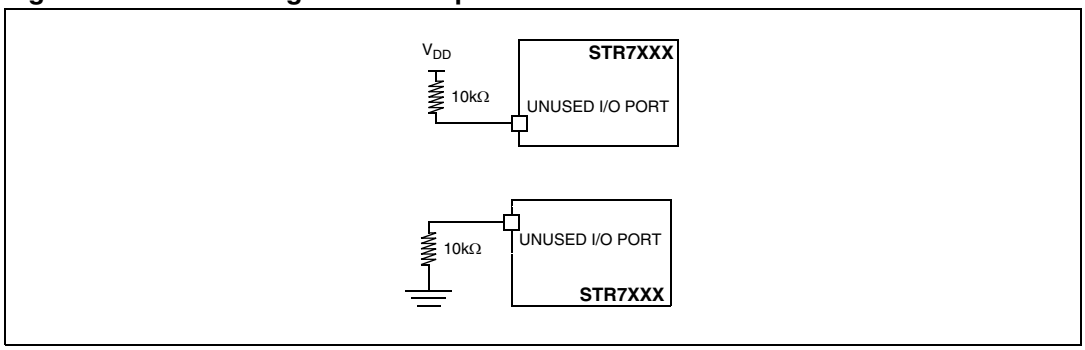
Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

Table 32. General characteristics

I/O static characteristics							
Symbol	**Parameter**	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
V_{IL}	Input low level voltage	TTL ports				0.8	V
V_{IH}	Input high level voltage			2			
V_{hys}	Schmitt trigger voltage hysteresis(1)				400		mV
$I_{INJ(PIN)}$	Injected Current on any I/O pin					± 4	mA
$\Sigma I_{INJ(PIN}$ (2)	Total injected current (sum of all I/O and control pins)					± 25	
I_{lkg}	Input leakage current on robust pins	See *Section 6.3.12 on page 72*					
	Input leakage current(3)	$V_{SS} \le V_{IN} \le V_{DD\_IO}$				±1	µA
I_S	Static current consumption(4)	Floating input mode			200		
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN}=V_{SS}$	V_{DD_IO}=3.3 V	50	95	200	kΩ
			V_{DD_IO}=5 V	20	58	150	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN}=V_{DD\_IO}$	V_{DD_IO}=3.3 V	25	80	180	kΩ
			V_{DD_IO}=5 V	20	50	120	kΩ
C_{IO}	I/O pin capacitance				5		pF
$t_{w(IT)in}$	External interrupt/wake-up lines pulse time(6)			2			T_{APB}

1. Hysteresis voltage between Schmitt trigger switching levels.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{DD\_IO}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 6.2 on page 32* for more details.
3. Leakage could be higher than max. if negative current is injected on adjacent pins.
4. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor (see *Figure 25*). Data based on design simulation and/or technology characteristics, not tested in production.
5. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor.
6. To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

Figure 25. Connecting unused I/O pins



Output driving current

The GP I/Os have different drive capabilities:

- O2 outputs can sink or source up to +/-2 mA.
- O4 outputs can sink or source up to +/-4 mA.
- outputs can sink or source up to +/-8 mA or can sink +20 mA (with a relaxed V_{OL}).

In the application, the user must limit the number of I/O pins which can drive current to respect the absolute maximum rating specified in *Section 6.2.2* :

- The sum of the current sourced by all the I/Os on $V_{DD\_IO,}$ plus the maximum RUN consumption of the MCU sourced on $V_{DD\_IO,}$ can not exceed the absolute maximum rating IV_{DD_IO}.
- The sum of the current sunk by all the I/Os on V_{SS_IO} plus the maximum RUN consumption of the MCU sunk on V_{SS_IO} can not exceed the absolute maximum rating IV_{SS_IO}.

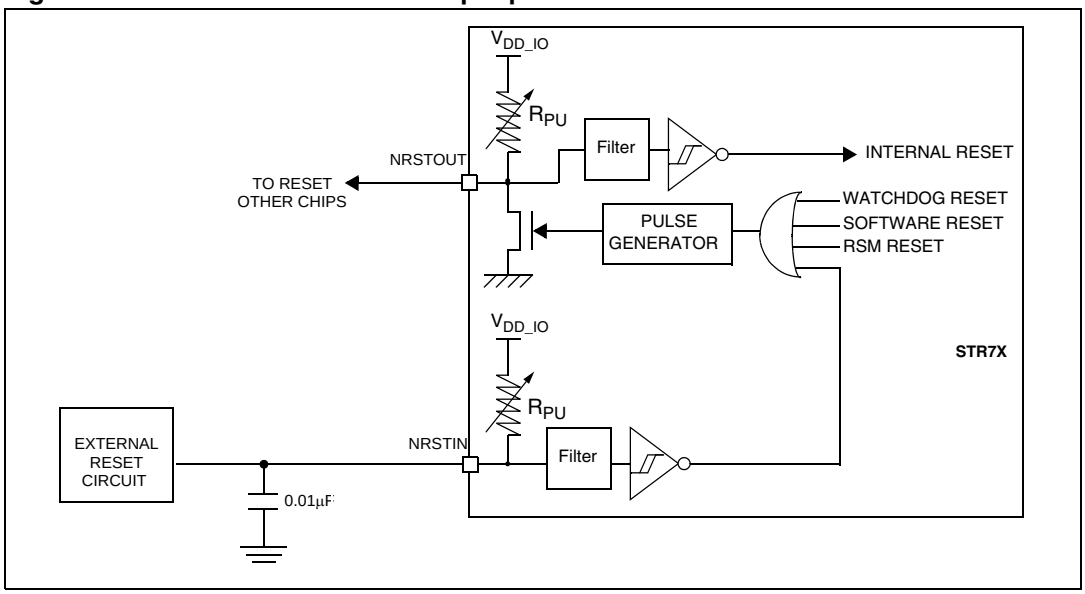
Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

Table 33. Output driving current

I/O Output drive characteristics for V_{DD_IO} = 3.0 to 3.6 V and EN33 bit =1 or V_{DD_IO} = 4.5 to 5.5 V and EN33 bit =0						
I/O Type	**Symbol**	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
O2	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+2 mA		0.4	V
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-2 mA	V_{DD_IO}-0.8		
O4	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+4 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-4 mA	V_{DD_IO}-0.8		
O8	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+8 mA		0.4	
		Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time	I_{IO}=+20 mA, $T_A \leq 85°C$ $T_A \geq 85°C$		1.3 1.5	
			I_{IO}=+8 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-8 mA	V_{DD_IO}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS_IO}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD_IO}.

Figure 27. Recommended NRSTIN pin protection



1. The user must ensure that the level on the NRSTIN pin can go below the $V_{IL(NRSTIN)}$ max. level specified in *NRSTIN and NRSTOUT pins on page 58*. Otherwise the reset will not be taken into account internally.

not possible to power off the STR7x while some another I^2C master node remains powered on: otherwise, the STR7x will be powered by the protection diode.

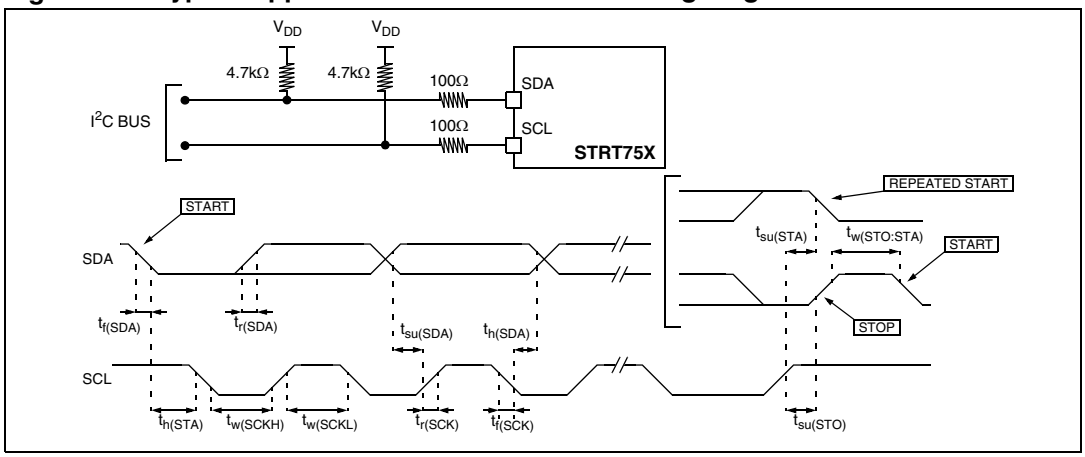
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 41. SDA and SCL characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20+0.1C_b	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20+0.1C_b	300	ns
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		µs
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. f_{PCLK}, must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
2. Data based on standard I^2C protocol requirement, not tested in production.
3. The maximum hold time $t_{h(SDA)}$ is not applicable
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 40. Typical application with I^2C bus and timing diagram



1. Measurement points are done at CMOS levels: 0.3xV_{DD} and 0.7xV_{DD}.

6.3.12 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA_ADC}, f_{PCLK}, and T_A unless otherwise specified.

Table 45. 10-bit ADC characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
f_{ADC}	ADC clock frequency		0.4		8	MHz
V_{AIN}	Conversion voltage range(2)		V_{SSA_ADC}		V_{DDA_ADC}	V
R_{AIN}	External input impedance(3)(4)				10	kΩ
C_{AIN}	External capacitor on analog input(3)(4)				6.8	pF
I_{lkg}	Induced input leakage current	+400 µA injected on any pin			1	µA
		-400 µA injected on any pin except specific adjacent pins in *Table 46*			1	µA
		-400µA injected on specific adjacent pins in *Table 46*		40		µA
C_{ADC}	Internal sample and hold capacitor			3.5		pF
t_{CAL}	Calibration Time	f_{CK_ADC}=8 MHz	725.25			µs
			5802			$1/f_{ADC}$
t_{CONV}	Total Conversion time (including sampling time)	f_{CK_ADC}=8 MHz	3.75			µs
			30 (11 for sampling + 19 for Successive Approximation)			$1/f_{ADC}$
I_{ADC}		Sunk on V_{DDA_ADC}		3.7		mA

1. Unless otherwise specified, typical data are based on T_A=25°C. They are given only as design guidelines and are not tested.
2. Calibration is needed once after each power-up.
3. $C_{PARASITIC}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
4. Depending on the input signal variation (f_{AIN}), C_{AIN} can be increased for stabilization time and reduced to allow the use of a larger serial resistor (R_{AIN}). It is valid for all f_{ADC} frequencies ≤ 8 MHz.

General PCB design guidelines

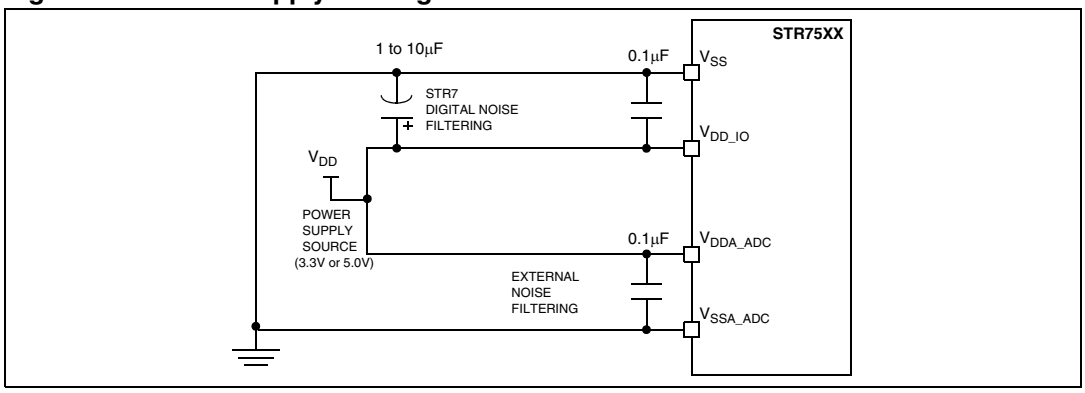
To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 µF and optionally, if needed 10 pF capacitors as close as possible to the STR7 power supply pins and a 1 to 10 µF capacitor close to the power source (see *Figure 43*).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{DDA_ADC} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs near the A/D input being converted.

Software filtering of spurious conversion results

For EMC performance reasons, it is recommended to filter A/D conversion outliers using software filtering techniques.

Figure 43. Power supply filtering

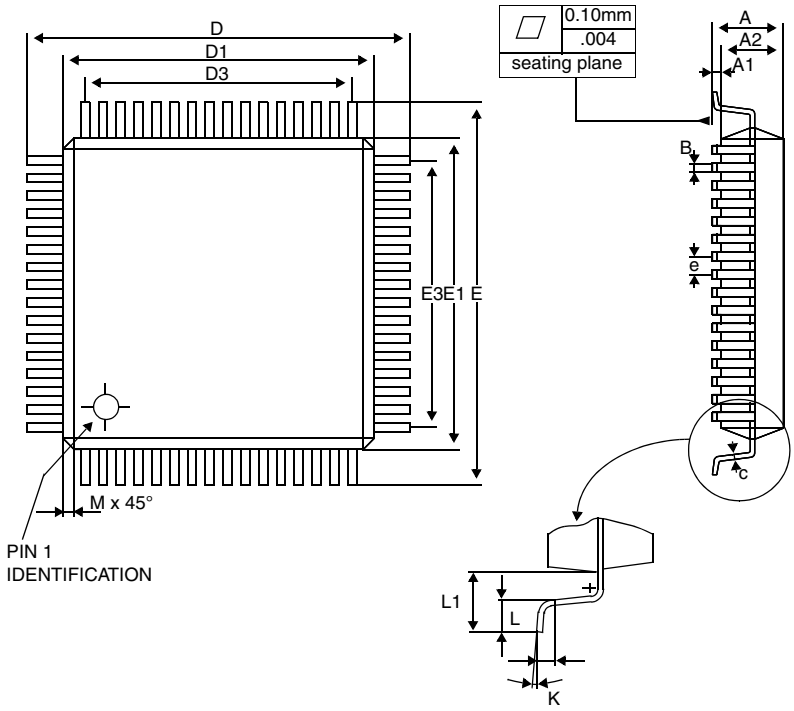


7 Package characteristics

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 Package mechanical data

Figure 45. 64-pin low profile quad flat package (10x10)



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of pins					
N	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

8 Order codes

Table 49. Order codes

Order code	Flash Prog. Memory (Bank 0) Kbytes	Package	CAN Periph	USB Periph	Nominal Temp. Range (T_A)
STR750FV0T6	64	LQFP100 14x14	Yes	Yes	-40 to +85°C
STR750FV1T6	128				
STR750FV2T6	256				
STR750FV0H6	64	LFBGA100 10x10			
STR750FV1H6	128				
STR750FV2H6	256				
STR751FR0T6	64	LQFP64 10x10	-	Yes	-40 to +85°C
STR751FR1T6	128				
STR751FR2T6	256				
STR751FR0H6	64	LFBGA64 8x8			
STR751FR1H6	128				
STR751FR2H6	256				
STR752FR0T6	64	LQFP64 10x10	Yes	-	-40 to +85°C
STR752FR1T6	128				
STR752FR2T6	256				
STR752FR0H6	64	LFBGA64 8x8			
STR752FR1H6	128				
STR752FR2H6	256				
STR752FR0T7	64	LQFP64 10x10	Yes	-	-40 to +105°C
STR752FR1T7	128				
STR752FR2T7	256				
STR752FR0H7	64	LFBGA64 8x8			
STR752FR1H7	128				
STR752FR2H7	256				
STR755FR0T6	64	LQFP64 10x10	-	-	-40 to +85°C
STR755FR1T6	128				
STR755FR2T6	256				
STR755FR0H6	64	LFBGA64 8x8			
STR755FR1H6	128				
STR755FR2H6	256				

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