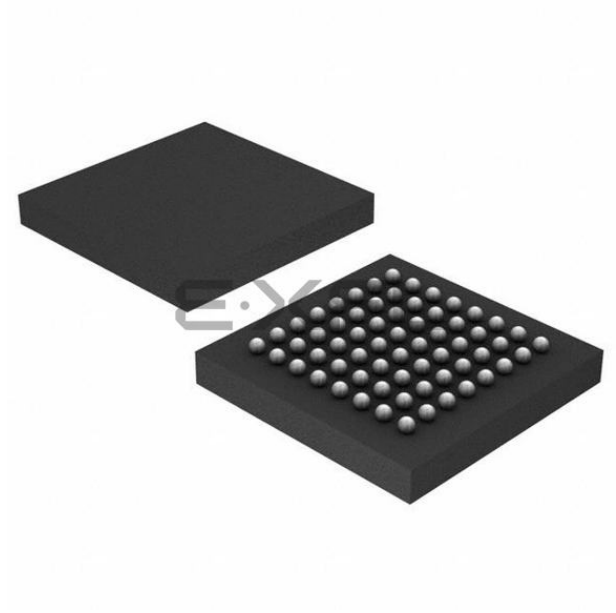

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

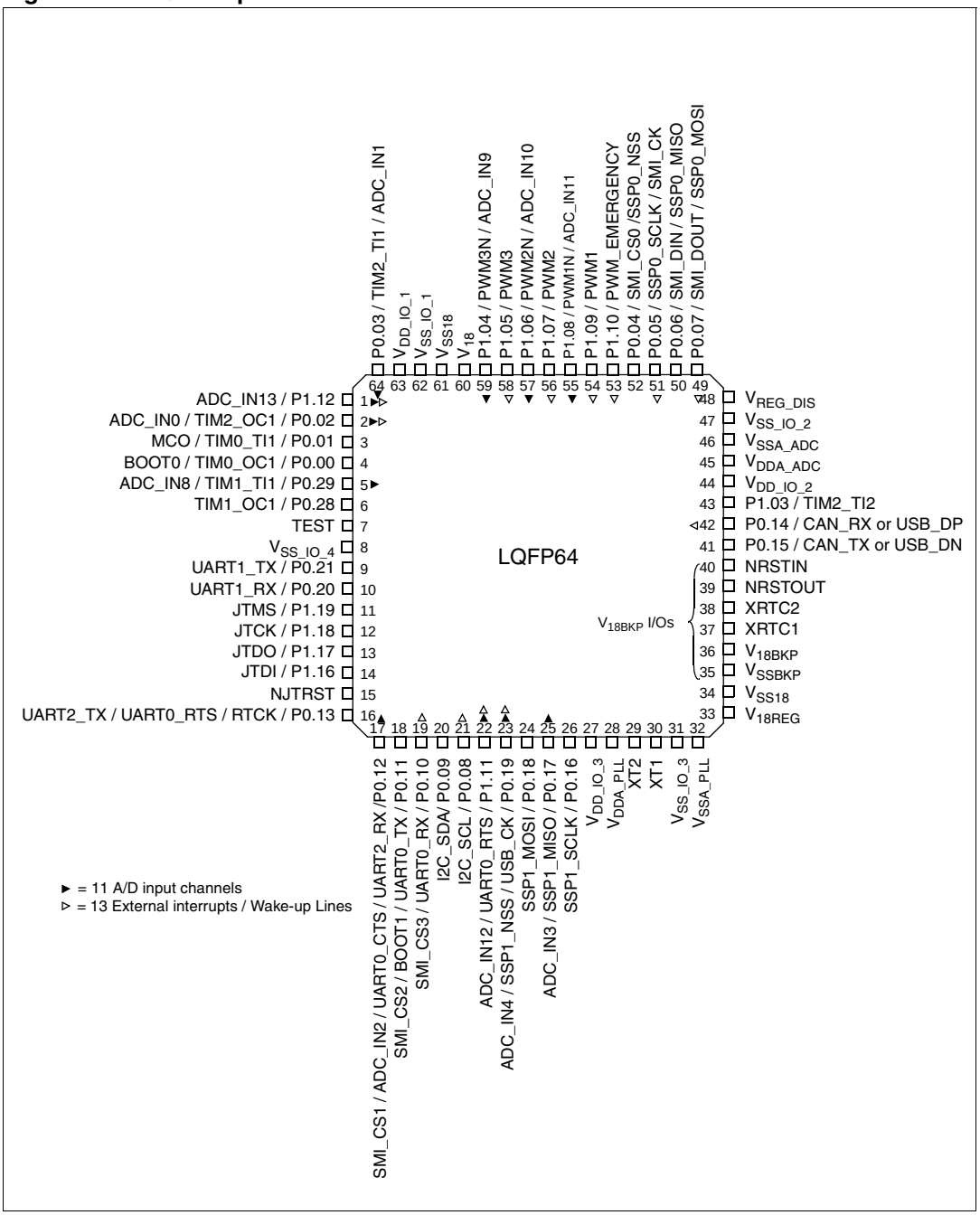
Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, I²C, SPI, SSI, SSP, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str752fr1h6

Contents

GPIOs (general purpose input/output)

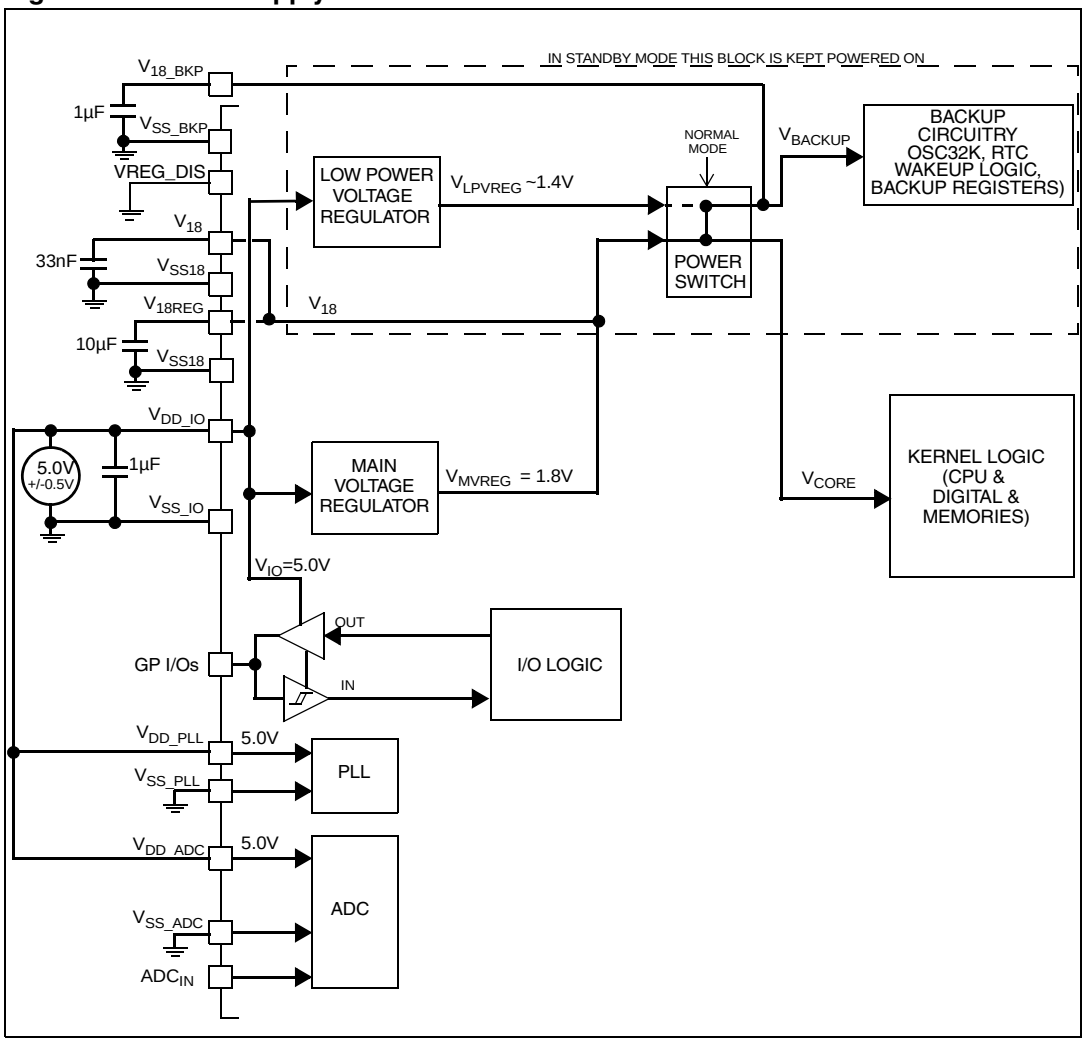
Each of the 72 GPIO pins (38 GPIOs in 64-pin devices) can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as Peripheral Alternate Function. Port 1.15 is an exception, it can be used as general-purpose input only or wake-up from STANDBY mode (WKP_STDBY). Most of the GPIO pins are shared with digital or analog alternate functions.

Figure 3. LQFP64 pinout



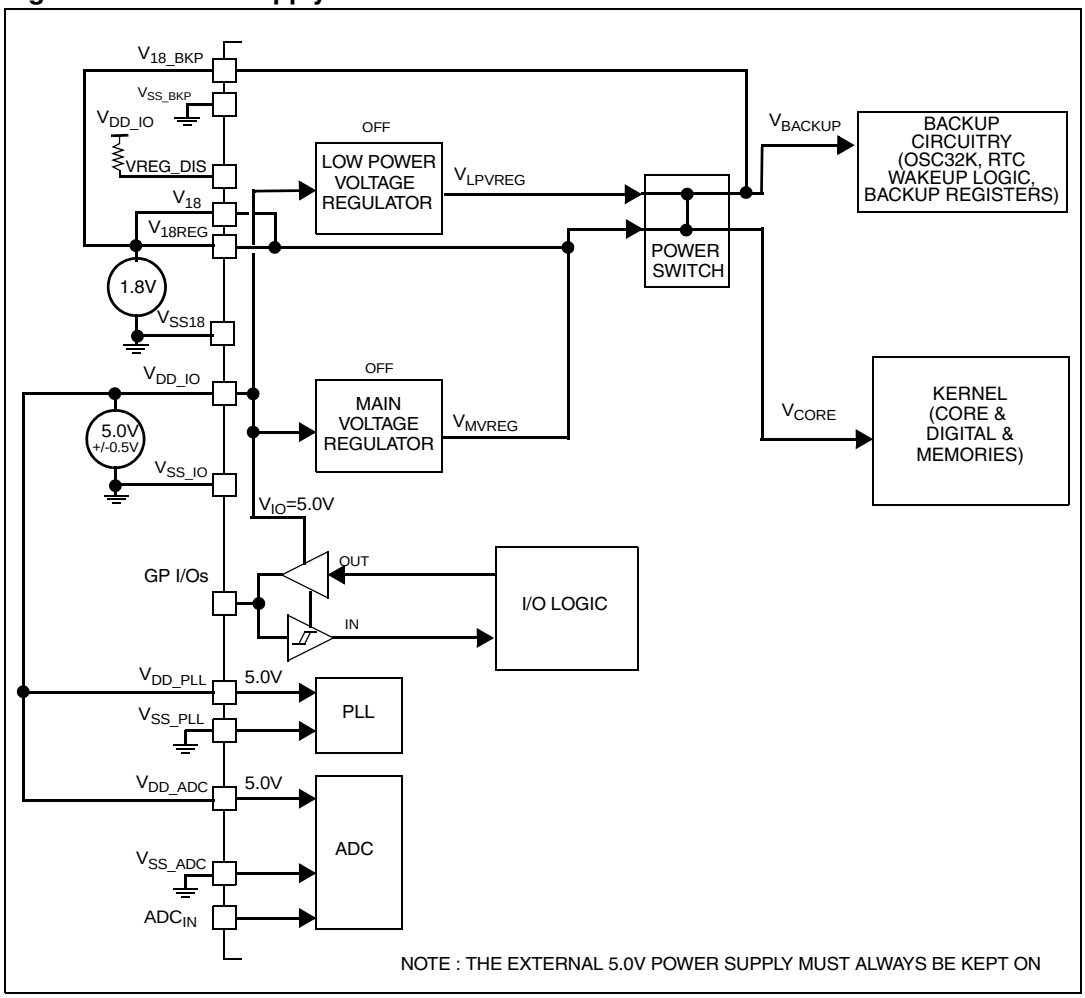
Power supply scheme 3: Single external 5 V power source

Figure 10. Power supply scheme 3



Power supply scheme 4: Dual external 1.8 V and 5.0 V supply

Figure 11. Power supply scheme 4



6.1.7 I/O characteristics versus the various power schemes (3.3V or 5.0V)

Unless otherwise mentioned, all the I/O characteristics are valid for both

- V_{DD_IO}=3.0 V to 3.6 V with bit EN33=1
- V_{DD_IO}=4.5 V to 5.5 V with bit EN33=0

When V_{DD_IO}=3.0 V to 3.6 V, I/Os are not 5V tolerant.

6.1.8 Current consumption measurements

All the current consumption measurements mentioned below refer to Power scheme 1 and 2 as described in *Figure 12* and *Figure 13*

Figure 12. Power consumption measurements in power scheme 1 (regulators enabled)

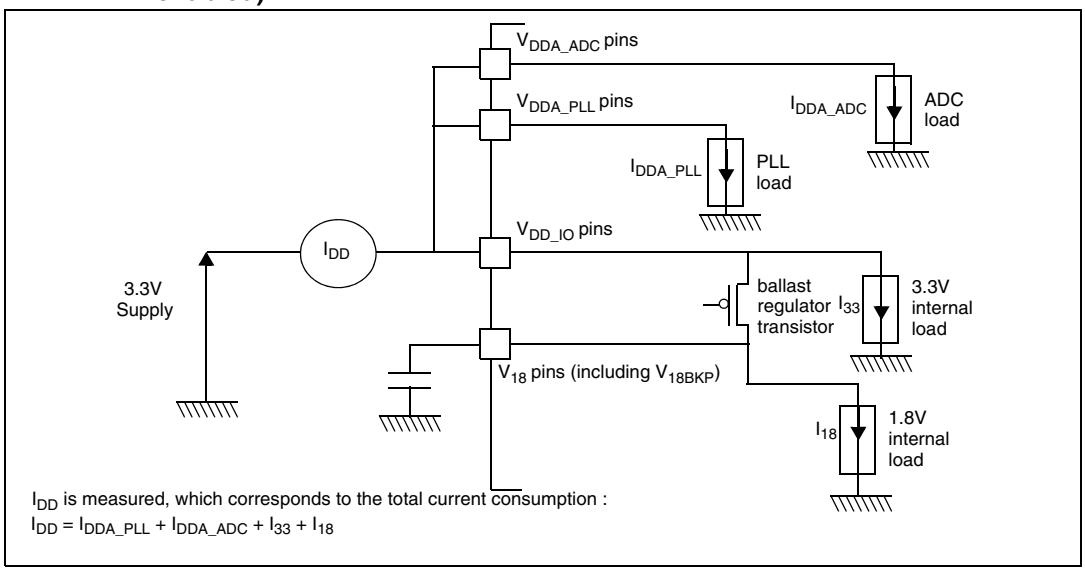


Figure 13. Power consumption measurements in power scheme 2 (regulators disabled)

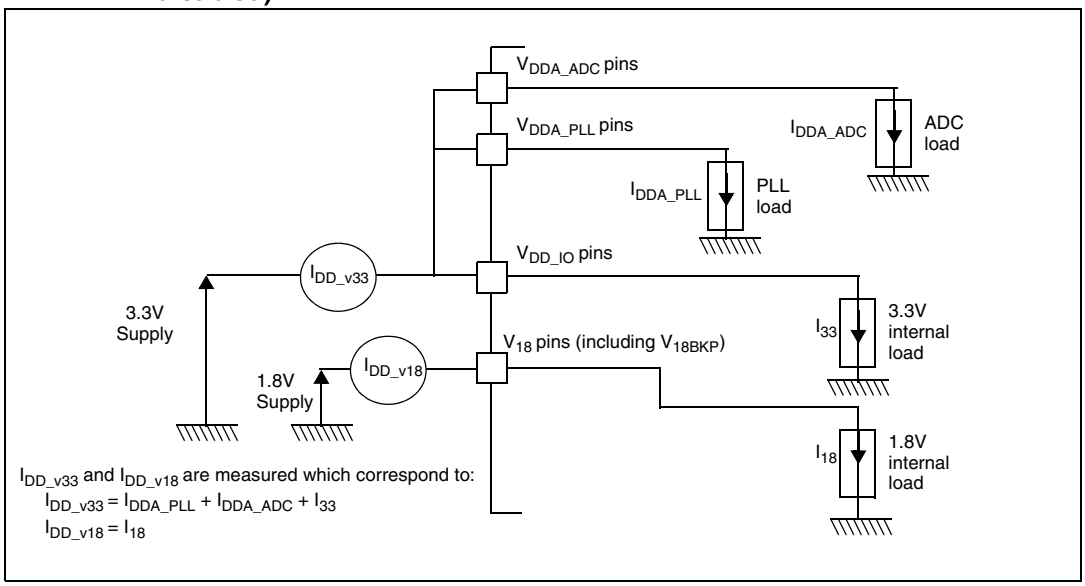


Figure 14. Power consumption measurements in power scheme 3 (regulators enabled)

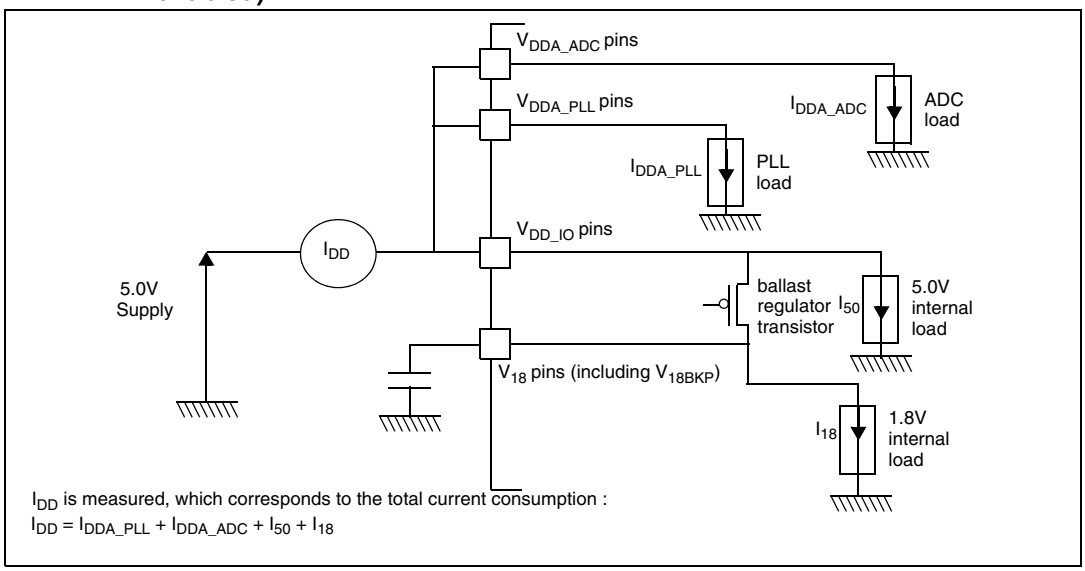
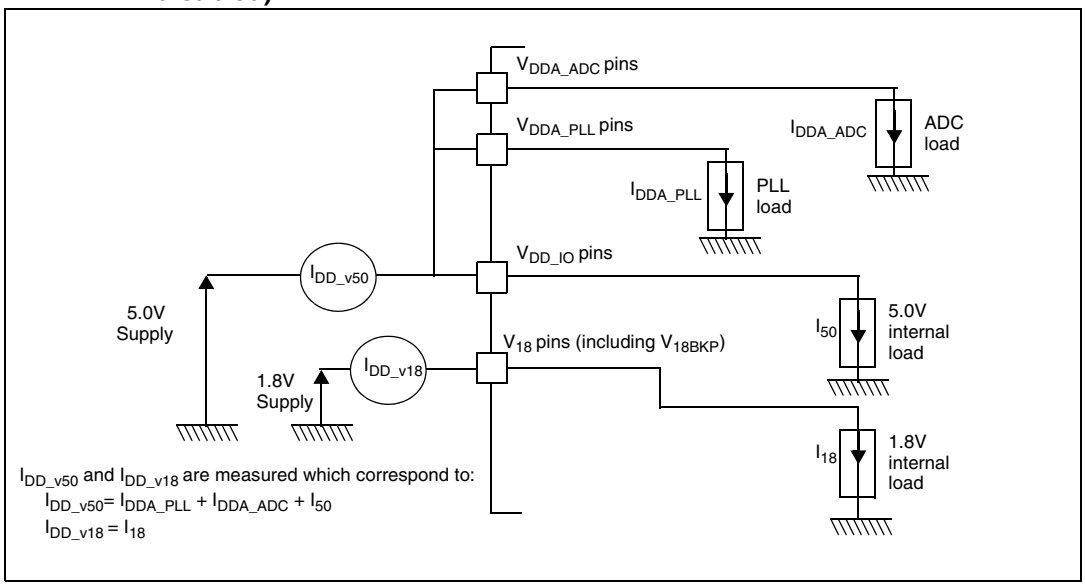


Figure 15. Power consumption measurements in power scheme 4 (regulators disabled)



6.3 Operating conditions

6.3.1 General operating conditions

Subject to general operating conditions for V_{DD_IO}, and T_A unless otherwise specified.

Table 10. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB Clock frequency	Accessing SRAM with 0 wait states	0	64	MHz
		Accessing Flash in burst mode, $T_A \leq 85°$ C	0	60	
		Accessing Flash in burst mode $T_A > 85°$ C		56	
		Accessing Flash with 0 wait states	0	32	
		Write access to Flash registers(1)	0	30	
		Accessing Flash in RWW mode	0	16	
f_{PCLK}	Internal APB Clock frequency		0	32	MHz
V_{DD_IO}	Standard Operating Voltage Power Scheme 1 & 2		3.0	3.6	V
	Standard Operating Voltage Power Scheme 3 & 4		4.5	5.5	
V_{18}	Standard Operating Voltage Power Scheme 2 & 4		1.65	1.95	
P_D	Power dissipation at $T_A = 85°$ C for suffix 6 or $T_A = 105°$ C for suffix 7(2)	LQFP100		434	mW
		LQFP64		444	
		LFBGA100		487	
		LFBGA64		344	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
		Low power dissipation(3)	-40	105	°C
	Ambient temperature for 7 suffix version	Maximum power dissipation	-40	105	°C
		Low power dissipation (3)	-40	125	°C
T_J	Junction temperature range	6 Suffix Version	-40	105	°C
		7 Suffix Version	-40	125	°C

1. Write access to Flash registers is either a program, erase, set protection or un-set protection operation.
2. If T_A is lower, higher PD values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.2: Thermal characteristics on page 79*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.2: Thermal characteristics on page 79*).

6.3.5 Clock and timing characteristics

XT1 external clock source

Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 20. XT1 external clock source

Symbol	Parameter	Conditions(1) (2)	Min	Typ	Max	Unit
f_{XT1}	External clock source frequency	see *Figure 20*		4	60	MHz
V_{XT1H}	XT1 input pin high level voltage		$0.7xV_{DD\_IO}$		V_{DD_IO}	V
V_{XT1L}	XT1 input pin low level voltage		V_{SS}		$0.3xV_{DD\_IO}$	
$t_{w(XT1H)}$ $t_{w(XT1L)}$	XT1 high or low time (3)		6			ns
$t_{r(XT1)}$ $t_{f(XT1)}$	XT1 rise or fall time (3)				20	
I_L	XTx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD\_IO}$			±1	µA
$C_{IN(XT1)}$	XT1 input capacitance(3)			5		pF
$DuCy_{(XT1)}$	Duty cycle		45		55	%

1. Data based on typical application software.
2. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.
3. Data based on design simulation and/or technology characteristics, not tested in production.

6.3.6 Memory characteristics

Flash memory

Subject to general operating conditions for V_{DD_IO} and V_{18}, T_A = -40 to 105 °C unless otherwise specified.

Table 26. Flash memory characteristics

Symbol	Parameter	Test Conditions	Value		Unit
			Typ	Max(1)	
t_{PW}	Word Program		35		µs
t_{PDW}	Double Word Program		60		µs
t_{PB0}	Bank 0 Program (256K)	Single Word programming of a checker-board pattern	2	4.9(2)	s
t_{PB1}	Bank 1 Program (16K)	Single Word programming of a checker-board pattern	125	224(2)	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed (all 1) Preprogrammed (all 0)	1.54 1.176	2.94(2) 2.38(2)	s
t_{ES}	Sector Erase (8K)	Not preprogrammed (all 1) Preprogrammed (all 0)	392 343	560(2) 532(2)	ms
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed (all 1) Preprogrammed (all 0)	8.0 6.6	13.7 11.2	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed (all 1) Preprogrammed (all 0)	0.9 0.8	1.5 1.3	s
t_{RPD}	Recovery when disabled			20	µs
t_{PSL}	Program Suspend Latency			10	µs
t_{ESL}	Erase Suspend Latency			300	µs

1. Data based on characterisation not tested in production
2. 10K program/erase cycles.

Table 27. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END_B0}	Endurance (Bank 0 sectors)		10			kcycles
N_{END_B1}	Endurance (Bank 1 sectors)		100			kcycles
Y_{RET}	Data Retention	T_A=85° C	20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

1. Data based on characterisation not tested in production.

6.3.7 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electro magnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behaviour is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 28. EMC characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-2	Class A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-4	Class A

Table 33. Output driving current

I/O Output drive characteristics for V_{DD_IO} = 3.0 to 3.6 V and EN33 bit =1 or V_{DD_IO} = 4.5 to 5.5 V and EN33 bit =0						
I/O Type	**Symbol**	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
O2	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+2 mA		0.4	V
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-2 mA	V_{DD_IO}-0.8		
O4	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+4 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-4 mA	V_{DD_IO}-0.8		
O8	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+8 mA		0.4	
		Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time	I_{IO}=+20 mA, $T_A \leq 85°C$ $T_A \geq 85°C$		1.3 1.5	
			I_{IO}=+8 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-8 mA	V_{DD_IO}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS_IO}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD_IO}.

Figure 28. SPI configuration - master mode, single transfer

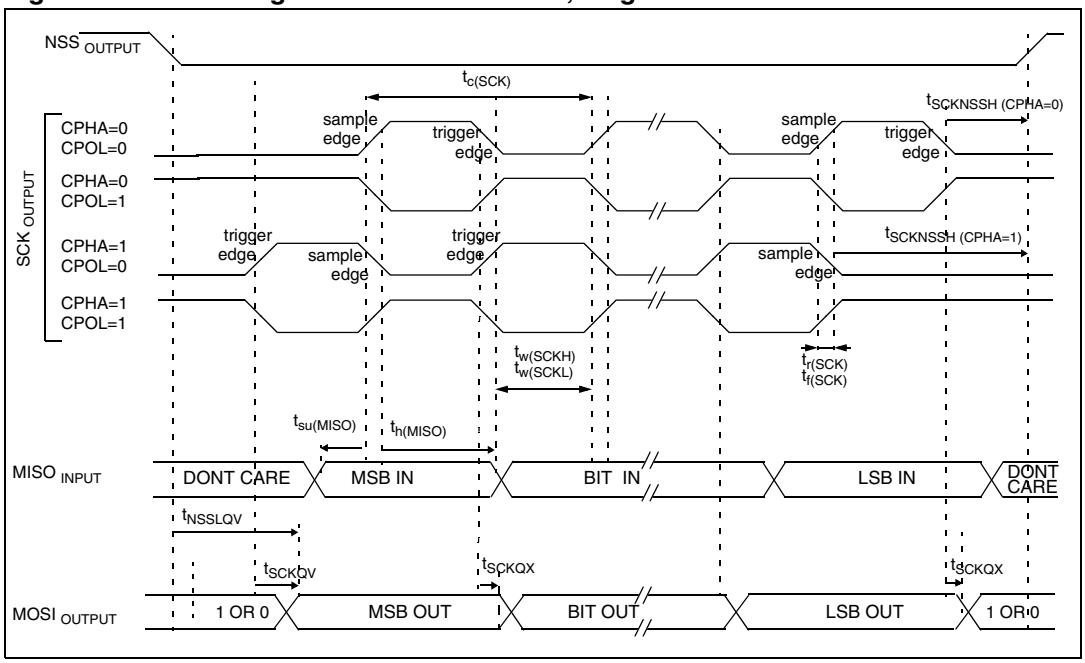


Figure 29. SPI configuration - master mode, continuous transfer, CPHA=0

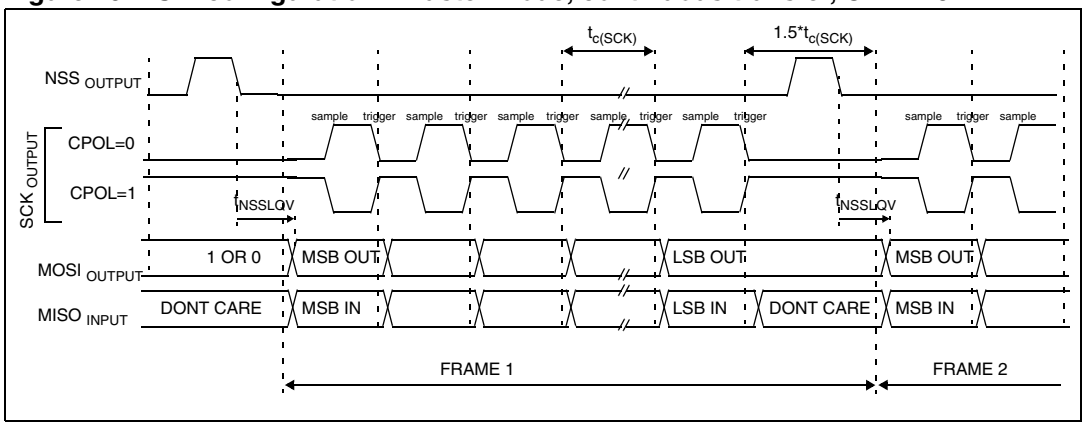
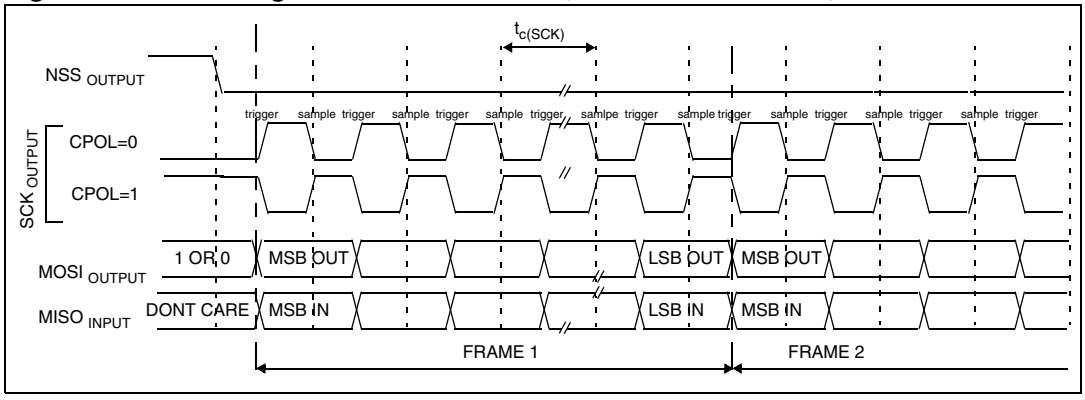


Figure 30. SPI configuration - master mode, continuous transfer, CPHA=1



SSP synchronous serial peripheral in slave mode (SPI or TI mode)

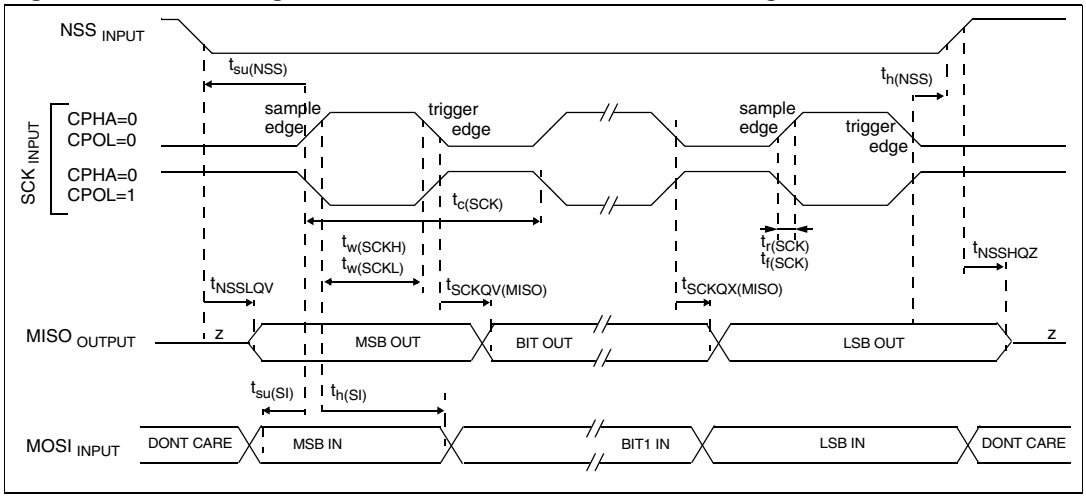
Subject to general operating conditions with $C_L \approx 45$ pF

Table 39. SSP slave mode characteristics(1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK}	SPI clock frequency		SSP0		2.66 MHz (f_{PLCK}/12)	MHz
			SSP1			
$t_{su(NSS)}$	NSS input setup time w.r.t SCK first edge		SSP0	0		ns
			SSP1	0		
$t_{h(NSS)}$	NSS input hold time w.r.t SCK last edge		SSP0	t_{PCLK}+15ns		
			SSP1	t_{PCLK}+15ns		
t_{NSSLQV}	NSS low to Data Output MISO valid time		SSP0	$2t_{PCLK}$	$3t_{PCLK}$+30 ns	
			SSP1	$2t_{PCLK}$	$3t_{PCLK}$+30 ns	
t_{NSSLQZ}	NSS low to Data Output MISO invalid time		SSP0	$2t_{PCLK}$	$3t_{PCLK}$+15 ns	
			SSP1	$2t_{PCLK}$	$3t_{PCLK}$+15 ns	
t_{SCKQV}	SCK trigger edge to data output MISO valid time		SSP0		15	
			SSP1		30	
t_{SCKQX}	SCK trigger edge to data output MISO invalid time		SSP0	$2t_{PCLK}$		
			SSP1	$2t_{PCLK}$		
$t_{su(MOSI)}$	MOSI setup time w.r.t SCK sampling edge		SSP0	0		
			SSP1	0		
$t_{h(MOSI)}$	MOSI hold time w.r.t SCK sampling edge		SSP0	$3t_{PCLK}$+15 ns		
			SSP1	$3t_{PCLK}$+15 ns		

1. Data based on characterisation results, not tested in production.

Figure 33. SPI configuration, slave mode with CPHA=0, single transfer



6.3.11 USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 42. USB startup time

Symbol	Parameter	Conditions	Max	Unit
$t_{STARTUP}$	USB transceiver startup time		1	µs

Table 43. USB characteristics

USB DC Electrical Characteristics					
Symbol	**Parameter**	**Conditions**	**Min.(1)(2)**	**Max.(1)(2)**	**Unit**
Input Levels					
V_{DI}	Differential Input Sensitivity	I(DP, DM)	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	
V_{SE}	Single Ended Receiver Threshold		1.3	2.0	
Output Levels					
V_{OL}	Static Output Level Low	R_L of 1.5 kΩ to 3.6V(3)		0.3	V
V_{OH}	Static Output Level High	R_L of 15 kΩ to V_{SS}(3)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. It is important to be aware that the DP/DM pins are not 5 V tolerant. As a consequence, in case of a a shortcut with Vbus (typ: 5.0V), the protection diodes of the DP/DM pins will be direct biased . This will not damage the device if not more than 50 mA is sunk for longer than 24 hours but the reliability may be affected.
3. R_L is the load connected on the USB drivers

Figure 41. USB: data signal rise and fall time

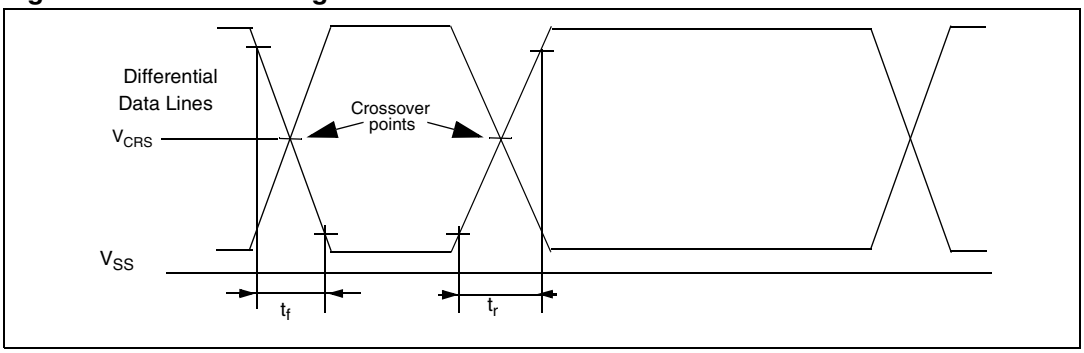


Table 44. USB: Full speed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Driver characteristics:					
t_r	Rise time(1)	C_L=50 pF	4	20	ns
t_f	Fall Time1)	C_L=50 pF	4	20	ns

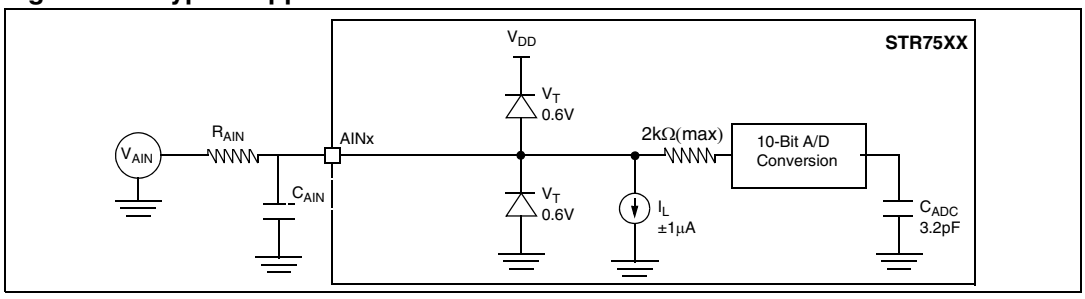
ADC accuracy vs. negative injection current

Injecting negative current on specific pins listed in *Table 46* (generally adjacent to the analog input pin being converted) should be avoided as this significantly reduces the accuracy of the conversion being performed. It is recommended to add a Schottky diode (pin to ground) to pins which may potentially inject negative current.

Table 46. List of adjacent pins

Analog input	Related adjacent pins
a	None
AIN1/P0.03	None
AIN2/P0.12	P0.11
AIN3/P0.17	P0.18 and P0.16
AIN4/P0.19	P0.24
AIN5/P0.22	None
AIN6/P0.23	P2.04
AIN7/P0.27	P1.11 and P0.26
AIN8/P0.29	P0.30 and P0.28
AIN9/P1.04	None
AIN10/P1.06	P1.05
AIN11/P1.08	P1.04 and P1.13
AIN12/P1.11	P2.17 and P0.27
AIN13/P1.12	None
AIN14/P1.13	P1.14 and P1.01
AIN15/P1.14	None

Figure 42. Typical application with ADC



Analog power supply and reference pins

The V_{DDA_ADC} and V_{SSA_ADC} pins are the analog power supply of the A/D converter cell.

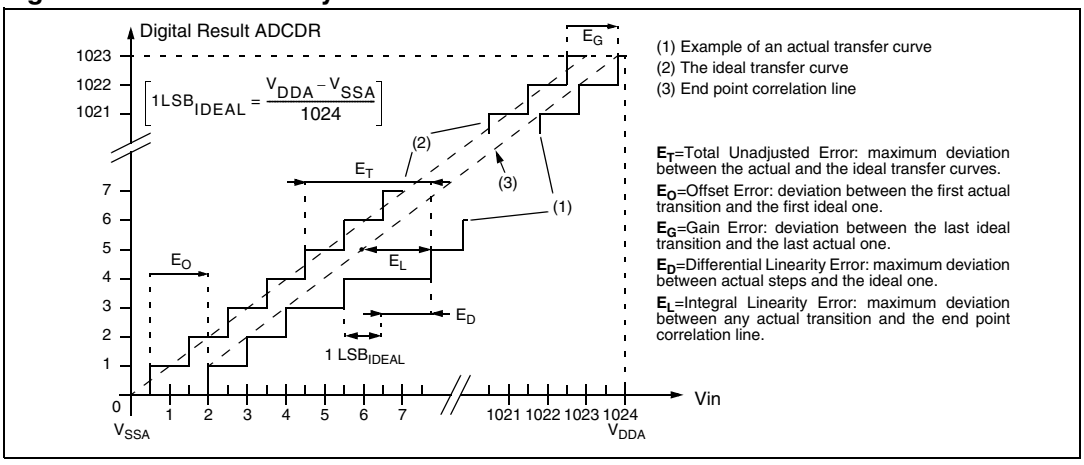
Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see *: General PCB design guidelines on page 74*).

Table 47. ADC accuracy

ADC accuracy with f_{CK_SYS} = 20 MHz, f_{ADC}=8 MHz, R_{AIN} < 10 kΩ This assumes that the ADC is calibrated(1)					
Symbol	**Parameter**	**Conditions**	**Typ**	**Max**	**Unit**
$\|E_T\|$	Total unadjusted error (2) (3)	V_{DDA_ADC}=3.3 V	1	1.2	LSB
		V_{DDA_ADC}=5.0 V	1	1.2	
$\|E_O\|$	Offset error(2) (3)	V_{DDA_ADC}=3.3 V	0.15	0.5	
		V_{DDA_ADC}=5.0 V	0.15	0.5	
E_G	Gain Error (2) (3)	V_{DDA_ADC}=3.3 V	-0.8	-0.2	
		V_{DDA_ADC}=5.0 V	-0.8	-0.2	
$\|E_D\|$	Differential linearity error(2) (3)	V_{DDA_ADC}=3.3 V	0.7	0.9	
		V_{DDA_ADC}=5.0 V	0.7	0.9	
$\|E_L\|$	Integral linearity error (2) (3)	V_{DDA_ADC}=3.3 V	0.6	0.8	
		V_{DDA_ADC}=5.0 V	0.6	0.8	

1. Calibration is needed once after each power-up.
2. Refer to *ADC accuracy vs. negative injection current on page 73*
3. ADC Accuracy vs. MCO (Main Clock Output): the ADC accuracy can be significantly degraded when activating the MCO on pin P0.01 while converting an analog channel (especially those which are close to the MCO pin). To avoid this, when an ADC conversion is launched, it is strongly recommended to disable the MCO.

Figure 44. ADC accuracy characteristics



7.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 10: General operating conditions on page 34*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in ° C/W,
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$),
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum Power Dissipation on Output Pins.
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 48. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 100 - 14 x 14 mm / 0.5 mm pitch	46	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 100 - 10 x 10 x 1.7mm	41	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

8 Order codes

Table 49. Order codes

Order code	Flash Prog. Memory (Bank 0) Kbytes	Package	CAN Periph	USB Periph	Nominal Temp. Range (T_A)
STR750FV0T6	64	LQFP100 14x14	Yes	Yes	-40 to +85°C
STR750FV1T6	128				
STR750FV2T6	256				
STR750FV0H6	64	LFBGA100 10x10			
STR750FV1H6	128				
STR750FV2H6	256				
STR751FR0T6	64	LQFP64 10x10	-	Yes	-40 to +85°C
STR751FR1T6	128				
STR751FR2T6	256				
STR751FR0H6	64	LFBGA64 8x8			
STR751FR1H6	128				
STR751FR2H6	256				
STR752FR0T6	64	LQFP64 10x10	Yes	-	-40 to +85°C
STR752FR1T6	128				
STR752FR2T6	256				
STR752FR0H6	64	LFBGA64 8x8			
STR752FR1H6	128				
STR752FR2H6	256				
STR752FR0T7	64	LQFP64 10x10	Yes	-	-40 to +105°C
STR752FR1T7	128				
STR752FR2T7	256				
STR752FR0H7	64	LFBGA64 8x8			
STR752FR1H7	128				
STR752FR2H7	256				
STR755FR0T6	64	LQFP64 10x10	-	-	-40 to +85°C
STR755FR1T6	128				
STR755FR2T6	256				
STR755FR0H6	64	LFBGA64 8x8			
STR755FR1H6	128				
STR755FR2H6	256				

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