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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, I²C, SPI, SSI, SSP, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str752fr2t6

Contents

Serial memory interface (SMI)

The Serial Memory interface is directly able to access up to 4 serial FLASH devices. It can be used to access data, execute code directly or boot the application from external memory. The memory is addressed as 4 banks of up to 16 Mbytes each.

Clocks and start-up

After RESET or when exiting from Low Power Mode, the CPU is clocked immediately by an internal RC oscillator (FREEOSC) at a frequency centered around 5 MHz, so the application code can start executing without delay. In parallel, the 4/8 MHz Oscillator is enabled and its stabilization time is monitored using a dedicated counter.

An oscillator failure detection is implemented: when the clock disappears on the XT1 pin, the circuit automatically switches to the FREEOSC oscillator and an interrupt is generated.

In Run mode, the AHB and APB clock speeds can be set at a large number of different frequencies thanks to the PLL and various prescalers: up to 60 MHz for AHB and up to 32 MHz for APB when fetching from Flash (64 MHz and 32 MHz when fetching from SRAM).

In SLOW mode, the AHB clock can be significantly decreased to reduce power consumption.

The built-in Clock Controller also provides the 48 MHz USB clock directly without any extra oscillators or PLL. For instance, starting from the 4 MHz crystal source, it is possible to obtain in parallel 60 MHz for the AHB clock, 48 MHz for the USB clock and 30 MHz for the APB peripherals.

Boot modes

At start-up, boot pins are used to select one of five boot options:

- Boot from internal flash
- Boot from external serial Flash memory
- Boot from internal boot loader
- Boot from internal SRAM

Booting from SMI memory allows booting from a serial flash. This way, a specific boot monitor can be implemented. Alternatively, the STR750F can boot from the internal boot loader that implements a boot from UART.

Power supply schemes

You can connect the device in any of the following ways depending on your application.

- **Power Scheme 1: Single external 3.3V power source**. In this configuration the V_{CORE} supply required for the internal logic is generated internally by the main voltage regulator and the V_{BACKUP} supply is generated internally by the low power voltage regulator. This scheme has the advantage of requiring only one 3.3V power source.
- **Power Scheme 2: Dual external 3.3V and 1.8V power sources.** In this configuration, the internal voltage regulators are switched off by forcing the VREG_DIS pin to high level. V_{CORE} is provided externally through the V_{18} and V_{18REG} power pins and V_{BACKUP} through the V_{18_BKP} pin. This scheme is intended to save power consumption for applications which already provide an 1.8V power supply.
- **Power Scheme 3: Single external 5.0V power source.** In this configuration the V_{CORE} supply required for the internal logic is generated internally by the main voltage

I²C bus

The I²C bus interface can operate in multi-master and slave mode. It can support standard and fast modes (up to 400KHz).

High speed universal asynch. receiver transmitter (UART)

The three UART interfaces are able to communicate at speeds of up to 2 Mbit/s. They provide hardware management of the CTS and RTS signals and have LIN Master capability.

To optimize the data transfer between the processor and the peripheral, two FIFOs (receive/transmit) of 16 bytes each have been implemented.

One UART can be served by the DMA controller (UART0).

Synchronous serial peripheral (SSP)

The two SSPs are able to communicate up to 8 Mbit/s (SSP1) or up to 16 Mbit/s (SSP0) in standard full duplex 4-pin interface mode as a master device or up to 2.66 Mbit/s as a slave device. To optimize the data transfer between the processor and the peripheral, two FIFOs (receive/transmit) of 8 x 16 bit words have been implemented. The SSPs support the Motorola SPI or TI SSI protocols.

One SSP can be served by the DMA controller (SSP0).

Controller area network (CAN)

The CAN is compliant with the specification 2.0 part B (active) with a bit rate up to 1Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Up to 32 message objects are handled through an internal RAM buffer. In LQFP64 devices, CAN and USB cannot be connected simultaneously.

Universal serial bus (USB)

The STR750F embeds a USB device peripheral compatible with the USB Full speed 12Mbs. The USB interface implements a full speed (12 Mbit/s) function interface. It has software configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock source is generated from the internal main PLL. V_{DD} must be in the range 3.3V±10% for USB operation.

ADC (analog to digital converter)

The 10-bit Analog to Digital Converter, converts up to 16 external channels (11 channels in 64-pin devices) in single-shot or scan modes. In scan mode, continuous conversion is performed on a selected group of analog inputs. The minimum conversion time is 3.75 µs (including the sampling time).
The ADC can be served by the DMA controller.

An analog watchdog feature allows you to very precisely monitor the converted voltage of up to four channels. An IRQ is generated when the converted voltage is outside the programmed thresholds.

The events generated by TIM0, TIM2 and PWM timers can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

GPIOs (general purpose input/output)

Each of the 72 GPIO pins (38 GPIOs in 64-pin devices) can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as Peripheral Alternate Function. Port 1.15 is an exception, it can be used as general-purpose input only or wake-up from STANDBY mode (WKP_STDBY). Most of the GPIO pins are shared with digital or analog alternate functions.

4.1 Pin description table

Legend / abbreviations for *Table 6*:

Type:	I = input, O = output, S = supply,
Input levels:	All Inputs are LVTTL at V_{DD_IO} = 3.3V+/-0.3V or TTL at V_{DD_IO} = 5V± 0.5V. In both cases, T_T means V_{ILmax} =0.8V V_{IHmin}=2.0V
Inputs:	All inputs can be configured as floating or with internal weak pull-up or pull down (pu/pd)
Outputs:	All Outputs can be configured as Open Drain (OD) or Push-Pull (PP) (see also note 6 below *Table 6*). There are 3 different types of Output with different drives and speed characteristics: – O8: f_{max} = 40 MHz on C_L=50pF and 8 mA static drive capability for V_{OL}=0.4V and up to 20 mA for V_{OL}=1.3V (see*Output driving current on page 55*) – O4: f_{max} = 20 MHz on C_L=50pF and 4 mA static drive capability for V_{OL}=0.4V (see*Output driving current on page 55*) – O2: f_{max} = 10 MHz on C_L=50pF and 2 mA static drive capability of for V_{OL}=0.4V (see*Output driving current on page 55*)
External interrupts/wake-up lines:	EITx

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
91	A4	59	A3	P1.04 / PWM3N / ADC_IN9	I/O	T_T	**X**	X		O4	X	X		**Port 1.04**	PWM: PWM3 complementary output(4)	ADC: analog input 9
92	A3			P1.14 / ADC_IN15	I/O	T_T	**X**	X		O8	X	X		**Port 1.14**	ADC: analog input 15	
93	A2			P1.13 / ADC_IN14	I/O	T_T	**X**	X	EIT13	O8	X	X		**Port 1.13**	ADC: analog input 14	
94	D5			P1.01 / TIM0_TI2	I/O	T_T	**X**	X		O2	X	X		**Port 1.01**	TIM0: Input Capture / trigger / external clock 2 (remappable to P0.05)(8)	
95	E6			P1.00 / TIM0_OC2	I/O	T_T	**X**	X		O2	X	X		**Port 1.00**	TIM0: Output compare 2 (remappable to P0.04)(8)	
96	C4	60	C4	V18	S									Stabilization for main voltage regulator. Requires external capacitors 33nF between V18 and VSS18. See *Figure 4.2*. To be connected to the 1.8V external power supply when embedded regulators are not used.		
97	D4	61	C5	VSS18	S									Ground Voltage for the main voltage regulator.		
98	D3	62	A2	VSS_IO	S									Ground Voltage for digital I/Os		
99	C3	63	B2	VDD_IO	S									Supply Voltage for digital I/Os		
100	A1	64	A1	P0.03 / TIM2_TI1 / ADC_IN1	I/O	T_T	**X**	X		O2	X	X		**Port 0.03**	TIM2: Input Capture / trigger / external clock 1	ADC: analog input 1

1. For STR755FVx part numbers, the USB pins must be left unconnected.
2. The non available pins on LQPFP64 and LFBGA64 packages are internally tied to low level.
3. None of the I/Os are True Open Drain: when configured as Open Drain, there is always a protection diode between the I/O pin and VDD_IO.
4. In the 100-pin package, this Alternate Function is duplicated on two ports. You can configure one port to use this AF, the other port is then free for general purpose I/O (GPIO), external interrupt/wake-up lines, or analog input (ADC_IN) where these functions are listed in the table.
5. It is mandatory that the NJTRST pin is reset to ground during the power-up phase. It is recommended to connect this pin to NRSTOUT pin (if available) or NRSTIN.
6. After reset, these pins are enabled as JTAG alternate function see (*Port reset state on page 16*). To use these ports as general purpose I/O (GPIO), the DBGOFF control bit in the GPIO_REMAP0R register must be set by software (in this case, debugging these I/Os via JTAG is not possible).
7. There are two different TQFP and BGA 64-pin packages: in the first one, pins 41 and 42 are mapped to USB DN/DP while for the second one, they are mapped to P0.15/CAN_TX and P0.14/CAN_RX.
8. For details on remapping these alternate functions, refer to the GPIO_REMAP0R register description.

6.1.6 Power supply schemes

When mentioned, some electrical parameters can refer to a dedicated power scheme among the four possibilities. The four different power schemes are described below.

Power supply scheme 1: Single external 3.3 V power source

Figure 8. Power supply scheme 1

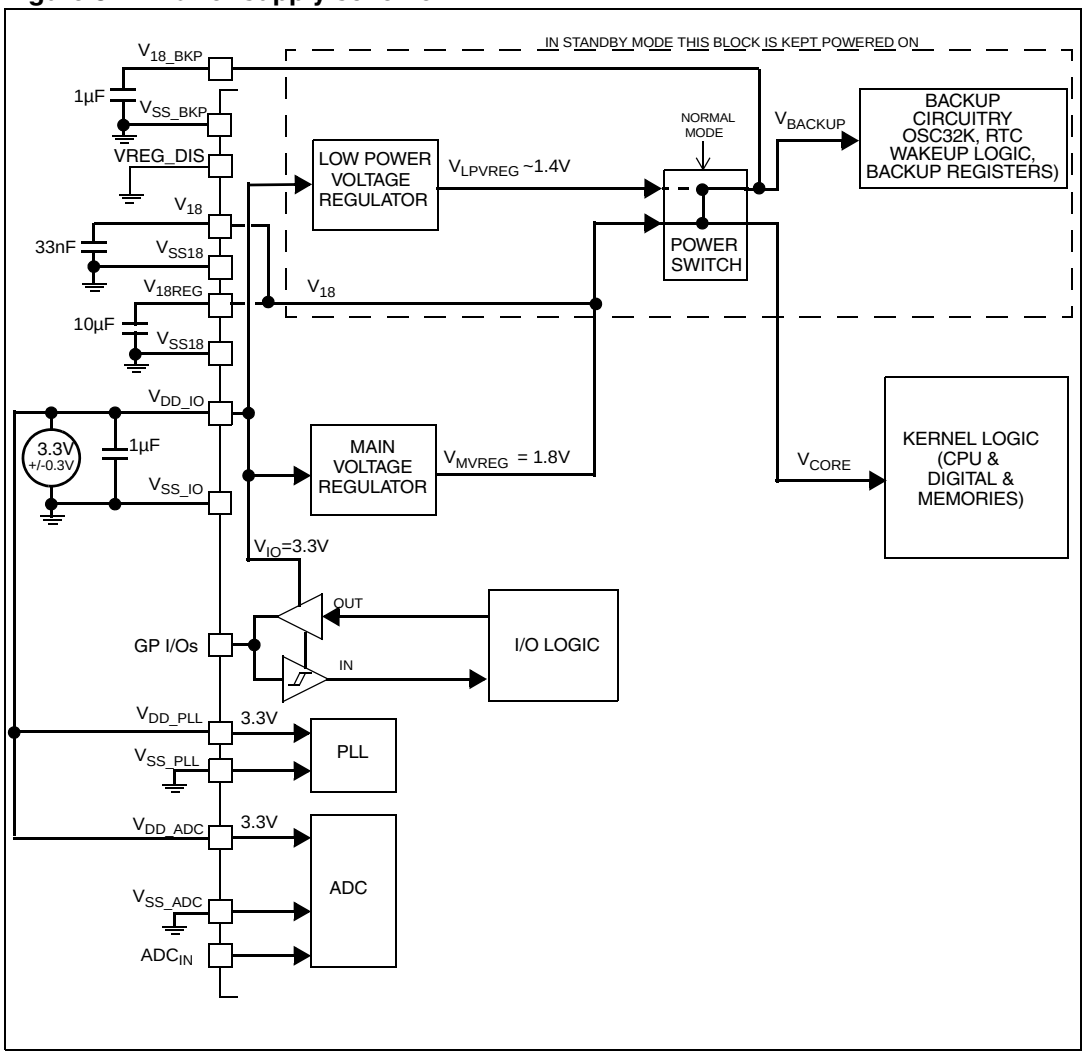


Figure 12. Power consumption measurements in power scheme 1 (regulators enabled)

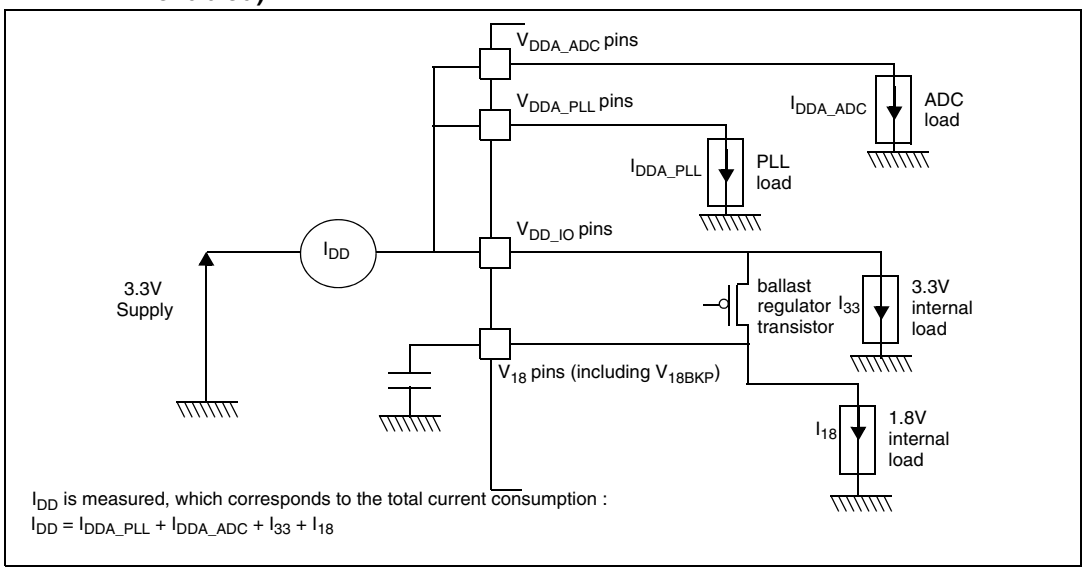
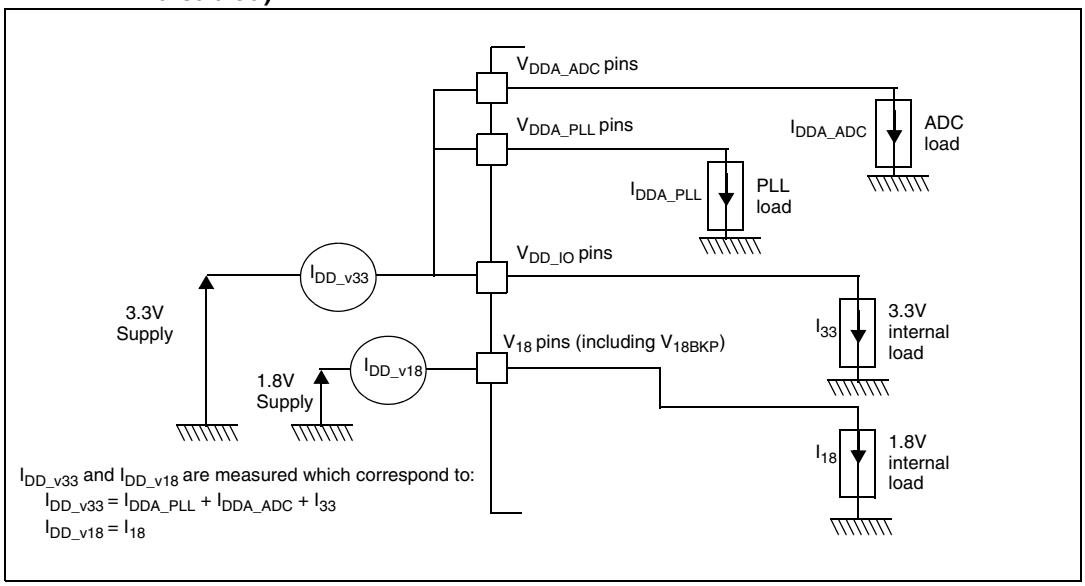


Figure 13. Power consumption measurements in power scheme 2 (regulators disabled)



6.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 11. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{VDD_IO}	V_{DD_IO} rise time rate		20			µs/V
					20	ms/V
t_{V18}	V_{18} rise time rate (1)	When 1.8 V power is supplied externally	20			µs/V
					20	ms/V

1. Data guaranteed by characterization, not tested in production.

6.3.3 Embedded voltage regulators

Subject to general operating conditions for V_{DD_IO}, and T_A

Table 12. Embedded voltage regulators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{MVREG}	MVREG power supply(1)	load <150 mA	1.65	1.80	1.95	V
V_{LPVREG}	LPVREG power supply(2)	load <10 mA	1.30	1.40	1.50	V
t_{VREG_PWRUP}(1)	Voltage Regulators start-up time (to reach 90% of final V_{18} value) at V_{DD_IO} power-up(3)	V_{DD_IO} rise slope = 20 µs/V		80		µs
		V_{DD_IO} rise slope = 20 ms/V		35		ms

1. V_{MVREG} is observed on the V_{18}, V_{18REG} and V_{18BKP} pins except in the following case:
   - In STOP mode with MVREG OFF (LP_PARAM13 bit). See note 2.
   - In STANDBY mo*de. See note 2.*
2. In STANDBY mode, V_{LPVREG} is observed on the V_{18BKP} pin
   In STOP mode, V_{LPVREG} is observed on the V_{18}, V_{18REG} and V_{18BKP} pins.
3. Once V_{DD_IO} has reached 3.0 V, the RSM (Regulator Startup Monitor) generates an internal RESET during this start-up time.

6.3.4 Supply current characteristics

The current consumption is measured as described in *Figure 12 on page 30* and *Figure 13 on page 30*.

Subject to general operating conditions for V_{DD_IO}, and T_A

Maximum power consumption

For the measurements in *Table 13* and *Table 14*, the MCU is placed under the following conditions:

- All I/O pins are configured in output push-pull 0
- All peripherals are disabled except if explicitly mentioned.
- Embedded Regulators are used to provide 1.8 V (except if explicitly mentioned).

Table 13. Maximum power consumption in RUN and WFI modes

Symbol	Parameter	Conditions (1)		Typ (2)	Max (3)	Unit
I_{DD}	Supply current in RUN mode	External Clock with PLL multiplication, code running from RAM, all peripherals enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz Single supply scheme see *Figure 12* / *Figure 14*	3.3V and 5V range	80	90	mA
	Supply current in WFI mode	External Clock, code running from RAM: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz Single supply scheme see *Figure 12*./ *Figure 14* Parameter setting BURST=1, WFI_FLASHEN=1	3.3V and 5V range	62	67	mA

1. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4*.
2. Typical data are based on T_A=25°C, V_{DD_IO}=3.3V or 5.0V and V_{18}=1.8V unless otherwise specified.
3. Data based on product characterisation, tested in production at V_{DD_IO} max and V_{18} max (1.95V in dual supply mode or regulator output value in single supply mode) and T_A max.

On-Chip peripheral power consumption

Conditions:

- V_{DD_IO}=V_{DDA_ADC}=V_{DDA_PLL}=3.3 V or 5 V ±10% unless otherwise specified.
- T_A= 25° C
- Clocked by OSC4M with PLL multiplication, f_{CK_SYS}=64 MHz, f_{HCLK}=32 MHz, f_{PCLK}=32 MHz

Table 19. On-Chip peripherals

Symbol	Parameter	Typ (3.3V and 5.0V)	Unit
$I_{DD(TIM)}$	TIM Timer supply current (1)	0.7	mA
$I_{DD(PWM)}$	PWM Timer supply current(2)	1	
$I_{DD(SSP)}$	SSP supply current (3)	1.3	
$I_{DD(UART)}$	UART supply current (4)	1.6	
$I_{DD(I2C)}$	I2C supply current (5)	0.3	
$I_{DD(ADC)}$	ADC supply current when converting (6)	1.2	
$I_{DD(USB)}$	USB supply current (7) **Note:** V_{DD_IO} must be 3.3 V ±10%	0.90	
$I_{DD(CAN)}$	CAN supply current (8)	2.8	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 32 MHz. No IC/OC programmed (no I/O pads toggling)
2. Data based on a differential I_{DD} measurement between reset configuration and PWM running at 32 MHz. This measurement does not include PWM pads toggling consumption.
3. Data based on a differential I_{DD} measurement between reset configuration and permanent SPI master communication at maximum speed 16 MHz. The data sent is 55h. This measurement does not include the pad toggling consumption.
4. Data based on a differential I_{DD} measurement between reset configuration and a permanent UART data transmit sequence at 1Mbauds. This measurement does not include the pad toggling consumption.
5. Data based on a differential I_{DD} measurement between reset configuration (I2C disabled) and a permanent I2C master communication at 100kHz (data sent equal to 55h). This measurement includes the pad toggling consumption but not the external 10kOhm external pull-up on clock and data lines.
6. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions at 8 MHz in scan mode on 16 inputs configured as AIN.
7. Data based on a differential I_{DD} measurement between reset configuration and a running generic HID application.
8. Data based on a differential IDD measurement between reset configuration (CAN disabled) and a permanent CAN data transmit sequence in loopback mode at 1MHz. This measurement does not include the pad toggling consumption.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 31. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A=+25° C T_A=+85° C T_A=+105° C	Class A
DLU	Dynamic latch-up class	V_{DD}= 5.5 V, f_{OSC4M}=4 MHz, f_{CK_SYS}=32 MHz, T_A=+25° C	Class A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

Table 33. Output driving current

I/O Output drive characteristics for V_{DD_IO} = 3.0 to 3.6 V and EN33 bit =1 or V_{DD_IO} = 4.5 to 5.5 V and EN33 bit =0						
I/O Type	**Symbol**	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
O2	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+2 mA		0.4	V
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-2 mA	V_{DD_IO}-0.8		
O4	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+4 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-4 mA	V_{DD_IO}-0.8		
O8	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+8 mA		0.4	
		Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time	I_{IO}=+20 mA, $T_A \leq 85°C$ $T_A \geq 85°C$		1.3 1.5	
			I_{IO}=+8 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-8 mA	V_{DD_IO}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS_IO}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD_IO}.

Figure 31. TI configuration - master mode, single transfer

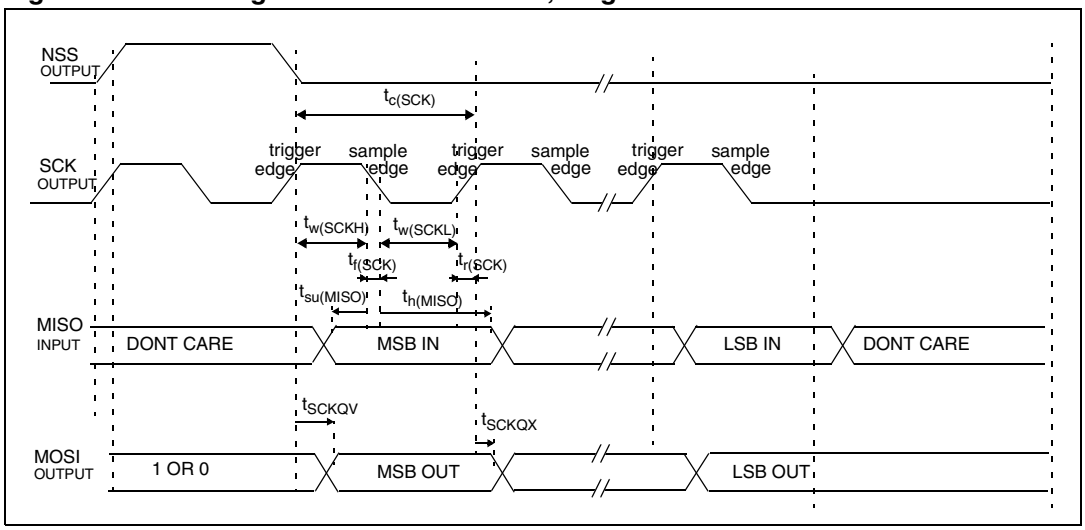
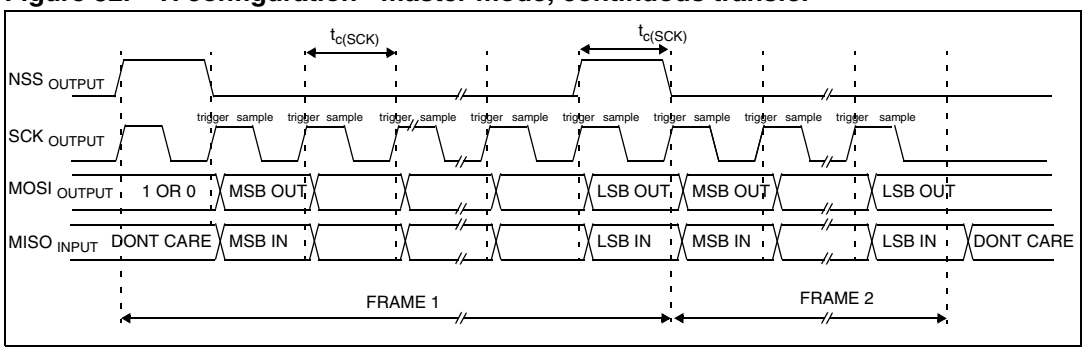


Figure 32. TI configuration - master mode, continuous transfer



SSP synchronous serial peripheral in slave mode (SPI or TI mode)

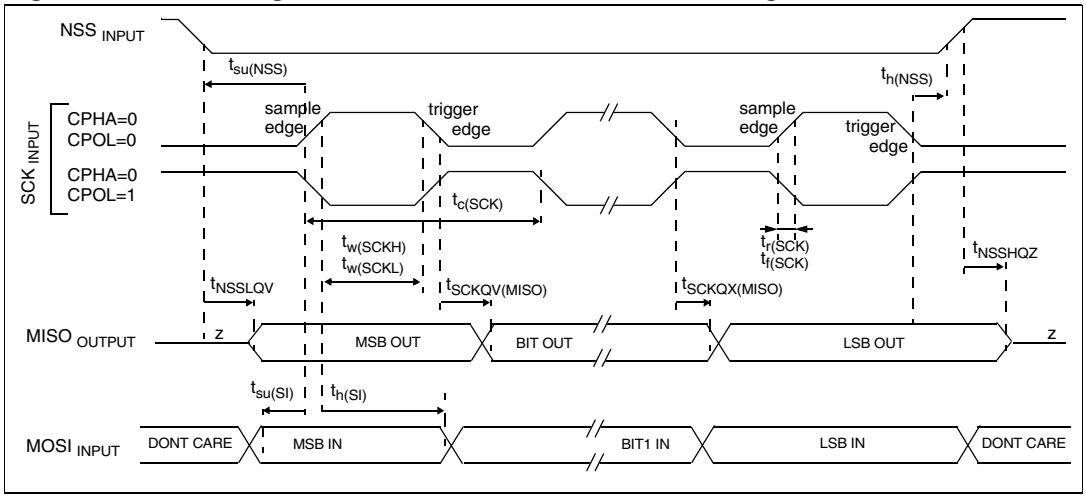
Subject to general operating conditions with $C_L \approx 45$ pF

Table 39. SSP slave mode characteristics(1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK}	SPI clock frequency		SSP0		2.66 MHz (f_{PLCK}/12)	MHz
			SSP1			
$t_{su(NSS)}$	NSS input setup time w.r.t SCK first edge		SSP0	0		ns
			SSP1	0		
$t_{h(NSS)}$	NSS input hold time w.r.t SCK last edge		SSP0	t_{PCLK}+15ns		
			SSP1	t_{PCLK}+15ns		
t_{NSSLQV}	NSS low to Data Output MISO valid time		SSP0	$2t_{PCLK}$	$3t_{PCLK}$+30 ns	
			SSP1	$2t_{PCLK}$	$3t_{PCLK}$+30 ns	
t_{NSSLQZ}	NSS low to Data Output MISO invalid time		SSP0	$2t_{PCLK}$	$3t_{PCLK}$+15 ns	
			SSP1	$2t_{PCLK}$	$3t_{PCLK}$+15 ns	
t_{SCKQV}	SCK trigger edge to data output MISO valid time		SSP0		15	
			SSP1		30	
t_{SCKQX}	SCK trigger edge to data output MISO invalid time		SSP0	$2t_{PCLK}$		
			SSP1	$2t_{PCLK}$		
$t_{su(MOSI)}$	MOSI setup time w.r.t SCK sampling edge		SSP0	0		
			SSP1	0		
$t_{h(MOSI)}$	MOSI hold time w.r.t SCK sampling edge		SSP0	$3t_{PCLK}$+15 ns		
			SSP1	$3t_{PCLK}$+15 ns		

1. Data based on characterisation results, not tested in production.

Figure 33. SPI configuration, slave mode with CPHA=0, single transfer



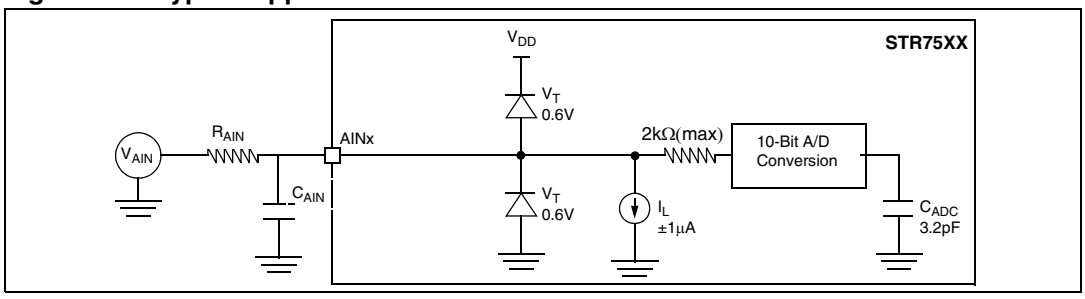
ADC accuracy vs. negative injection current

Injecting negative current on specific pins listed in *Table 46* (generally adjacent to the analog input pin being converted) should be avoided as this significantly reduces the accuracy of the conversion being performed. It is recommended to add a Schottky diode (pin to ground) to pins which may potentially inject negative current.

Table 46. List of adjacent pins

Analog input	Related adjacent pins
a	None
AIN1/P0.03	None
AIN2/P0.12	P0.11
AIN3/P0.17	P0.18 and P0.16
AIN4/P0.19	P0.24
AIN5/P0.22	None
AIN6/P0.23	P2.04
AIN7/P0.27	P1.11 and P0.26
AIN8/P0.29	P0.30 and P0.28
AIN9/P1.04	None
AIN10/P1.06	P1.05
AIN11/P1.08	P1.04 and P1.13
AIN12/P1.11	P2.17 and P0.27
AIN13/P1.12	None
AIN14/P1.13	P1.14 and P1.01
AIN15/P1.14	None

Figure 42. Typical application with ADC



Analog power supply and reference pins

The V_{DDA_ADC} and V_{SSA_ADC} pins are the analog power supply of the A/D converter cell.

Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see *: General PCB design guidelines on page 74*).

General PCB design guidelines

To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 µF and optionally, if needed 10 pF capacitors as close as possible to the STR7 power supply pins and a 1 to 10 µF capacitor close to the power source (see *Figure 43*).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{DDA_ADC} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs near the A/D input being converted.

Software filtering of spurious conversion results

For EMC performance reasons, it is recommended to filter A/D conversion outliers using software filtering techniques.

Figure 43. Power supply filtering

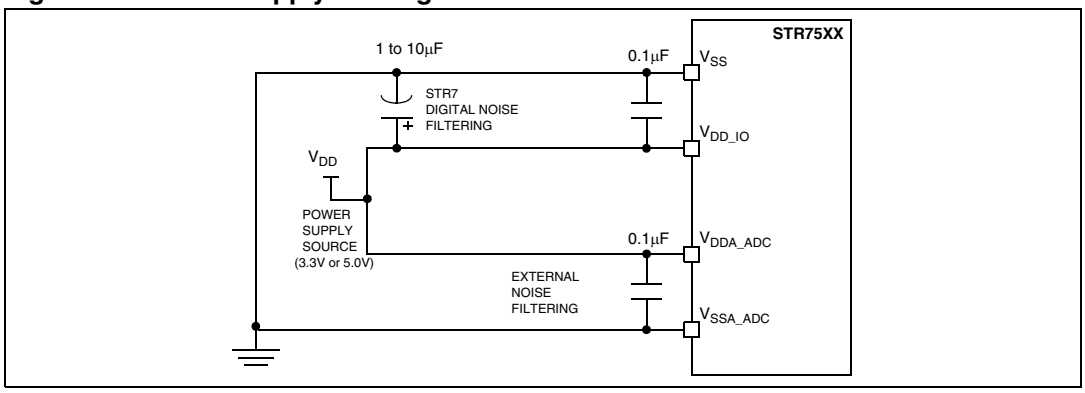
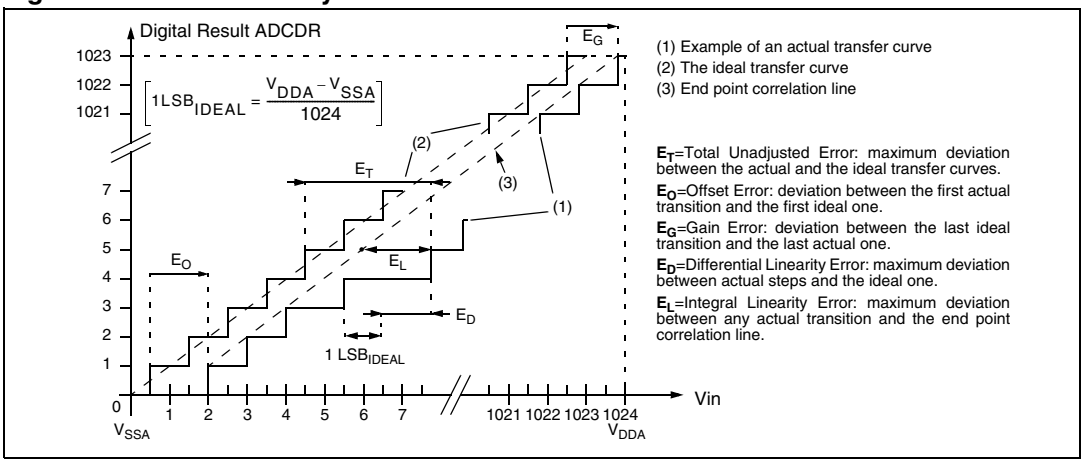


Table 47. ADC accuracy

ADC accuracy with f_{CK_SYS} = 20 MHz, f_{ADC}=8 MHz, R_{AIN} < 10 kΩ This assumes that the ADC is calibrated(1)					
Symbol	**Parameter**	**Conditions**	**Typ**	**Max**	**Unit**
$\|E_T\|$	Total unadjusted error (2) (3)	V_{DDA_ADC}=3.3 V	1	1.2	LSB
		V_{DDA_ADC}=5.0 V	1	1.2	
$\|E_O\|$	Offset error(2) (3)	V_{DDA_ADC}=3.3 V	0.15	0.5	
		V_{DDA_ADC}=5.0 V	0.15	0.5	
E_G	Gain Error (2) (3)	V_{DDA_ADC}=3.3 V	-0.8	-0.2	
		V_{DDA_ADC}=5.0 V	-0.8	-0.2	
$\|E_D\|$	Differential linearity error(2) (3)	V_{DDA_ADC}=3.3 V	0.7	0.9	
		V_{DDA_ADC}=5.0 V	0.7	0.9	
$\|E_L\|$	Integral linearity error (2) (3)	V_{DDA_ADC}=3.3 V	0.6	0.8	
		V_{DDA_ADC}=5.0 V	0.6	0.8	

1. Calibration is needed once after each power-up.
2. Refer to *ADC accuracy vs. negative injection current on page 73*
3. ADC Accuracy vs. MCO (Main Clock Output): the ADC accuracy can be significantly degraded when activating the MCO on pin P0.01 while converting an analog channel (especially those which are close to the MCO pin). To avoid this, when an ADC conversion is launched, it is strongly recommended to disable the MCO.

Figure 44. ADC accuracy characteristics



7.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 10: General operating conditions on page 34*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in ° C/W,
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$),
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum Power Dissipation on Output Pins.
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 48. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 100 - 14 x 14 mm / 0.5 mm pitch	46	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 100 - 10 x 10 x 1.7mm	41	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

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