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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, I²C, SPI, SSI, SSP, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str752fr2t7

Table 4. LFBGA100 ball connections

	1	2	3	4	5	6	7	8	9	10
A	P0.03	P1.13	P1.14	P1.04	P1.06	P1.08	P0.05	P0.06	P0.07	P1.02
B	P1.12	P0.02	P0.01	P1.05	P1.07	P1.09	P0.04	P2.13	P1.03	P2.10
C	P0.31	P0.00	V_{DD_IO}	V_{18}	P1.10	P2.09	V_{SS_IO}	V_{SSA_ADC}	P2.11	USB_DP
D	P0.29	P0.30	V_{SS_IO}	V_{SS18}	P1.01	P1.15	V_{DD_IO}	V_{DDA_ADC}	P2.12	USB_DN
E	P0.28	P0.23	P0.22	V_{SS_IO}	TEST	P1.00	NRSTOUT	VREG_DIS	NRSTIN	P0.14
F	P2.03	P0.21	P0.20	P2.02	P2.04	P2.05	P2.06	V_{SS18}	V_{SSBKP}	P0.15
G	NJTRST	P1.18	P1.19	P2.01	P2.00	P2.07	2.08	V_{18REG}	V_{18BKP}	XRTC2
H	P0.13	P1.16	P1.17	P2.19	P2.18	P2.17	P0.24	P2.14	P2.16	XRTC1
J	P0.11	P0.12	P1.11	P0.27	P0.19	P0.26	P0.25	P2.15	V_{DD_IO}	V_{SS_IO}
K	P0.10	P0.09	P0.08	P0.18	P0.17	P0.16	XT1	XT2	V_{DDA_PLL}	V_{SSA_PLL}

Table 5. LFBGA64 ball connections

	1	2	3	4	5	6	7	8
A	P0.03	V_{SS_IO}	P1.04	P1.06	P1.08	P0.05	P0.06	P0.07
B	P1.12	V_{DD_IO}	P1.05	P1.07	P1.09	P0.04	P1.10	P1.03
C	P0.01	P0.02	P0.00	V_{18}	V_{SS18}	V_{DD_IO}	V_{SS_IO}	P0.14
D	P0.29	P0.28	TEST	V_{SS_IO}	VREG_DIS	V_{DDA_ADC}	V_{SSA_ADC}	P0.15
E	P1.18	P1.19	P0.20	P0.21	NRSTOUT	NRSTIN	V_{18BKP}	XRTC2
F	P0.13	NJTRST	P1.16	P1.17	V_{18REG}	V_{SS18}	V_{SSBKP}	XRTC1
G	P0.11	P0.12	P1.11	P0.19	V_{DD_IO}	V_{SS_IO}	V_{DDA_PLL}	V_{SSA_PLL}
H	P0.10	P0.09	P0.08	P0.17	P0.18	P0.16	XT2	XT1

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
26	J2	17	G2	P0.12 / UART2_RX / UART0_CTS / ADC_IN2 / SMI_CS1	I/O	T_T	X	X		O4	X	X		**Port 0.12**	UART0: Clear To Send input	ADC: Analog input 2
															Serial Memory Interface: chip select output 1	UART2: Receive Data input (when remapped)(8)
27	J1	18	G1	P0.11 / UART0_TX / BOOT1 / SMI_CS2	I/O	T_T	X	X		O4	X	X		**Port 0.11/Boot mode selection input 1**	UART0: Transmit data output	Serial Memory Interface: chip select output 2
28	K1	19	H1	P0.10 / UART0_RX / SMI_CS3	I/O	T_T	X	X	EIT4	O2	X	X		**Port 0.10**	UART0: Receive Data input	Serial Memory Interface: chip select output 3
29	K2	20	H2	P0.09 / I2C_SDA	I/O	T_T	X	X		O4	X	X		**Port 0.09**	I2C: Serial Data	
30	K3	21	H3	P0.08 / I2C_SCL	I/O	T_T	X	X	EIT3	O4	X	X		**Port 0.08**	I2C: Serial clock	
31	H4			P2.19	I/O	T_T	X	X		O2	X	X		**Port 2.19**		
32	H5			P2.18	I/O	T_T	X	X		O2	X	X		**Port 2.18**		
33	H6			P2.17 / UART2_RTS	I/O	T_T	X	X		O2	X	X		**Port 2.17**	UART2: Ready To Send output(4)	
34	J3	22	G3	P1.11 /UART0_RTS ADC_IN12	I/O	T_T	X	X	EIT11	O8	X	X		**Port 1.11**	UART0: Ready To Send output(4)	ADC: Analog input 12
35	J4			P0.27 / UART2_RTS / ADC_IN7	I/O	T_T	X	X		O2	X	X		**Port 0.27**	UART2: Ready To Send output(8)	ADC: Analog input 7
36	J6			P0.26 / UART2_CTS	I/O	T_T	X	X		O2	X	X		**Port 0.26**	UART2: Clear To Send input	
37	J7			P0.25 / UART2_TX	I/O	T_T	X	X		O2	X	X		**Port 0.25**	UART2: Transmit data output (remappable to P0.13)(8)	
38	H7			P0.24 / UART2_RX	I/O	T_T	X	X		O2	X	X		**Port 0.24**	UART2: Receive data input (remappable to P0.12)(8)	
39	J5	23	G4	P0.19 / USB_CK / SSP1_NSS / ADC_IN4	I/O	T_T	X	X	EIT6	O2	X	X		**Port 0.19**	SSP1: Slave select input (remappable to P0.11)(8)	ADC: Analog input 4
															USB: 48 MHz Clock input	
40	K4	24	H5	P0.18 / SSP1_MOSI	I/O	T_T	X	X		O2	X	X		**Port 0.18**	SSP1: Master out/slave in data (remappable to P0.10)(8)	
41	K5	25	H4	P0.17 / SSP1_MISO / ADC_IN3	I/O	T_T	X	X		O2	X	X		**Port 0.17**	SSP1: Master in/slave out data (remappable to P0.09)(8)	ADC: Analog input 3
42	K6	26	H6	P0.16 / SSP1_SCLK	I/O	T_T	X	X		O2	X	X		**Port 0.16**	SSP1: serial clock (remappable to P0.08)(8)	

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP			
43	H9			P2.16	I/O	T_T	X	X		O2	X	X		**Port 2.16**	
44	J9	27	G5	VDD_IO	S									Supply voltage for digital I/Os	
45	K9	28	G7	VDDA_PLL	S									Supply voltage for PLL	
46	K8	29	H7	XT2										4 MHz main oscillator	
47	K7	30	H8	XT1											
48	J10	31	G6	VSS_IO	S									Ground voltage for digital I/Os	
49	K10	32	G8	VSSA_PLL	S									Ground voltage for PLL	
50	J8			P2.15	I/O	T_T	X	X		O2	X	X		**Port 2.15**	
51	H8			P2.14	I/O	T_T	X	X		O2	X	X		**Port 2.14**	
52	G8	33	F5	V18REG	S									Stabilization for main voltage regulator. Requires external capacitors of at least 10µF between V18REG and VSS18. See *Figure 4.2*. To be connected to the 1.8V external power supply when embedded regulators are not used,	
53	F8	34	F6	VSS18	S									Ground Voltage for the main voltage regulator	
54	F9	35	F7	VSSBKP	S									Stabilization for low power voltage regulator.	
55	G9	36	E7	V18BKP	S									Ground Voltage for the low power voltage regulator. Requires external capacitors of at least 1µF between V18BKP and VSSBKP. See *Figure 4.2*. To be connected to the 1.8V external power supply when embedded regulators are not used,	
56	H10	37	F8	XRTC1									X	32 kHz oscillator for Realtime Clock	
57	G10	38	E8	XRTC2									X		
58	E7	39	E5	NRSTOUT	O								X	Reset output	
59	E9	40	E6	NRSTIN	I	T_T							X	Reset input	
60	D6			P1.15 / WKP_STDBY	I	T_T	X		EIT15				X	**Port 1.15**	Wake-up from STANDBY input pin
61	B8			P2.13	I/O	T_T	X	X		O2	X	X		**Port 2.13**	
62	D9			P2.12	I/O	T_T	X	X		O2	X	X		**Port 2.12**	
63	F10	41 (7)	D8 (7)	P0.15 / CAN_TX	I/O	T_T	X	X		O2	X	X		**Port 0.15**	CAN: Transmit data output
64	E10	42 (7)	C8 (7)	P0.14 / CAN_RX	I/O	T_T	X	X	EIT5	O2	X	X		**Port 0.14**	CAN: Receive data input
65	D10	41 (7)	D8 (7)	USB_DN	I/O									USB: bidirectional data (data -)	
66	C10	42 (7)	C8 (7)	USB_DP	I/O									USB: bidirectional data (data +)	
67	B9	43	B8	P1.03 / TIM2_TI2	I/O	T_T	X	X		O2	X	X		**Port 1.03**	TIM2: Input Capture / trigger / external clock 2 (remappable to P0.07)(8)

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
91	A4	59	A3	P1.04 / PWM3N / ADC_IN9	I/O	T_T	**X**	X		O4	X	X		**Port 1.04**	PWM: PWM3 complementary output(4)	ADC: analog input 9
92	A3			P1.14 / ADC_IN15	I/O	T_T	**X**	X		O8	X	X		**Port 1.14**	ADC: analog input 15	
93	A2			P1.13 / ADC_IN14	I/O	T_T	**X**	X	EIT13	O8	X	X		**Port 1.13**	ADC: analog input 14	
94	D5			P1.01 / TIM0_TI2	I/O	T_T	**X**	X		O2	X	X		**Port 1.01**	TIM0: Input Capture / trigger / external clock 2 (remappable to P0.05)(8)	
95	E6			P1.00 / TIM0_OC2	I/O	T_T	**X**	X		O2	X	X		**Port 1.00**	TIM0: Output compare 2 (remappable to P0.04)(8)	
96	C4	60	C4	V18	S									Stabilization for main voltage regulator. Requires external capacitors 33nF between V18 and VSS18. See *Figure 4.2*. To be connected to the 1.8V external power supply when embedded regulators are not used.		
97	D4	61	C5	VSS18	S									Ground Voltage for the main voltage regulator.		
98	D3	62	A2	VSS_IO	S									Ground Voltage for digital I/Os		
99	C3	63	B2	VDD_IO	S									Supply Voltage for digital I/Os		
100	A1	64	A1	P0.03 / TIM2_TI1 / ADC_IN1	I/O	T_T	**X**	X		O2	X	X		**Port 0.03**	TIM2: Input Capture / trigger / external clock 1	ADC: analog input 1

1. For STR755FVx part numbers, the USB pins must be left unconnected.
2. The non available pins on LQPFP64 and LFBGA64 packages are internally tied to low level.
3. None of the I/Os are True Open Drain: when configured as Open Drain, there is always a protection diode between the I/O pin and VDD_IO.
4. In the 100-pin package, this Alternate Function is duplicated on two ports. You can configure one port to use this AF, the other port is then free for general purpose I/O (GPIO), external interrupt/wake-up lines, or analog input (ADC_IN) where these functions are listed in the table.
5. It is mandatory that the NJTRST pin is reset to ground during the power-up phase. It is recommended to connect this pin to NRSTOUT pin (if available) or NRSTIN.
6. After reset, these pins are enabled as JTAG alternate function see (*Port reset state on page 16*). To use these ports as general purpose I/O (GPIO), the DBGOFF control bit in the GPIO_REMAP0R register must be set by software (in this case, debugging these I/Os via JTAG is not possible).
7. There are two different TQFP and BGA 64-pin packages: in the first one, pins 41 and 42 are mapped to USB DN/DP while for the second one, they are mapped to P0.15/CAN_TX and P0.14/CAN_RX.
8. For details on remapping these alternate functions, refer to the GPIO_REMAP0R register description.

Power supply scheme 3: Single external 5 V power source

Figure 10. Power supply scheme 3

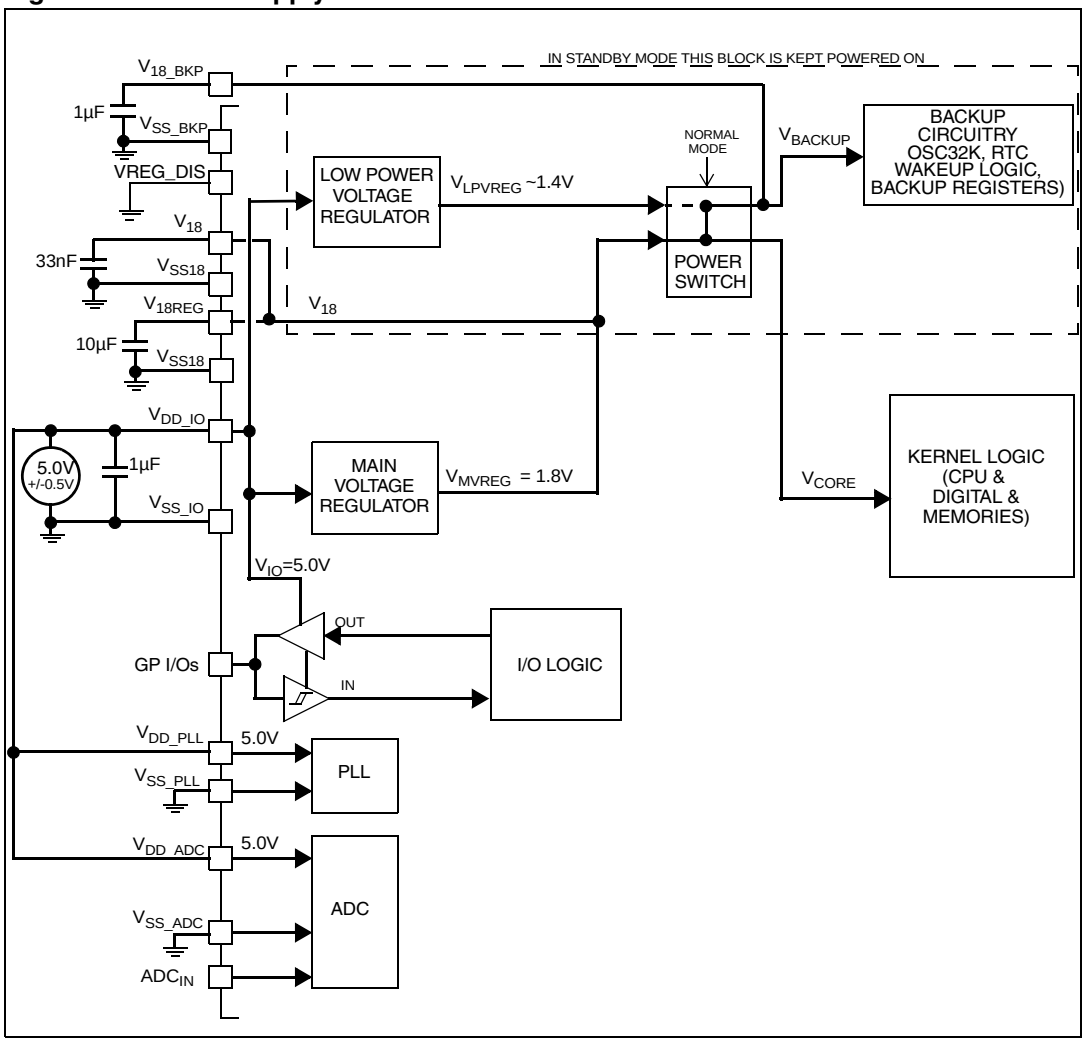


Figure 14. Power consumption measurements in power scheme 3 (regulators enabled)

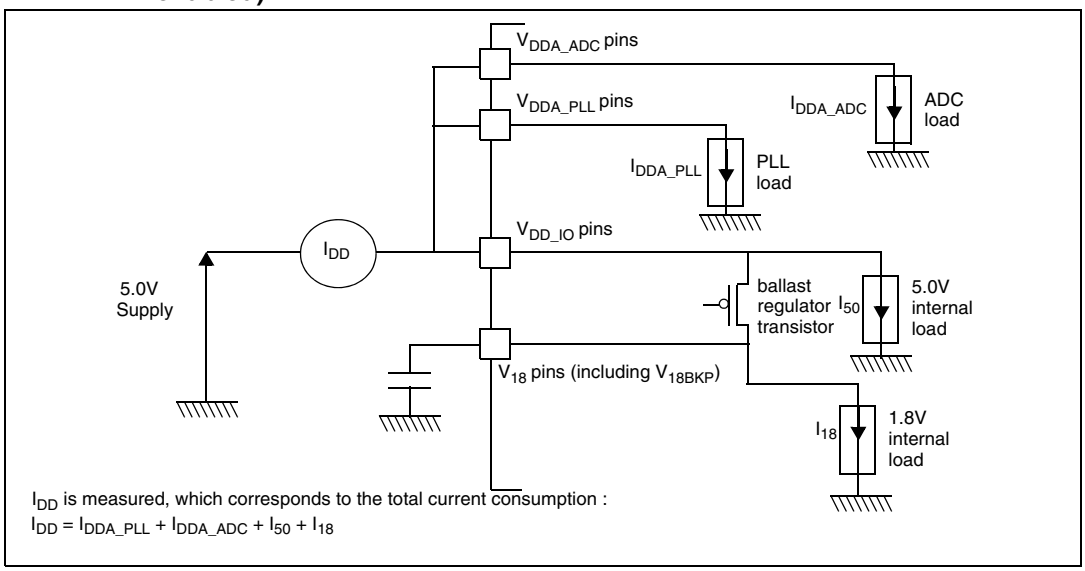
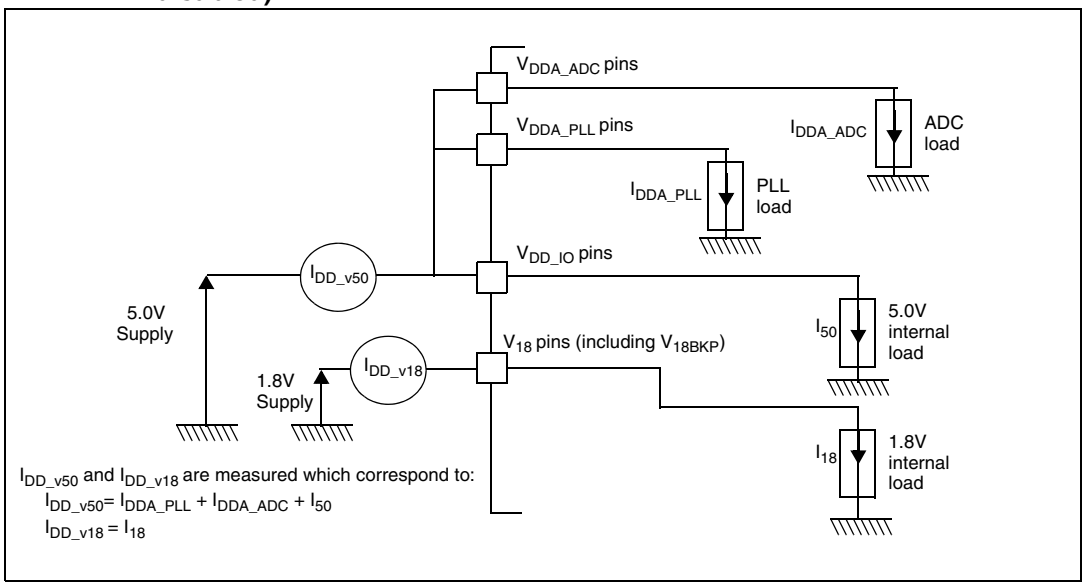


Figure 15. Power consumption measurements in power scheme 4 (regulators disabled)



6.2.2 Current characteristics

Table 8. Current characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD_IO} (1)	Total current into V_{DD_IO} power lines (source) (2)	150	mA
I_{VSS_IO} (1)	Total current out of V_{SS} ground lines (sink) (2)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ (3) & (4)	Injected current on NRSTIN pin	± 5	
	Injected current on XT1 and XT2 pins	± 5	
	Injected current on any other pin (5)	± 5	
$\Sigma I_{INJ(PIN)}$ (3)	Total injected current (sum of all I/O and control pins) (5)	± 25	

1. The user can use GPIOs to source or sink high current (up to 20 mA for O8 type High Sink I/Os). In this case, the user must ensure that these absolute max. values are not exceeded (taking into account the RUN power consumption) and must follow the rules described in *Section 6.3.8: I/O port pin characteristics on page 54*.
2. All 3.3 V or 5.0 V power (V_{DD_IO}, V_{DDA_ADC}, V_{DDA_PLL}) and ground (V_{SS_IO}, V_{SSA_ADC}, V_{DDA_ADC}) pins must always be connected to the external 3.3V or 5.0V supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Data based on T_A=25°C.
4. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.12: 10-bit ADC characteristics on page 72*.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

6.2.3 Thermal characteristics

Table 9. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Subject to general operating conditions for V_{DD_IO}, and T_A unless otherwise specified.

Table 10. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB Clock frequency	Accessing SRAM with 0 wait states	0	64	MHz
		Accessing Flash in burst mode, $T_A \leq 85°$ C	0	60	
		Accessing Flash in burst mode $T_A > 85°$ C		56	
		Accessing Flash with 0 wait states	0	32	
		Write access to Flash registers(1)	0	30	
		Accessing Flash in RWW mode	0	16	
f_{PCLK}	Internal APB Clock frequency		0	32	MHz
V_{DD_IO}	Standard Operating Voltage Power Scheme 1 & 2		3.0	3.6	V
	Standard Operating Voltage Power Scheme 3 & 4		4.5	5.5	
V_{18}	Standard Operating Voltage Power Scheme 2 & 4		1.65	1.95	
P_D	Power dissipation at $T_A = 85°$ C for suffix 6 or $T_A = 105°$ C for suffix 7(2)	LQFP100		434	mW
		LQFP64		444	
		LFBGA100		487	
		LFBGA64		344	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
		Low power dissipation(3)	-40	105	°C
	Ambient temperature for 7 suffix version	Maximum power dissipation	-40	105	°C
		Low power dissipation (3)	-40	125	°C
T_J	Junction temperature range	6 Suffix Version	-40	105	°C
		7 Suffix Version	-40	125	°C

1. Write access to Flash registers is either a program, erase, set protection or un-set protection operation.
2. If T_A is lower, higher PD values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.2: Thermal characteristics on page 79*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.2: Thermal characteristics on page 79*).

Typical power consumption

The following measurement conditions apply to *Table 15*, *Table 16* and *Table 17*.

In RUN mode:

- Program is executed from Flash (except if especially mentioned). The program consists of an infinite loop. When f_{HCLK} > 32 MHz, burst mode is activated.
- A standard 4 MHz crystal source is used.
- In all cases the PLL is used to multiply the frequency.
- All measurements are done in the single supply scheme with internal regulators used (see *Figure 12*)

In WFI Mode:

- In WFI Mode the measurement conditions are similar to RUN mode (OSC4M and PLL enabled). In addition, the Flash can be disabled depending on burst mode activation:
  - For AHB frequencies greater than 32 MHz, burst mode is activated and the Flash is kept enabled by setting the WFI_FLASH_EN bit (this bit cannot be reset when burst mode is activated).
  - For AHB frequencies less than or equal to 32 MHz, burst mode is deactivated, WFI_FLASH_EN is reset and the LP_PARAM14 bit is set (Flash is disabled in WFI mode).

In SLOW mode:

- The same program as in RUN mode is executed from Flash. The CPU is clocked by the FREEOSC, OSC4M, LPOSC or OSC32K. Only EXTIT peripheral is enabled in the MRCC_PCLKEN register.

In SLOW-WFI mode:

- In SLOW-WFI, the measurement conditions are similar to SLOW mode (CPU clocked by a low frequency clock). In addition, the LP_PARAM14 bit is set (FLASH is OFF). The WFI routine itself is executed from SRAM (it is not allowed to execute a WFI from the internal FLASH)

In STOP mode:

- Several measurements are given: in the single supply scheme with internal regulators used (see *Figure 12*): and in the dual supply scheme (see *Figure 13*).

In STANDBY mode:

- Three measurements are given:
  - The RTC is disabled, only the consumption of the LPVREG and RSM remain (almost no leakage currents)
  - The RTC is running, clocked by a standard 32.768 kHz crystal.
  - The RTC is running, clocked by the internal Low Power RC oscillator (LPOSC)
- STANDBY mode is only supported in the single supply scheme (see *Figure 12*)

Subject to general operating conditions for V_{DD_IO}, and T_A

Table 15. Single supply typical power consumption in Run, WFI, Slow and Slow-WFI modes

Symbol	Para meter	Conditions	3.3V typ(1)	5V typ(2)	Unit
I_{DD} (3)	Supply current in RUN mode(4)	Clocked by OSC4M with PLL multiplication, all peripherals enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz f_{HCLK}=56 MHz, f_{PCLK}=28 MHz f_{HCLK}=48 MHz, f_{PCLK}=24 MHz f_{HCLK}=32 MHz, f_{PCLK}=32 MHz f_{HCLK}=16 MHz, f_{PCLK}=16 MHz f_{HCLK}=8 MHz, f_{PCLK}=8 MHz	 80 75 65 59 34 20	 82 77 67 61 37 22	mA
		Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz f_{HCLK}=56 MHz, f_{PCLK}=28 MHz f_{HCLK}=48 MHz, f_{PCLK}=24 MHz f_{HCLK}=32 MHz, f_{PCLK}=32 MHz f_{HCLK}=16 MHz, f_{PCLK}=16 MHz f_{HCLK}=8 MHz, f_{PCLK}=8 MHz	 65 60 54 42 22 16	 67 62 55 44 24 18	mA
	Supply current in WFI mode(4)	Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz(5) f_{HCLK}=56 MHz, f_{PCLK}=28 MHz(5) f_{HCLK}=48 MHz, f_{PCLK}=24 MHz(5) f_{HCLK}=32 MHz, f_{PCLK}=32 MHz(6) f_{HCLK}=16 MHz, f_{PCLK}= 16 MHz (6) f_{HCLK}= 8 MHz, f_{PCLK}= 8 MHz(6)	 62 59 53 22 13 10	 63 60 54 23 15 11	mA
	Supply current in SLOW mode(4)	Clocked by FREEOSC: f_{HCLK}=f_{PCLK}=~5 MHz, Clocked by OSC4M: f_{HCLK}=f_{PCLK}=4 MHz Clocked by LPOSC: f_{HCLK}=f_{PCLK}=~300 kHz Clocked by OSC32K: f_{HCLK}=f_{PCLK}=32.768 kHz	9 8 3.65 3.5	10 9 3.9 4.2	mA
	Supply current in SLOW-WFI mode(4)(7)	Clocked by FREEOSC: f_{HCLK}=f_{PCLK}=~5 MHz Clocked by OSC4M: f_{HCLK}=f_{PCLK}=4 MHz Clocked by LPOSC: f_{HCLK}=f_{PCLK}=~300 kHz Clocked by OSC32K: f_{HCLK}=f_{PCLK}=32.768 kHz	3.5 3.1 1.15 0.98	4.0 3.75 1.65 1.5	mA

1. Typical data based on T_A=25° C and V_{DD_IO}=3.3V.
2. Typical data based on T_A=25° C and V_{DD_IO}=5.0V.
3. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4 on page 36*.
4. Single supply scheme see *Figure 14*.
5. Parameter setting BURST=1, WFI_FLASHEN=1
6. Parameter setting BURST=0, WFI_FLASHEN=0
7. Parameter setting WFI_FLASHEN=0, OSC4MOFF=1

OSC32K crystal / ceramic resonator oscillator

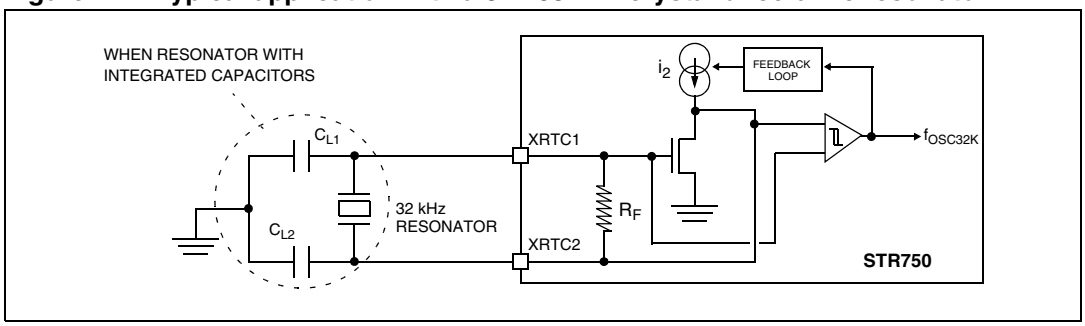
The STR7 RTC clock can be supplied with a 32.768 kHz Crystal/Ceramic resonator oscillator. All the information given in this paragraph are based on product characterisation with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

Table 23. OSC32K crystal / ceramic resonator oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC32K}	Oscillator Frequency			32.768		kHz
R_F	Feedback resistor	V_{DD_IO}=3.3 V or 5.0 V	270	310	370	kΩ
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal or ceramic resonator (R_S)(1)	R_S=40KΩ		12.5	15	pF
i_2	XT2 driving current	V_{DD_IO}=3.3 V or 5.0 V V_{IN}=V_{SS}	1		5	µA
$t_{SU(OSC32K)}$(2)	Startup time	V_{DD_IO} is stabilized		2.5		s

1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value. Refer to crystal/ceramic resonator manufacturer for more details
2. $t_{SU(OSC32K)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 32 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal/ceramic resonator manufacturer

Figure 22. Typical application with a 32.768 kHz crystal or ceramic resonator



PLL characteristics

PLL Jitter Terminology

- Self-referred single period jitter (period jitter)

  Period Jitter is defined as the difference of the maximum period (T_{max}) and minimum period (T_{min}) at the output of the PLL where T_{max} is the maximum time difference between 2 consecutive clock rising edges and T_{min} is the minimum time difference between 2 consecutive clock rising edges.

  See *Figure 23*

- Self-referred long term jitter (N period jitter)

  Self-referred long term Jitter is defined as the difference of the maximum period (T_{max}) and minimum period (T_{min}) at the output of the PLL where T_{max} is the maximum time

6.3.6 Memory characteristics

Flash memory

Subject to general operating conditions for V_{DD_IO} and V_{18}, T_A = -40 to 105 °C unless otherwise specified.

Table 26. Flash memory characteristics

Symbol	Parameter	Test Conditions	Value		Unit
			Typ	Max(1)	
t_{PW}	Word Program		35		µs
t_{PDW}	Double Word Program		60		µs
t_{PB0}	Bank 0 Program (256K)	Single Word programming of a checker-board pattern	2	4.9(2)	s
t_{PB1}	Bank 1 Program (16K)	Single Word programming of a checker-board pattern	125	224(2)	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed (all 1) Preprogrammed (all 0)	1.54 1.176	2.94(2) 2.38(2)	s
t_{ES}	Sector Erase (8K)	Not preprogrammed (all 1) Preprogrammed (all 0)	392 343	560(2) 532(2)	ms
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed (all 1) Preprogrammed (all 0)	8.0 6.6	13.7 11.2	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed (all 1) Preprogrammed (all 0)	0.9 0.8	1.5 1.3	s
t_{RPD}	Recovery when disabled			20	µs
t_{PSL}	Program Suspend Latency			10	µs
t_{ESL}	Erase Suspend Latency			300	µs

1. Data based on characterisation not tested in production
2. 10K program/erase cycles.

Table 27. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END_B0}	Endurance (Bank 0 sectors)		10			kcycles
N_{END_B1}	Endurance (Bank 1 sectors)		100			kcycles
Y_{RET}	Data Retention	T_A=85° C	20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

1. Data based on characterisation not tested in production.

Electro magnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 29. EMI characteristics

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f_{OSC4M}/f_{HCLK}]		Unit
				4/32MHz	4/60MHz	
S_{EMI}	Peak level	Flash devices: V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, LQFP64 package conforming to SAE J 1752/3	0.1 MHz to 30 MHz	22	26	dBµV
			30 MHz to 130 MHz	31	26	
			130 MHz to 1 GHz	19	23	
			SAE EMI Level	>4	>4	-

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electro-Static discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard.

Table 30. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25° C	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)		200	
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charge Device Model)		750	

1. Data based on product characterisation, not tested in production.

6.3.9 TB and TIM timer characteristics

Subject to general operating conditions for V_{DD_IO}, f_{CK_SYS}, and T_A unless otherwise specified.

Refer to *Section 6.3.8: I/O port pin characteristics on page 54* for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

Table 36. TB and TIM timers

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time	TIM0,1,2		2			t_{CK_TIM}
$t_{res(TIM)}$	Timer resolution time(1)	TB	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	16.6(1)			ns
		TIM0,1,2	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60MHz	16.6(1)			ns
f_{EXT}	Timer external clock frequency on TI1 or TI2	TIM0,1,2	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	0		$f_{CK\_TIM}/4$	MHz
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0		15	MHz
Res_{TIM}	Timer resolution					16	bit
$t_{COUNTER}$	16-bit Counter clock period when internal clock is selected (16-bit Prescaler)	TB		1		65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0.0166		1092	µs
		TIM0,1,2		1		65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0.0166		1092	µs
t_{MAX_COUNT}	Maximum Possible Count	TB				65536x65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s
		TIM0,1,2				65536x65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s

1. Take into account the frequency limitation due to the I/O speed capability when outputting the PWM to I/O pin, described in *: Output speed on page 57*.

SSP synchronous serial peripheral in slave mode (SPI or TI mode)

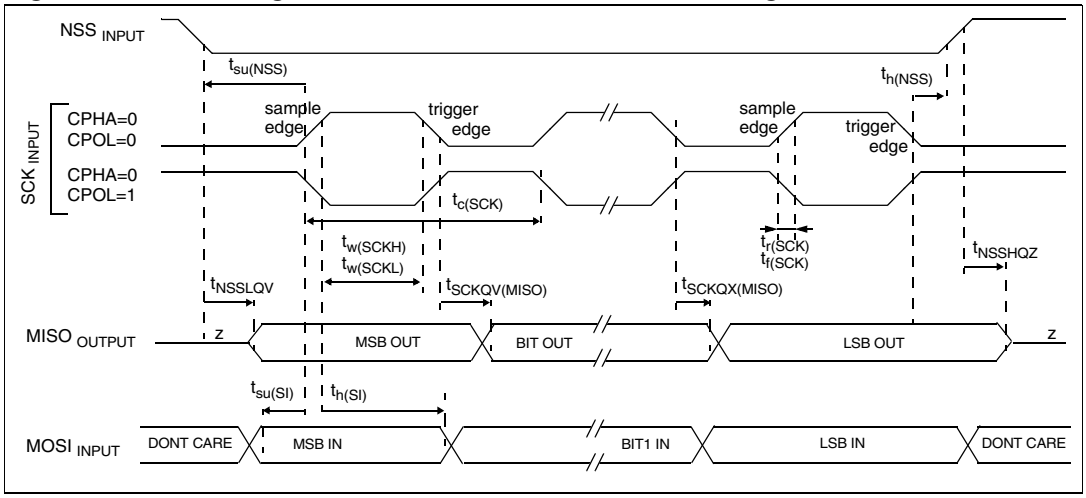
Subject to general operating conditions with $C_L \approx 45$ pF

Table 39. SSP slave mode characteristics(1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK}	SPI clock frequency		SSP0		2.66 MHz (f_{PLCK}/12)	MHz
			SSP1			
$t_{su(NSS)}$	NSS input setup time w.r.t SCK first edge		SSP0	0		ns
			SSP1	0		
$t_{h(NSS)}$	NSS input hold time w.r.t SCK last edge		SSP0	t_{PCLK}+15ns		
			SSP1	t_{PCLK}+15ns		
t_{NSSLQV}	NSS low to Data Output MISO valid time		SSP0	$2t_{PCLK}$	$3t_{PCLK}$+30 ns	
			SSP1	$2t_{PCLK}$	$3t_{PCLK}$+30 ns	
t_{NSSLQZ}	NSS low to Data Output MISO invalid time		SSP0	$2t_{PCLK}$	$3t_{PCLK}$+15 ns	
			SSP1	$2t_{PCLK}$	$3t_{PCLK}$+15 ns	
t_{SCKQV}	SCK trigger edge to data output MISO valid time		SSP0		15	
			SSP1		30	
t_{SCKQX}	SCK trigger edge to data output MISO invalid time		SSP0	$2t_{PCLK}$		
			SSP1	$2t_{PCLK}$		
$t_{su(MOSI)}$	MOSI setup time w.r.t SCK sampling edge		SSP0	0		
			SSP1	0		
$t_{h(MOSI)}$	MOSI hold time w.r.t SCK sampling edge		SSP0	$3t_{PCLK}$+15 ns		
			SSP1	$3t_{PCLK}$+15 ns		

1. Data based on characterisation results, not tested in production.

Figure 33. SPI configuration, slave mode with CPHA=0, single transfer



SMI - serial memory interface

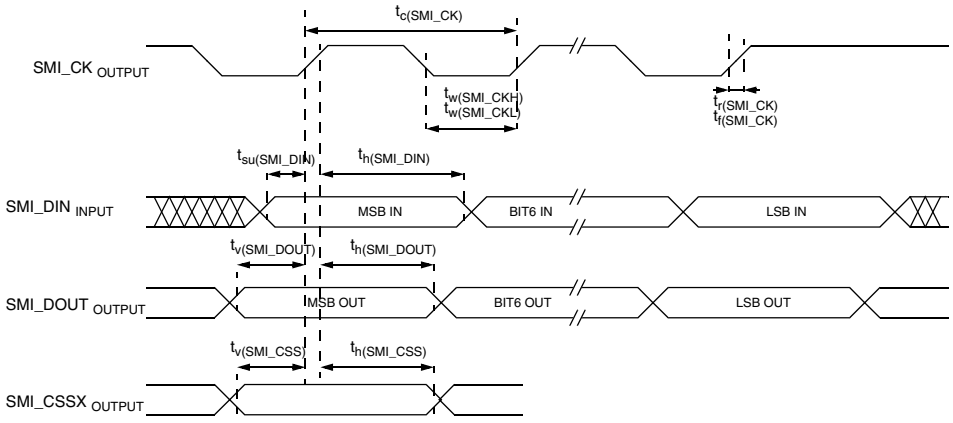
Subject to general operating conditions with $C_L \approx 30$ pF.

Table 40. SMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
f_{SMI_CK}	SMI clock frequency		32(2)(3)	MHz
			48(4)	
$t_{r(SMI\_CK)}$	SMI clock rise time		10	ns
$t_{f(SMI\_CK)}$	SMI clock fall time		8	
$t_{v(SMI\_DOUT)}$	Data output valid time		10	
$t_{h(SMI\_DOUT)}$	Data output hold time		0	
$t_{v(SMI\_CSSx)}$	CSS output valid time		10	
$t_{h(SMI\_CSSx)}$	CSS output hold time		0	
$t_{su(SMI\_DIN)}$	Data input setup time	0		
$t_{h(SMI\_DIN)}$	Data input hold time	5		

1. Data based on characterisation results, not tested in production.
2. Max. frequency = $f_{PCLK}/2 = 64/2 = 32$ MHz.
3. Valid for all temperature ranges: -40 to 105 °C, with 30 pF load capacitance.
4. Valid up to 60 °C, with 10 pF load capacitance.

Figure 39. SMI timing diagram



I²C - Inter IC control interface

Subject to general operating conditions for V_{DD_IO}, f_{PCLK}, and T_A unless otherwise specified.

The I²C interface meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Restriction: The I/O pins which SDA and SCL are mapped to are not “True” Open-Drain: when configured as open-drain, the PMOS connected between the I/O pin and V_{DD_IO} is disabled, but it is still present. Also, there is a protection diode between the I/O pin and V_{DD_IO}. Consequently, when using this I²C in a multi-master network, it is

6.3.12 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA_ADC}, f_{PCLK}, and T_A unless otherwise specified.

Table 45. 10-bit ADC characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
f_{ADC}	ADC clock frequency		0.4		8	MHz
V_{AIN}	Conversion voltage range(2)		V_{SSA_ADC}		V_{DDA_ADC}	V
R_{AIN}	External input impedance(3)(4)				10	kΩ
C_{AIN}	External capacitor on analog input(3)(4)				6.8	pF
I_{lkg}	Induced input leakage current	+400 µA injected on any pin			1	µA
		-400 µA injected on any pin except specific adjacent pins in *Table 46*			1	µA
		-400µA injected on specific adjacent pins in *Table 46*		40		µA
C_{ADC}	Internal sample and hold capacitor			3.5		pF
t_{CAL}	Calibration Time	f_{CK_ADC}=8 MHz	725.25			µs
			5802			$1/f_{ADC}$
t_{CONV}	Total Conversion time (including sampling time)	f_{CK_ADC}=8 MHz	3.75			µs
			30 (11 for sampling + 19 for Successive Approximation)			$1/f_{ADC}$
I_{ADC}		Sunk on V_{DDA_ADC}		3.7		mA

1. Unless otherwise specified, typical data are based on T_A=25°C. They are given only as design guidelines and are not tested.
2. Calibration is needed once after each power-up.
3. $C_{PARASITIC}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
4. Depending on the input signal variation (f_{AIN}), C_{AIN} can be increased for stabilization time and reduced to allow the use of a larger serial resistor (R_{AIN}). It is valid for all f_{ADC} frequencies ≤ 8 MHz.

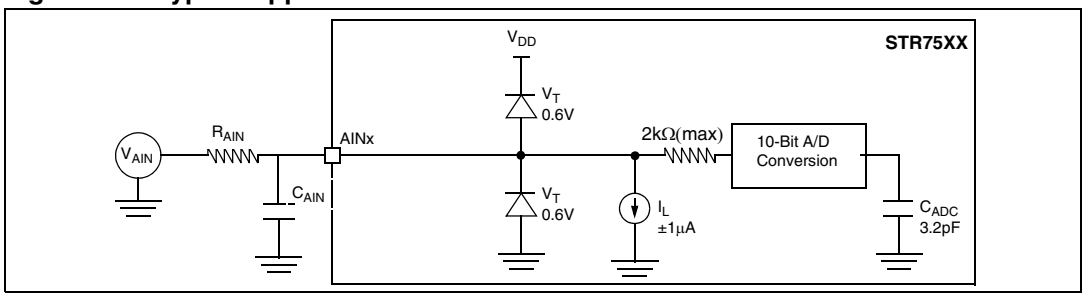
ADC accuracy vs. negative injection current

Injecting negative current on specific pins listed in *Table 46* (generally adjacent to the analog input pin being converted) should be avoided as this significantly reduces the accuracy of the conversion being performed. It is recommended to add a Schottky diode (pin to ground) to pins which may potentially inject negative current.

Table 46. List of adjacent pins

Analog input	Related adjacent pins
a	None
AIN1/P0.03	None
AIN2/P0.12	P0.11
AIN3/P0.17	P0.18 and P0.16
AIN4/P0.19	P0.24
AIN5/P0.22	None
AIN6/P0.23	P2.04
AIN7/P0.27	P1.11 and P0.26
AIN8/P0.29	P0.30 and P0.28
AIN9/P1.04	None
AIN10/P1.06	P1.05
AIN11/P1.08	P1.04 and P1.13
AIN12/P1.11	P2.17 and P0.27
AIN13/P1.12	None
AIN14/P1.13	P1.14 and P1.01
AIN15/P1.14	None

Figure 42. Typical application with ADC



Analog power supply and reference pins

The V_{DDA_ADC} and V_{SSA_ADC} pins are the analog power supply of the A/D converter cell.

Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see *: General PCB design guidelines on page 74*).

General PCB design guidelines

To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 µF and optionally, if needed 10 pF capacitors as close as possible to the STR7 power supply pins and a 1 to 10 µF capacitor close to the power source (see *Figure 43*).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{DDA_ADC} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs near the A/D input being converted.

Software filtering of spurious conversion results

For EMC performance reasons, it is recommended to filter A/D conversion outliers using software filtering techniques.

Figure 43. Power supply filtering

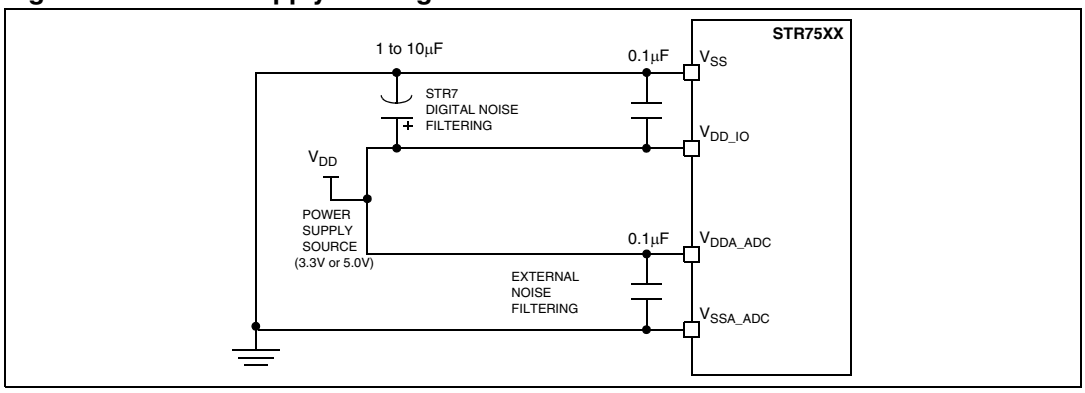


Table 49. Order codes (continued)

Order code	Flash Prog. Memory (Bank 0) Kbytes	Package	CAN Periph	USB Periph	Nominal Temp. Range (T_A)
STR755FV0T6	64	LQFP100 14x14	-	-	-40 to +85°C
STR755FV1T6	128				
STR755FV2T6	256				
STR755FV0H6	64	LFBGA100 10x10			
STR755FV1H6	128				
STR755FV2H6	256				