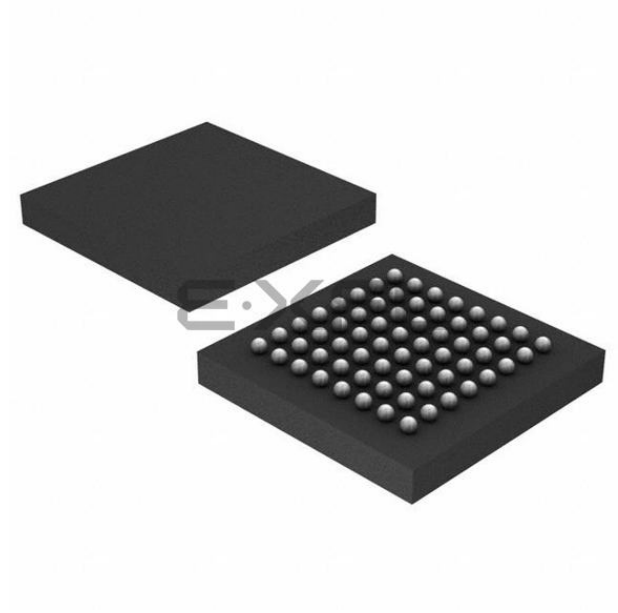

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, SPI, SSI, SSP, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str755fr0h6

1 Description

The STR750 family of 32-bit microcontrollers combines the industry-standard ARM7TDMI® 32-bit RISC core, featuring high performance, very low power, and very dense code, with a comprehensive set of peripherals and ST's latest 0.18µ embedded Flash technology. The STR750 family comprises a range of devices integrating a common set of peripherals as well as USB, CAN and some key innovations like clock failure detection and an advanced motor control timer. It supports both 3.3V and 5V, and it is also available in an extended temperature range (-40 to +105°C). This makes it a genuine general purpose microcontroller family, suitable for a wide range of applications:

- Appliances, brushless motor drives
- USB peripherals, UPS, alarm systems
- Programmable logic controllers, circuit breakers, inverters
- Medical and portable equipment

2 Device overview

Table 2. Device overview

Features	STR755FR0 STR755FR1 STR755FR2	STR751FR0/ STR751FR1/ STR751FR2	STR752FR0/ STR752FR1/ STR752FR2	STR755FV0 STR755FV1/ STR755FV2	STR750FV0/ STR750FV1/ STR750FV2
Flash - Bank 0 (bytes)	64K/128K/256K				
Flash - Bank 1 (bytes)	16K RWW				
RAM (bytes)	16K				
Operating Temperature.	Ambient temp.:-40 to +85°C / -40 to +105°C (see *Table 49*) Junction temp. -40 to + 125 °C (see *Table 10*)				
Common Peripherals	3 UARTs, 2 SSPs, 1 I2C, 3 timers 1 PWM timer, 38 I/Os 13 Wake-up lines, 11 A/D Channels			3 UARTs, 2 SSPs, 1 I^2C, 3 timers 1 PWM timer, 72 I/Os 15 Wake-up lines, 16 A/D Channels	
USB/CAN peripherals	None	USB	CAN	None	USB+CAN
Operating Voltage	3.3V or 5V	3.3V	3.3V or 5V		
Packages (**x**)	**T**=LQFP64 10x10, **H**=LFBGA64			**T**=LQFP100 14x14, **H**=LFBGA100	

3 Introduction

This Datasheet contains the description of the STR750F family features, pinout, Electrical Characteristics, Mechanical Data and Ordering information.

For complete information on the Microcontroller memory, registers and peripherals. Please refer to the STR750F Reference Manual.

For information on the ARM7TDMI-S core please refer to the ARM7TDMI-S Technical Reference Manual available from Arm Ltd.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash Programming Reference Manual

For information on third-party development tools, please refer to the http://www.st.com/mcu website.

3.1 Functional description

The STR750F family includes devices in 2 package sizes: 64-pin and 100-pin. Both types have the following common features:

ARM7TDMI-S™ core with embedded Flash & RAM

STR750F family has an embedded ARM core and is therefore compatible with all ARM tools and software. It combines the high performance ARM7TDMI-S™ CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage FLASH memory and high-speed RAM.

Figure 1 shows the general block diagram of the device family.

Embedded Flash memory

Up to 256 KBytes of embedded Flash is available in Bank 0 for storing programs and data. An additional Bank 1 provides 16 Kbytes of RWW (Read While Write) memory allowing it to be erased/programmed on-the-fly. This partitioning feature is ideal for storing application parameters.

- When configured in burst mode, access to Flash memory is performed at CPU clock speed with 0 wait states for sequential accesses and 1 wait state for random access (maximum 60 MHz).
- When not configured in burst mode, access to Flash memory is performed at CPU clock speed with 0 wait states (maximum 32 MHz)

Embedded SRAM

16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

Enhanced interrupt controller (EIC)

In addition to the standard ARM interrupt controller, the STR750F embeds a nested interrupt controller able to handle up to 32 vectors and 16 priority levels. This additional hardware block provides flexible interrupt management features with minimal interrupt latency.

4.1 Pin description table

Legend / abbreviations for *Table 6*:

Type:	I = input, O = output, S = supply,
Input levels:	All Inputs are LVTTL at V_{DD_IO} = 3.3V+/-0.3V or TTL at V_{DD_IO} = 5V± 0.5V. In both cases, T_T means V_{ILmax} =0.8V V_{IHmin}=2.0V
Inputs:	All inputs can be configured as floating or with internal weak pull-up or pull down (pu/pd)
Outputs:	All Outputs can be configured as Open Drain (OD) or Push-Pull (PP) (see also note 6 below *Table 6*). There are 3 different types of Output with different drives and speed characteristics: – O8: f_{max} = 40 MHz on C_L=50pF and 8 mA static drive capability for V_{OL}=0.4V and up to 20 mA for V_{OL}=1.3V (see*Output driving current on page 55*) – O4: f_{max} = 20 MHz on C_L=50pF and 4 mA static drive capability for V_{OL}=0.4V (see*Output driving current on page 55*) – O2: f_{max} = 10 MHz on C_L=50pF and 2 mA static drive capability of for V_{OL}=0.4V (see*Output driving current on page 55*)
External interrupts/wake-up lines:	EITx

Table 6. STR750F pin description (continued)

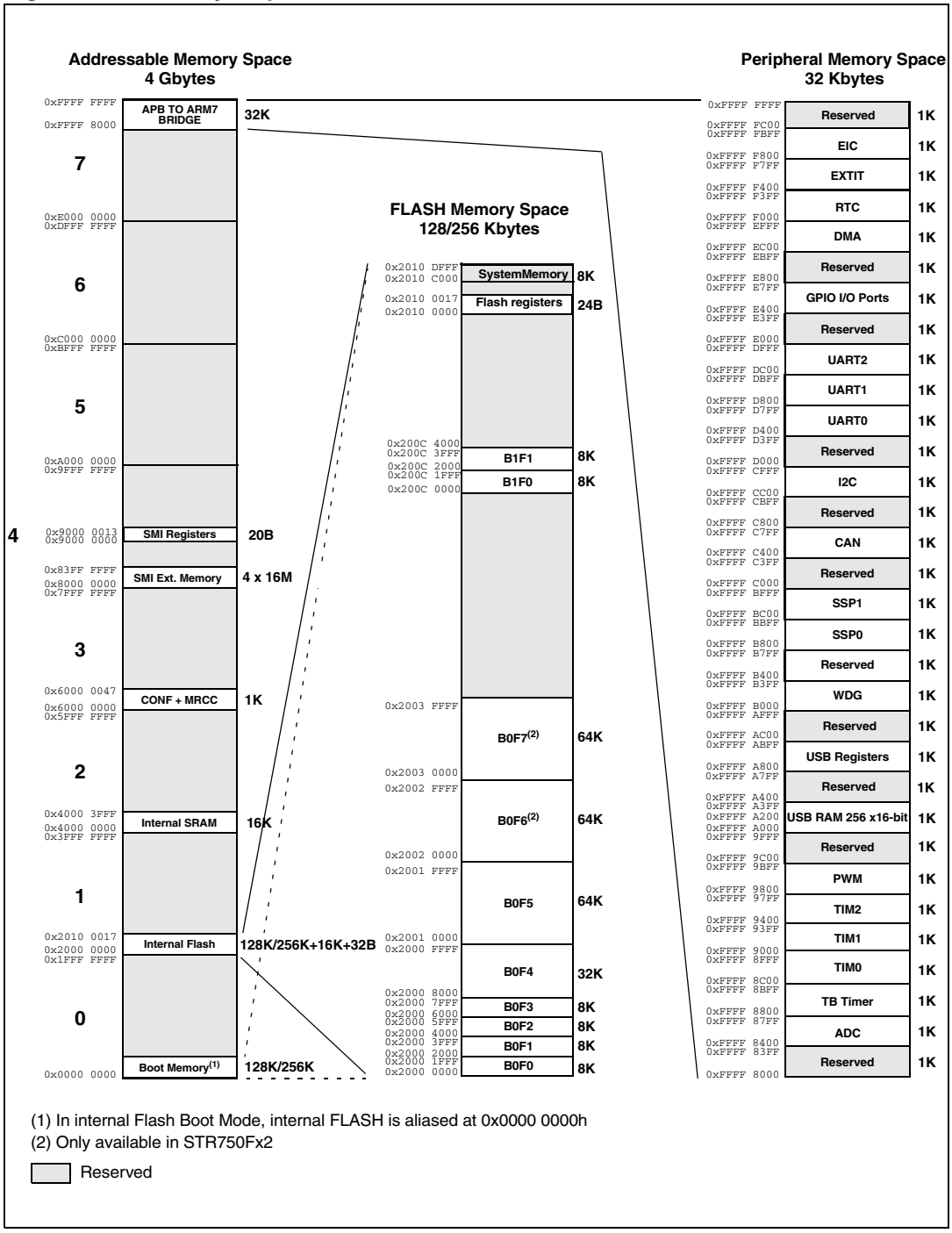
Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
7	D1	5	D1	P0.29 / TIM1_TI1 / ADC_IN8	I/O	T_T	**X**	X		O2	X	X		**Port 0.29**	TIM1: Input Capture 1	ADC: Analog input 8
8	E1	6	D2	P0.28 / TIM1_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 0.28**	TIM1: Output Compare 1	
9	E5	7	D3	TEST	I									Reserved, must be tied to ground		
10	E4	8	D4	VSS_IO	S									Ground Voltage for digital I/Os		
11	E2			P0.23 / UART1_RTS / ADC_IN6	I/O	T_T	**X**	X		O2	X	X		**Port 0.23**	UART1: Ready To Send output(4)	ADC analog input 6
12	F5			P2.04 / TIM2_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 2.04**	TIM2: Output Compare 1(4)	
13	F1			P2.03 / UART1_RTS	I/O	T_T	**X**	X		O2	X	X		**Port 2.03**	UART1: Ready To Send output(4)	
14	F4			P2.02	I/O	T_T	**X**	X		O2	X	X		**Port 2.02**		
15	E3			P0.22 / UART1_CTS / ADC_IN5	I/O	T_T	**X**	X		O2	X	X		**Port 0.22**	UART1: Clear To Send input	ADC: Analog input 5
16	F2	9	E4	P0.21 / UART1_TX	I/O	T_T	**X**	X		O2	X	X		**Port 0.21**	UART1: Transmit data output (remappable to P0.15)(4)	
17	F3	10	E3	P0.20 / UART1_RX	I/O	T_T	**X**	X		O2	X	X		**Port 0.20**	UART1: Receive data input (remappable to P0.14)(4)	
18	G3	11	E2	P1.19 / JTMS	I/O	T_T	X	X		O2	X	X		**JTAG mode selection input(6)**	Port 1.19	
19	G2	12	E1	P1.18 / JTCK	I/O	T_T	X	X		O2	X	X		**JTAG clock input(6)**	Port 1.18	
20	H3	13	F4	P1.17 / JTDO	I/O	T_T	X	X		O8	X	X		**JTAG data output(6)**	Port 1.17	
21	H2	14	F3	P1.16 / JTDI	I/O	T_T	X	X		O2	X	X		**JTAG data input(6)**	Port 1.16	
22	G1	15	F2	NJTRST	I	T_T								JTAG reset input(5)		
23	G4			P2.01	I/O	T_T	**X**	X		O2	X	X		**Port 2.01**		
24	G5			P2.00	I/O	T_T	**X**	X		O2	X	X		**Port 2.00**		
25	H1	16	F1	P0.13 / RTCK / UART0_RTS UART2_TX	I/O	T_T	X	X		O8	X	X		**JTAG return clock output(6)**	Port 0.13 / UART0: Ready To Send output(4)	UART2: Transmit Data output (when remapped)(8)

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
68	A10			P1.02 / TIM2_OC2	I/O	T_T	X	X		O2	X	X		**Port 1.02**	TIM2: Output compare 2 (remappable to P0.06)(8)	
69	D7	44	C6	VDD_IO	S									Supply Voltage for digital I/Os		
70	D8	45	D6	VDDA_ADC	S									Supply Voltage for A/D converter		
71	C9			P2.11	I/O	T_T	X	X		O2	X	X		**Port 2.11**		
72	B10			P2.10	I/O	T_T	X	X		O2	X	X		**Port 2.10**		
73	C8	46	D7	VSSA_ADC	S									Ground Voltage for A/D converter		
74	C7	47	C7	VSS_IO	S									Ground Voltage for digital I/Os		
75	E8	48	D5	VREG_DIS	I	T_T								Voltage Regulator Disable input		
76	A9	49	A8	P0.07 / SMI_DOUT / SSP0_MOSI	I/O	T_T	X	X	EIT2	O4	X	X		**Port 0.07**	Serial Memory Interface: data output	SSP0: Master out Slave in data
77	A8	50	A7	P0.06 / SMI_DIN / SSP0_MISO	I/O	T_T	X	X		O4	X	X		**Port 0.06**	Serial Memory Interface: data input	SSP0: Master in Slave out data
78	A7	51	A6	P0.05 / SSP0_SCLK / SMI_CK	I/O	T_T	X	X	EIT1	O4	X	X		**Port 0.05**	SSP0: Serial clock	Serial Memory Interface: Serial clock output
79	B7	52	B6	P0.04 / SMI_CS0 / SSP0_NSS	I/O	T_T	X	X		O4	X	X		**Port 0.04**	Serial Memory Interface: chip select output 0	SSP0: Slave select input
80	C5	53	B7	P1.10 PWM_EMERGENCY	I/O	T_T	X	X	EIT10	O2	X	X		**Port 1.10**	PWM: Emergency input	
81	B6	54	B5	P1.09 / PWM1	I/O	T_T	X	X	EIT9	O4	X	X		**Port 1.09**	PWM: PWM1 output	
82	C6			P2.09 / PWM1N	I/O	T_T	X	X		O2	X	X		**Port 2.09**	PWM: PWM1 complementary output(4)	
83	G7			P2.08 / PWM2	I/O	T_T	X	X		O2	X	X		**Port 2.08**	PWM: PWM2 output(4)	
84	G6			P2.07 / PWM2N	I/O	T_T	X	X		O2	X	X		**Port 2.07**	PWM: PWM2 complementary output(4)	
85	F7			P2.06 / PWM3	I/O	T_T	X	X		O2	X	X		**Port 2.06**	PWM: PWM3 output(4)	
86	F6			P2.05 / PWM3N	I/O	T_T	X	X		O2	X	X		**Port 2.05**	PWM: PWM3 complementary output(4)	
87	A6	55	A5	P1.08 / PWM1N / ADC_IN11	I/O	T_T	X	X		O4	X	X		**Port 1.08**	PWM: PWM1 complementary output(8)	ADC: analog input 11
88	B5	56	B4	P1.07 / PWM2	I/O	T_T	X	X	EIT8	O4	X	X		**Port 1.07**	PWM: PWM2 output(4)	
89	A5	57	A4	P1.06 / PWM2N / ADC_IN10	I/O	T_T	X	X		O4	X	X		**Port 1.06**	PWM: PWM2 complementary output(4)	ADC: analog input 10
90	B4	58	B3	P1.05 / PWM3	I/O	T_T	X	X	EIT7	O4	X	X		**Port 1.05**	PWM: PWM3 output(4)	

5 Memory map

Figure 5. Memory map



(1) In internal Flash Boot Mode, internal FLASH is aliased at 0x0000 0000h
(2) Only available in STR750Fx2

Reserved

6 Electrical parameters

6.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$max (given by the selected temperature range).

Data based on product characterisation, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25° C, V_{DD_IO}=3.3 V (for the 3.0 V≤V_{DD_IO}≤3.6 V voltage range) and V_{18}=1.8 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

Figure 14. Power consumption measurements in power scheme 3 (regulators enabled)

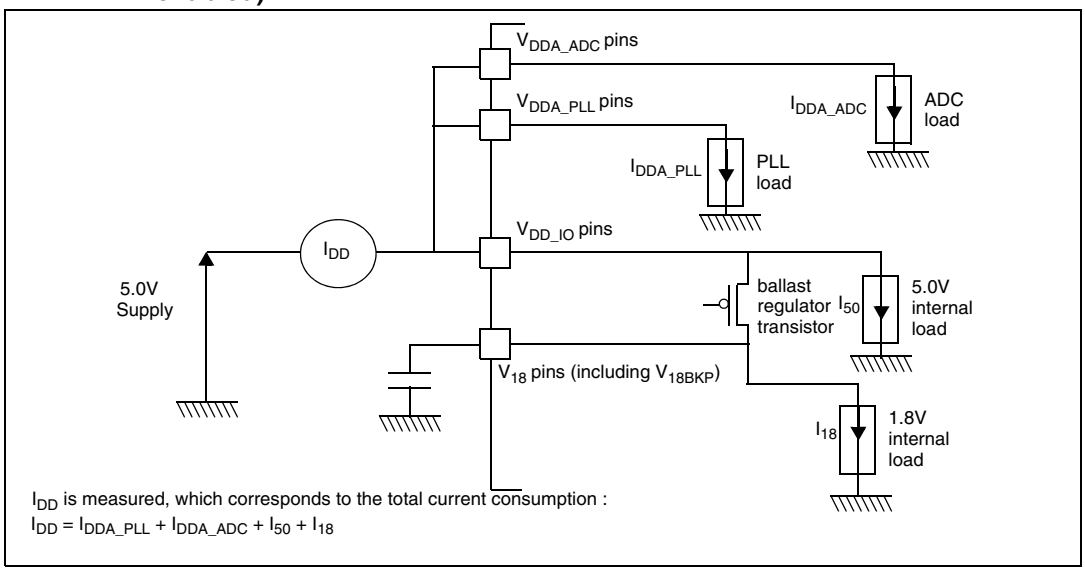


Figure 15. Power consumption measurements in power scheme 4 (regulators disabled)

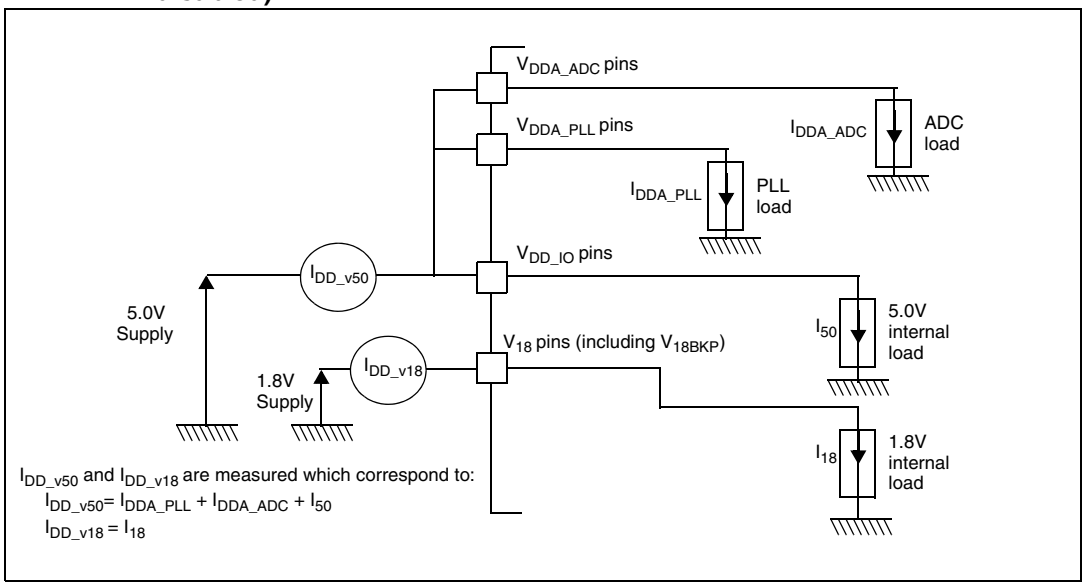


Table 14. Maximum power consumption in STOP and STANDBY modes

Symbol	Parameter	Conditions[1]		Typ[2]	Max[3]			Unit
					T_A 25°C	T_A 85°C	T_A 105°C	
I_{DD}	Supply current in STOP mode	LP_PARAM bits: ALL OFF[4] Single supply scheme see *Figure 12*.	3.3V range	12	16	117	250	µA
		LP_PARAM bits: ALL OFF Dual supply scheme see *Figure 13*.	I_{DD_V18} I_{DD_V33}	5 <1	8 3	60 20	110 26	µA
		LP_PARAM bits: ALL OFF[4] Single supply scheme see *Figure 10*	5V range	15	22	160	310	µA
		LP_PARAM bits: ALL OFF Dual supply scheme see *Figure 11*	I_{DD_V18} I_{DD_V50}	5 3	8 6	60 50	110 65	µA
	Supply current in STANDBY mode	RTC OFF	3.3 V range	10	20	25	28	
			5V range	15	25	30	33	

1. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4*.
2. Typical data are based on T_A=25°C, V_{DD_IO}=3.3V or 5.0V and V_{18}=1.8V unless otherwise specified.
3. Data based on product characterisation, tested in production at V_{DD_IO} max and V_{18} max (1.95V in dual supply mode or regulator output value in single supply mode).
4. In this mode, the whole digital circuitry is powered internally by the LPVREG at approximately 1.4V, which significantly reduces the leakage currents.

difference between N+1 consecutive clock rising edges and T_{min} is the minimum time difference between N+1 consecutive clock rising edges.

N should be kept sufficiently large to have a long term jitter (ex: thousands).

For N=1, this becomes the single period jitter.

See *Figure 23*

- Cycle-to-cycle jitter (N period jitter)

  This corresponds to the time variation between adjacent cycles over a random sample of adjacent clock cycles pairs. Jitter(cycle-to-cycle) = Max(Tcycle n- Tcycle n-1) for n=1 to N.

  See *Figure 24*

Figure 23. Self-referred jitter (single and long term)

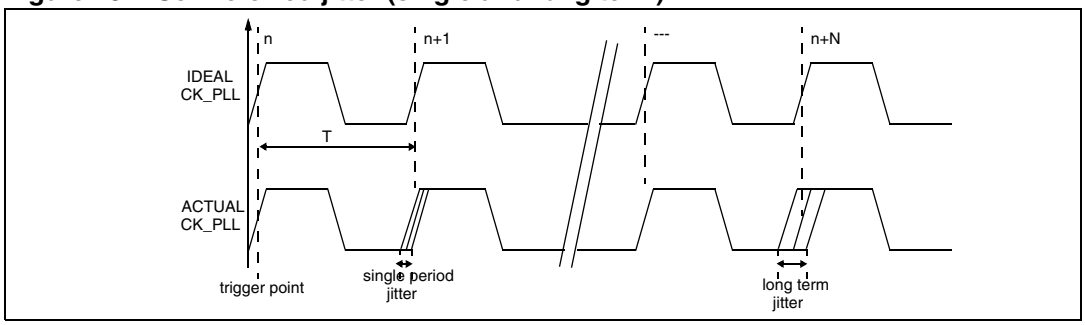
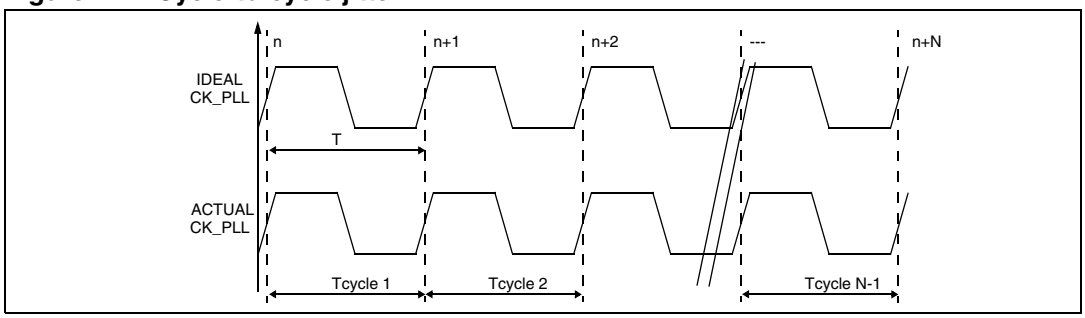


Figure 24. Cycle-to-cycle jitter



6.3.8 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

Table 32. General characteristics

I/O static characteristics							
Symbol	**Parameter**	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
V_{IL}	Input low level voltage	TTL ports				0.8	V
V_{IH}	Input high level voltage			2			
V_{hys}	Schmitt trigger voltage hysteresis(1)				400		mV
$I_{INJ(PIN)}$	Injected Current on any I/O pin					± 4	mA
$\Sigma I_{INJ(PIN}$ (2)	Total injected current (sum of all I/O and control pins)					± 25	
I_{lkg}	Input leakage current on robust pins	See *Section 6.3.12 on page 72*					
	Input leakage current(3)	$V_{SS} \le V_{IN} \le V_{DD\_IO}$				±1	µA
I_S	Static current consumption(4)	Floating input mode			200		
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN}=V_{SS}$	V_{DD_IO}=3.3 V	50	95	200	kΩ
			V_{DD_IO}=5 V	20	58	150	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN}=V_{DD\_IO}$	V_{DD_IO}=3.3 V	25	80	180	kΩ
			V_{DD_IO}=5 V	20	50	120	kΩ
C_{IO}	I/O pin capacitance				5		pF
$t_{w(IT)in}$	External interrupt/wake-up lines pulse time(6)			2			T_{APB}

1. Hysteresis voltage between Schmitt trigger switching levels.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{DD\_IO}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 6.2 on page 32* for more details.
3. Leakage could be higher than max. if negative current is injected on adjacent pins.
4. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor (see *Figure 25*). Data based on design simulation and/or technology characteristics, not tested in production.
5. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor.
6. To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

NRSTIN and NRSTOUT pins

NRSTIN Pin Input Driver is TTL/LVTTL as for all GP I/Os. A permanent pull-up is present which is the same as R_{PU} (see : General characteristics on page 54)

NRSTOUT Pin Output Driver is equivalent to the O2 type driver except that it works only as an open-drain (the P-MOS is de-activated). A permanent pull-up is present which is the same as R_{PU} (see : General characteristics on page 54)

Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

Table 35. NRSTIN and NRSTOUT pins

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
$V_{IL(NRSTIN)}$	NRSTIN Input low level voltage(1)					0.8	V
$V_{IH(NRSTIN)}$	NRSTIN Input high level voltage(1)			2			
$V_{hys(NRSTIN)}$	NRSTIN Schmitt trigger voltage hysteresis(2)				400		mV
$V_{OL(NRSTIN)}$	NRSTOUT Output low level voltage(3)	I_{IO}=+2 mA				0.4	V
$R_{PU(NRSTIN)}$	NRSTIN Weak pull-up equivalent resistor(4)	V_{IN}=V_{SS}	V_{DD_IO}=3.3 V	25	50	100	kΩ
			V_{DD_IO}=5 V	20	31	100	kΩ
$t_{w(RSTL)out}$	Generated reset pulse duration (visible at NRSTOUT pin)(5)	Internal reset source		15	20		µs
$t_{h(RSTL)in}$	External reset pulse hold time at NRSTIN pin(6)	At V_{DD_IO} power-up(5)		20			µs
		When V_{DD_IO} is established(5)		1			µs
$t_{g(RSTL)in}$	maximum negative spike duration filtered at NRSTIN pin(7)	The time between two spikes must be higher than 1/2 of the spike duration.			150		ns

1. Data based on product characterisation, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels.
3. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
4. The R_{PU} pull-up equivalent resistor are based on a resistive transistor
5. To guarantee the reset of the device, a minimum pulse of 15 µs has to be applied to the internal reset. At V_{DD_IO} power-up, the built-in reset stretcher may not generate the 15 µs pulse duration while once V_{DD_IO} is established, an external reset pulse will be internally stretched up to 15 µs thanks to the reset pulse stretcher.
6. The reset network (the resistor and two capacitors) protects the device against parasitic resets, especially in noisy environments.
7. In fact the filter is made to ignore all incoming pulses with short duration:
   - all negative spikes with a duration less than 150 ns are filtered
   - all trains of negative spikes with a ratio of 1/2 are filtered. This means that all spikes with a maximum duration of 150 ns with minimum interval between spikes of 75 ns are filtered.

   Data guaranteed by design, not tested in production.

Figure 28. SPI configuration - master mode, single transfer

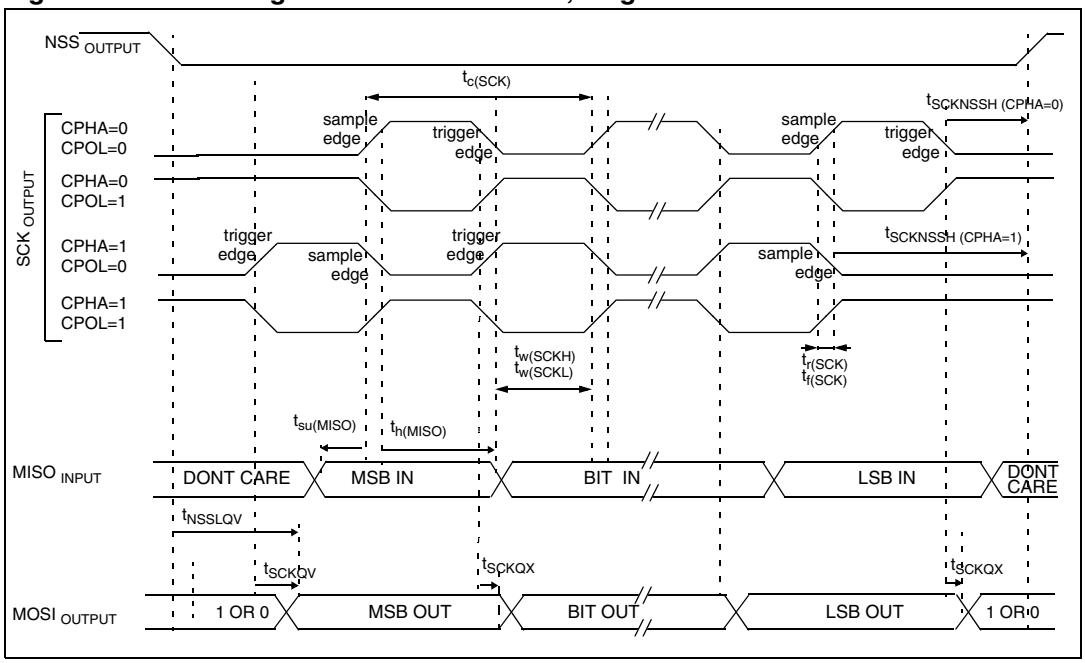


Figure 29. SPI configuration - master mode, continuous transfer, CPHA=0

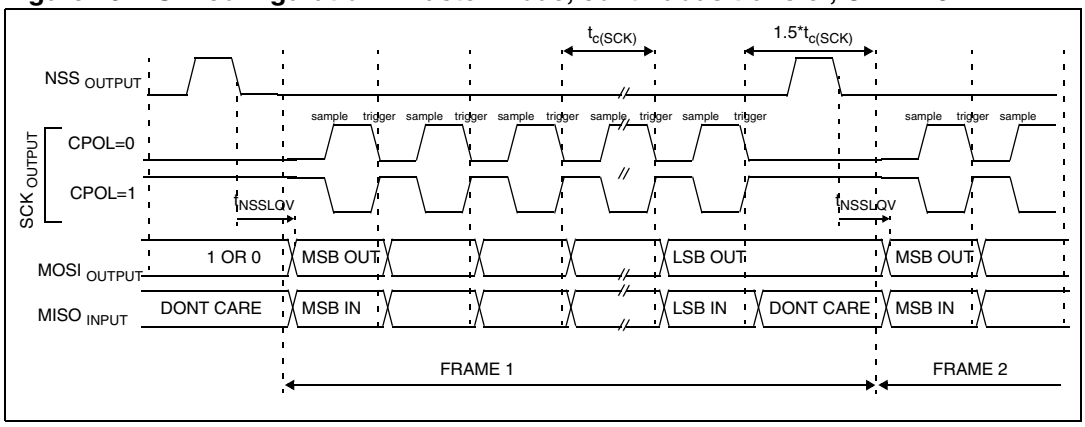


Figure 30. SPI configuration - master mode, continuous transfer, CPHA=1

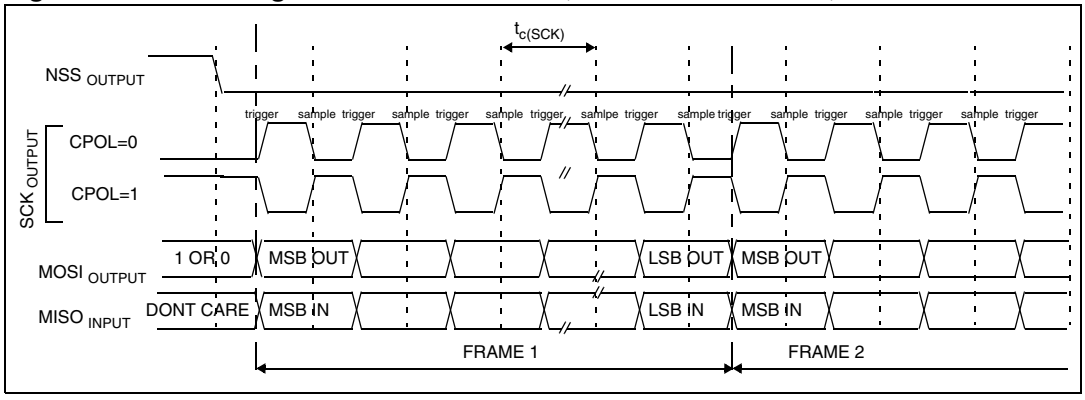


Figure 31. TI configuration - master mode, single transfer

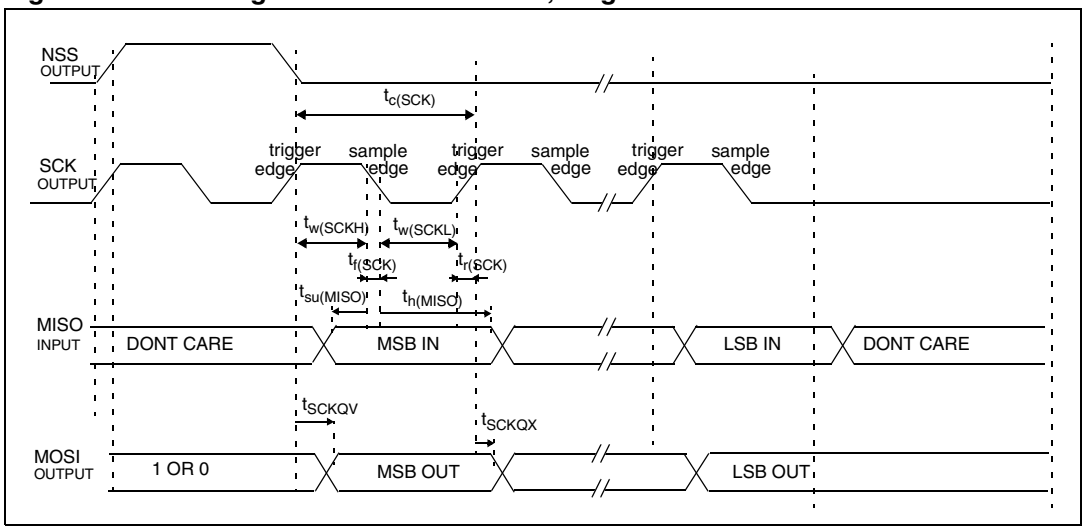
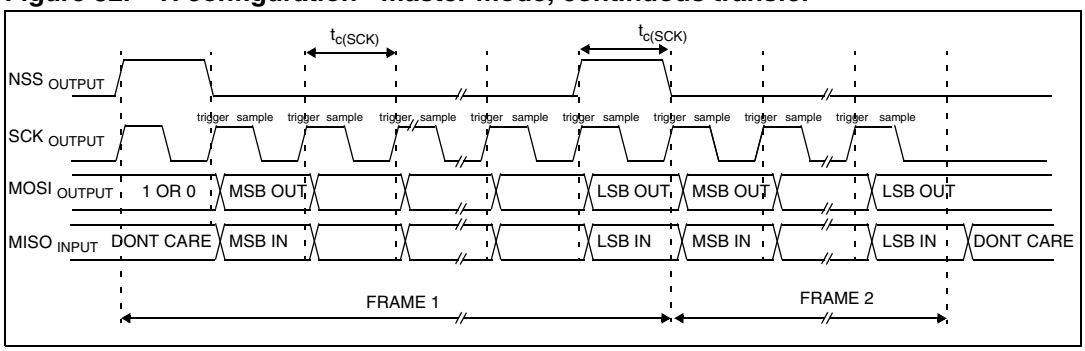


Figure 32. TI configuration - master mode, continuous transfer



SMI - serial memory interface

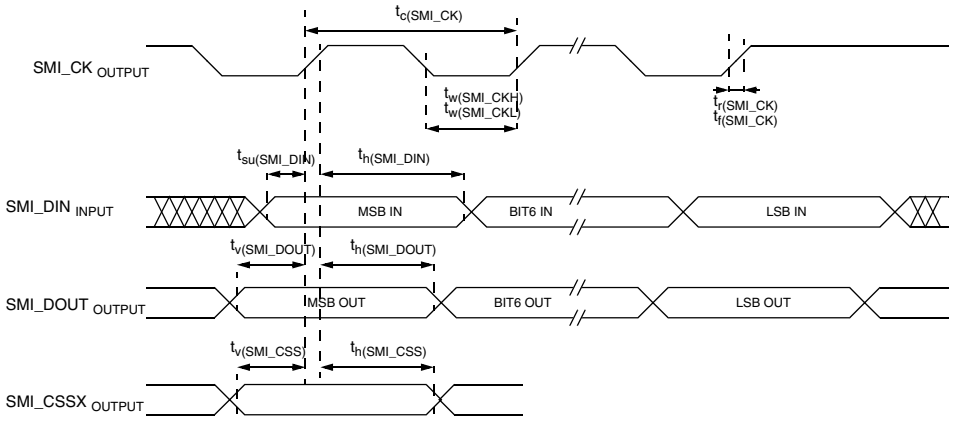
Subject to general operating conditions with $C_L \approx 30$ pF.

Table 40. SMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
f_{SMI_CK}	SMI clock frequency		32(2)(3)	MHz
			48(4)	
$t_{r(SMI\_CK)}$	SMI clock rise time		10	ns
$t_{f(SMI\_CK)}$	SMI clock fall time		8	
$t_{v(SMI\_DOUT)}$	Data output valid time		10	
$t_{h(SMI\_DOUT)}$	Data output hold time		0	
$t_{v(SMI\_CSSx)}$	CSS output valid time		10	
$t_{h(SMI\_CSSx)}$	CSS output hold time		0	
$t_{su(SMI\_DIN)}$	Data input setup time	0		
$t_{h(SMI\_DIN)}$	Data input hold time	5		

1. Data based on characterisation results, not tested in production.
2. Max. frequency = $f_{PCLK}/2 = 64/2 = 32$ MHz.
3. Valid for all temperature ranges: -40 to 105 °C, with 30 pF load capacitance.
4. Valid up to 60 °C, with 10 pF load capacitance.

Figure 39. SMI timing diagram



I²C - Inter IC control interface

Subject to general operating conditions for V_{DD_IO}, f_{PCLK}, and T_A unless otherwise specified.

The I²C interface meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Restriction: The I/O pins which SDA and SCL are mapped to are not “True” Open-Drain: when configured as open-drain, the PMOS connected between the I/O pin and V_{DD_IO} is disabled, but it is still present. Also, there is a protection diode between the I/O pin and V_{DD_IO}. Consequently, when using this I²C in a multi-master network, it is

Table 44. USB: Full speed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_{rfm}	Rise/ Fall Time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal Crossover Voltage		1.3	2.0	V

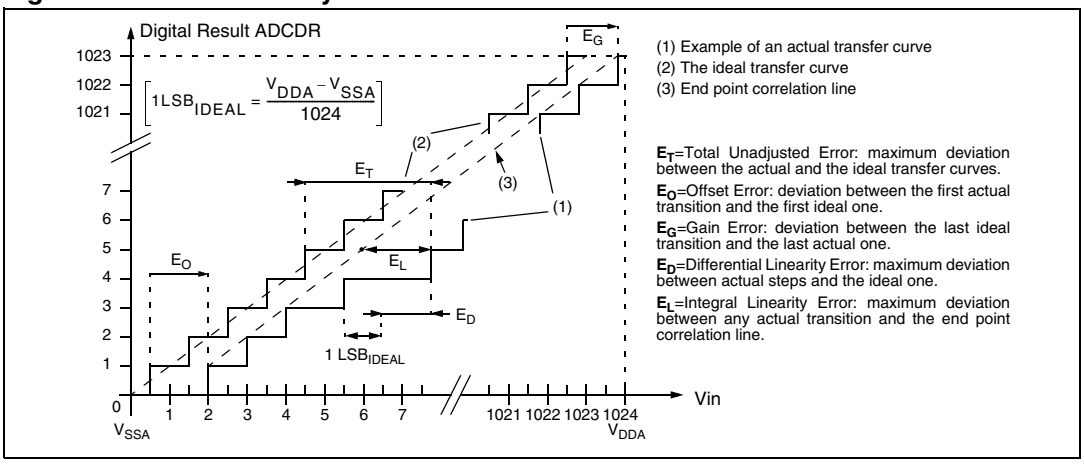
1. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

Table 47. ADC accuracy

ADC accuracy with f_{CK_SYS} = 20 MHz, f_{ADC}=8 MHz, R_{AIN} < 10 kΩ This assumes that the ADC is calibrated(1)					
Symbol	**Parameter**	**Conditions**	**Typ**	**Max**	**Unit**
$\|E_T\|$	Total unadjusted error (2) (3)	V_{DDA_ADC}=3.3 V	1	1.2	LSB
		V_{DDA_ADC}=5.0 V	1	1.2	
$\|E_O\|$	Offset error(2) (3)	V_{DDA_ADC}=3.3 V	0.15	0.5	
		V_{DDA_ADC}=5.0 V	0.15	0.5	
E_G	Gain Error (2) (3)	V_{DDA_ADC}=3.3 V	-0.8	-0.2	
		V_{DDA_ADC}=5.0 V	-0.8	-0.2	
$\|E_D\|$	Differential linearity error(2) (3)	V_{DDA_ADC}=3.3 V	0.7	0.9	
		V_{DDA_ADC}=5.0 V	0.7	0.9	
$\|E_L\|$	Integral linearity error (2) (3)	V_{DDA_ADC}=3.3 V	0.6	0.8	
		V_{DDA_ADC}=5.0 V	0.6	0.8	

1. Calibration is needed once after each power-up.
2. Refer to *ADC accuracy vs. negative injection current on page 73*
3. ADC Accuracy vs. MCO (Main Clock Output): the ADC accuracy can be significantly degraded when activating the MCO on pin P0.01 while converting an analog channel (especially those which are close to the MCO pin). To avoid this, when an ADC conversion is launched, it is strongly recommended to disable the MCO.

Figure 44. ADC accuracy characteristics

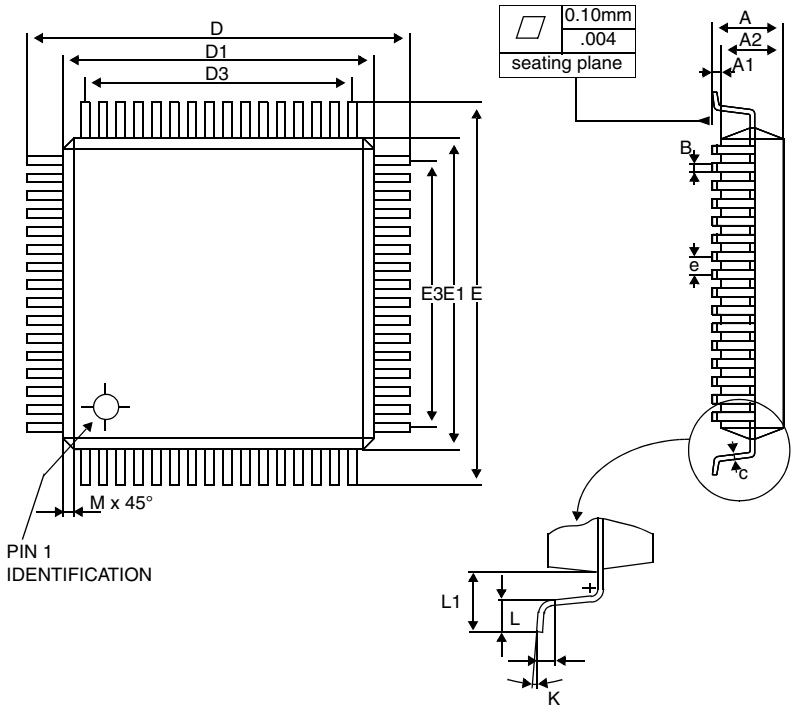


7 Package characteristics

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 Package mechanical data

Figure 45. 64-pin low profile quad flat package (10x10)



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of pins					
N	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 10: General operating conditions on page 34*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in ° C/W,
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$),
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum Power Dissipation on Output Pins.
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 48. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 100 - 14 x 14 mm / 0.5 mm pitch	46	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 100 - 10 x 10 x 1.7mm	41	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org