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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, SPI, SSI, SSP, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str755fr0t6

Serial memory interface (SMI)

The Serial Memory interface is directly able to access up to 4 serial FLASH devices. It can be used to access data, execute code directly or boot the application from external memory. The memory is addressed as 4 banks of up to 16 Mbytes each.

Clocks and start-up

After RESET or when exiting from Low Power Mode, the CPU is clocked immediately by an internal RC oscillator (FREEOSC) at a frequency centered around 5 MHz, so the application code can start executing without delay. In parallel, the 4/8 MHz Oscillator is enabled and its stabilization time is monitored using a dedicated counter.

An oscillator failure detection is implemented: when the clock disappears on the XT1 pin, the circuit automatically switches to the FREEOSC oscillator and an interrupt is generated.

In Run mode, the AHB and APB clock speeds can be set at a large number of different frequencies thanks to the PLL and various prescalers: up to 60 MHz for AHB and up to 32 MHz for APB when fetching from Flash (64 MHz and 32 MHz when fetching from SRAM).

In SLOW mode, the AHB clock can be significantly decreased to reduce power consumption.

The built-in Clock Controller also provides the 48 MHz USB clock directly without any extra oscillators or PLL. For instance, starting from the 4 MHz crystal source, it is possible to obtain in parallel 60 MHz for the AHB clock, 48 MHz for the USB clock and 30 MHz for the APB peripherals.

Boot modes

At start-up, boot pins are used to select one of five boot options:

- Boot from internal flash
- Boot from external serial Flash memory
- Boot from internal boot loader
- Boot from internal SRAM

Booting from SMI memory allows booting from a serial flash. This way, a specific boot monitor can be implemented. Alternatively, the STR750F can boot from the internal boot loader that implements a boot from UART.

Power supply schemes

You can connect the device in any of the following ways depending on your application.

- **Power Scheme 1: Single external 3.3V power source**. In this configuration the V_{CORE} supply required for the internal logic is generated internally by the main voltage regulator and the V_{BACKUP} supply is generated internally by the low power voltage regulator. This scheme has the advantage of requiring only one 3.3V power source.
- **Power Scheme 2: Dual external 3.3V and 1.8V power sources.** In this configuration, the internal voltage regulators are switched off by forcing the VREG_DIS pin to high level. V_{CORE} is provided externally through the V_{18} and V_{18REG} power pins and V_{BACKUP} through the V_{18_BKP} pin. This scheme is intended to save power consumption for applications which already provide an 1.8V power supply.
- **Power Scheme 3: Single external 5.0V power source.** In this configuration the V_{CORE} supply required for the internal logic is generated internally by the main voltage

regulator and the V_{BACKUP} supply is generated internally by the low power voltage regulator. This scheme has the advantage of requiring only one 5.0V power source.

- **Power Scheme 4: Dual external 5.0V and 1.8V power sources.** In this configuration, the internal voltage regulators are switched off, by forcing the VREG_DIS pin to high level. V_{CORE} is provided externally through the V_{18} and V_{18REG} power pins and V_{BACKUP} through the V_{18_BKP} pin. This scheme is intended to provide 5V I/O capability.

Caution: When powered by 5.0V, the USB peripheral cannot operate.

Low power modes

The STR750F supports 5 low power modes, SLOW, PCG, WFI, STOP and STANDBY.

- SLOW MODE: the system clock speed is reduced. Alternatively, the PLL and the main oscillator can be stopped and the device is driven by a low power clock (f_{RTC}). The clock is either an external 32.768 kHz oscillator or the internal low power RC oscillator.
- PCG MODE (Peripheral Clock Gating MODE): When the peripherals are not used, their APB clocks are gated to optimize the power consumption.
- WFI MODE (Wait For Interrupts): only the CPU clock is stopped, all peripherals continue to work and can wake-up the CPU when IRQs occur.
- STOP MODE: all clocks/peripherals are disabled. It is also possible to disable the oscillators and the Main Voltage Regulator (In this case the V_{CORE} is entirely powered by V_{18_BKP}). This mode is intended to achieve the lowest power consumption with SRAM and registers contents retained. The system can be woken up by any of the external interrupts / wake-up lines or by the RTC timer which can optionally be kept running. The RTC can be clocked either by the 32.768 kHz Crystal or the Low Power RC Oscillator.
  Alternatively, STOP mode gives flexibility to keep the either main oscillator, or the Flash or the Main Voltage Regulator enabled when a fast start after wake-up is preferred (at the cost of some extra power consumption).
- STANDBY MODE: This mode (only available in single supply power schemes) is intended to achieve the lowest power consumption even when the temperature is increasing. The digital power supply (V_{CORE}) is completely removed (no leakage even at high ambient temperature). SRAM and all register contents are lost. Only the RTC remains powered by V_{18_BKP}. The STR750F can be switched back from STANDBY to RUN mode by a trigger event on the WKP_STDBY pin or an alarm timeout on the RTC counter.

Caution: It is important to bear in mind that it is forbidden to remove power from the V_{DD_IO} power supply in any of the Low Power Modes (even in STANDBY MODE).

DMA

The flexible 4-channel general-purpose DMA is able to manage memory to memory, peripheral to memory and memory to peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

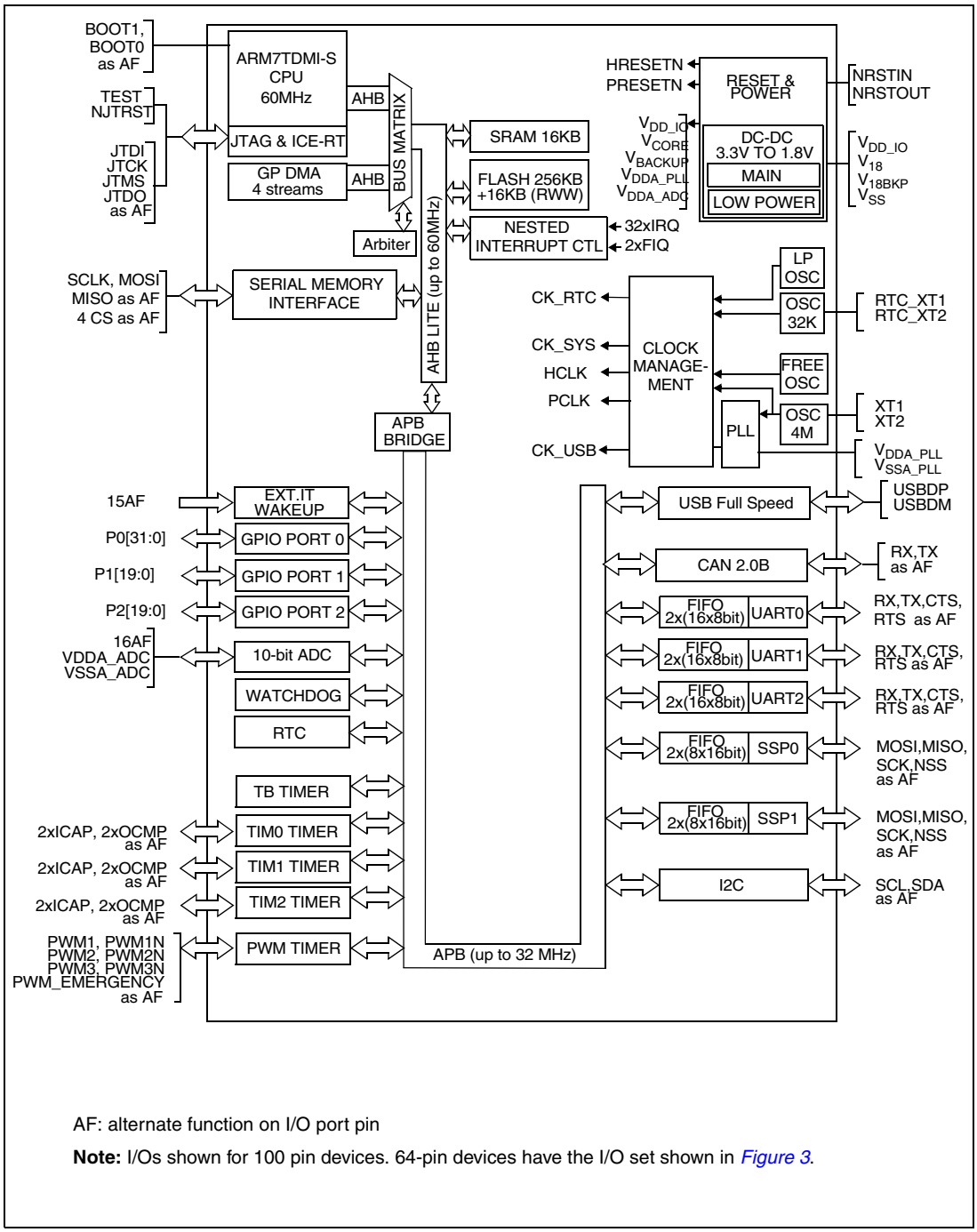
The DMA can be used with the main peripherals: UART0, SSP0, Motor control PWM timer (PWM), standard timer TIM0 and ADC.

RTC (real-time clock)

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a

3.2 Block diagram

Figure 1. STR750 block diagram



AF: alternate function on I/O port pin

Note: I/Os shown for 100 pin devices. 64-pin devices have the I/O set shown in *Figure 3*.

4.1 Pin description table

Legend / abbreviations for *Table 6*:

Type:	I = input, O = output, S = supply,
Input levels:	All Inputs are LVTTL at V_{DD_IO} = 3.3V+/-0.3V or TTL at V_{DD_IO} = 5V± 0.5V. In both cases, T_T means V_{ILmax} =0.8V V_{IHmin}=2.0V
Inputs:	All inputs can be configured as floating or with internal weak pull-up or pull down (pu/pd)
Outputs:	All Outputs can be configured as Open Drain (OD) or Push-Pull (PP) (see also note 6 below *Table 6*). There are 3 different types of Output with different drives and speed characteristics: – O8: f_{max} = 40 MHz on C_L=50pF and 8 mA static drive capability for V_{OL}=0.4V and up to 20 mA for V_{OL}=1.3V (see*Output driving current on page 55*) – O4: f_{max} = 20 MHz on C_L=50pF and 4 mA static drive capability for V_{OL}=0.4V (see*Output driving current on page 55*) – O2: f_{max} = 10 MHz on C_L=50pF and 2 mA static drive capability of for V_{OL}=0.4V (see*Output driving current on page 55*)
External interrupts/wake-up lines:	EITx

Port reset state

The reset state of the I/O ports is GPIO input floating. Exceptions are P1[19:16] and P0.13 which are configured as JTAG alternate functions:

- The JTAG inputs (JTDI, JTMS and JTDI) are configured as input floating and are ready to accept JTAG sequences.
- The JTAG output JTDO is configured as floating when idle (no JTAG operation) and is configured in output push-pull only when serial JTAG data must be output.
- The JTAG output RTCK is always configured as output push-pull. It outputs '0' level during the reset phase and then outputs the JTCK input signal resynchronized 3 times by the internal AHB clock.
- The GPIO_PCx registers do not control JTAG AF selection, so the reset values of GPIO_PCx for P1[19:16] and P0. 13 are the same as other ports. Refer to the GPIO section of the STR750 Reference Manual for the register description and reset values.
- P0.11 and P0.00 are sampled by the boot logic after reset, prior to fetching the first word of user code at address 0000 0000h.
- When booting from SMI (and only in this case), the reset state of the following GPIOs is "SMI alternate function output enabled":
  - P0.07 (SMI_DOUT)
  - P0.05 (SMI_CLK)
  - P0.04 (SMI_CS0)
  - P0.06 (SMI_DIN)

  Note that the other SMI pins: SMI_CS1,2,3 (P0.12, P0.11, P0.10) are not affected.

To avoid excess power consumption, unused I/O ports must be tied to ground.

Table 6. STR750F pin description

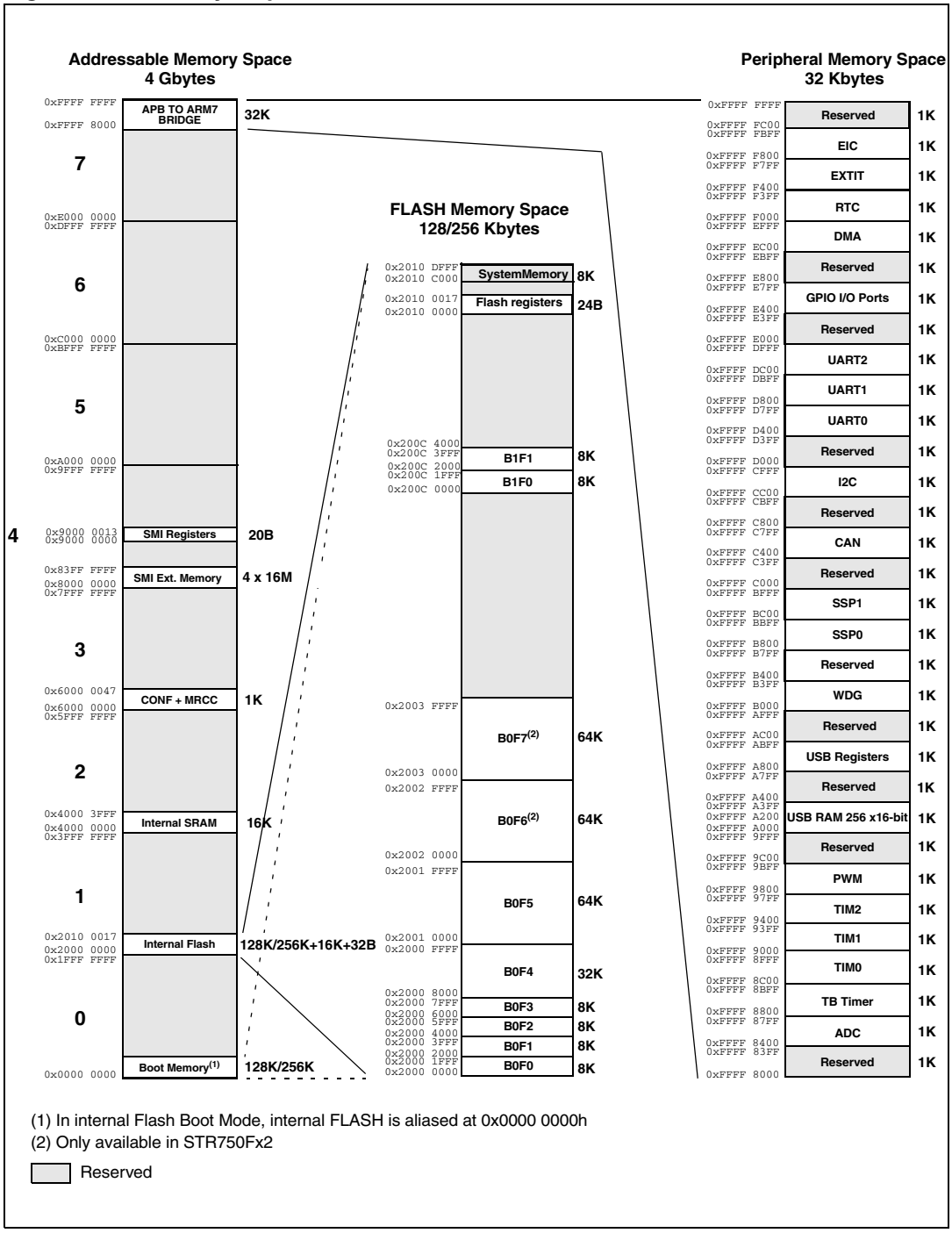
Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100[1]	LFBGA100[1]	LQFP64[2]	LFBGA64[2]			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD [3]	PP				
1	B1	1	B1	P1.12 / ADC_IN13	I/O	T_T	**X**	X	EIT12	O8	X	X		**Port 1.12**	ADC: Analog input 13	
2	B2	2	C2	P0.02 / TIM2_OC1 / ADC_IN0	I/O	T_T	**X**	X	EIT0	O8	X	X		**Port 0.02**	TIM2: Output Compare 1[4]	ADC: Analog input 0
3	B3	3	C1	P0.01 / TIM0_TI1 / MCO	I/O	T_T	**X**	X		O8	X	X		**Port 0.01**	TIM0: Input Capture / trigger / external clock 1	Main Clock Output
4	C2	4	C3	P0.00 / TIM0_OC1 / BOOT0	I/O	T_T	**X**	X		O8	X	X		**Port 0.00 / Boot mode selection input 0**	TIM0: Output Compare 1	
5	C1			P0.31 / TIM1_TI2	I/O	T_T	**X**	X		O2	X	X		**Port 0.31**	TIM1: Input Capture / trigger / external clock 2	
6	D2			P0.30 / TIM1_OC2	I/O	T_T	**X**	X		O2	X	X		**Port 0.30**	TIM1: Output Compare 2	

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
68	A10			P1.02 / TIM2_OC2	I/O	T_T	X	X		O2	X	X		**Port 1.02**	TIM2: Output compare 2 (remappable to P0.06)(8)	
69	D7	44	C6	VDD_IO	S									Supply Voltage for digital I/Os		
70	D8	45	D6	VDDA_ADC	S									Supply Voltage for A/D converter		
71	C9			P2.11	I/O	T_T	X	X		O2	X	X		**Port 2.11**		
72	B10			P2.10	I/O	T_T	X	X		O2	X	X		**Port 2.10**		
73	C8	46	D7	VSSA_ADC	S									Ground Voltage for A/D converter		
74	C7	47	C7	VSS_IO	S									Ground Voltage for digital I/Os		
75	E8	48	D5	VREG_DIS	I	T_T								Voltage Regulator Disable input		
76	A9	49	A8	P0.07 / SMI_DOUT / SSP0_MOSI	I/O	T_T	X	X	EIT2	O4	X	X		**Port 0.07**	Serial Memory Interface: data output	SSP0: Master out Slave in data
77	A8	50	A7	P0.06 / SMI_DIN / SSP0_MISO	I/O	T_T	X	X		O4	X	X		**Port 0.06**	Serial Memory Interface: data input	SSP0: Master in Slave out data
78	A7	51	A6	P0.05 / SSP0_SCLK / SMI_CK	I/O	T_T	X	X	EIT1	O4	X	X		**Port 0.05**	SSP0: Serial clock	Serial Memory Interface: Serial clock output
79	B7	52	B6	P0.04 / SMI_CS0 / SSP0_NSS	I/O	T_T	X	X		O4	X	X		**Port 0.04**	Serial Memory Interface: chip select output 0	SSP0: Slave select input
80	C5	53	B7	P1.10 PWM_EMERGENCY	I/O	T_T	X	X	EIT10	O2	X	X		**Port 1.10**	PWM: Emergency input	
81	B6	54	B5	P1.09 / PWM1	I/O	T_T	X	X	EIT9	O4	X	X		**Port 1.09**	PWM: PWM1 output	
82	C6			P2.09 / PWM1N	I/O	T_T	X	X		O2	X	X		**Port 2.09**	PWM: PWM1 complementary output(4)	
83	G7			P2.08 / PWM2	I/O	T_T	X	X		O2	X	X		**Port 2.08**	PWM: PWM2 output(4)	
84	G6			P2.07 / PWM2N	I/O	T_T	X	X		O2	X	X		**Port 2.07**	PWM: PWM2 complementary output(4)	
85	F7			P2.06 / PWM3	I/O	T_T	X	X		O2	X	X		**Port 2.06**	PWM: PWM3 output(4)	
86	F6			P2.05 / PWM3N	I/O	T_T	X	X		O2	X	X		**Port 2.05**	PWM: PWM3 complementary output(4)	
87	A6	55	A5	P1.08 / PWM1N / ADC_IN11	I/O	T_T	X	X		O4	X	X		**Port 1.08**	PWM: PWM1 complementary output(8)	ADC: analog input 11
88	B5	56	B4	P1.07 / PWM2	I/O	T_T	X	X	EIT8	O4	X	X		**Port 1.07**	PWM: PWM2 output(4)	
89	A5	57	A4	P1.06 / PWM2N / ADC_IN10	I/O	T_T	X	X		O4	X	X		**Port 1.06**	PWM: PWM2 complementary output(4)	ADC: analog input 10
90	B4	58	B3	P1.05 / PWM3	I/O	T_T	X	X	EIT7	O4	X	X		**Port 1.05**	PWM: PWM3 output(4)	

5 Memory map

Figure 5. Memory map



(1) In internal Flash Boot Mode, internal FLASH is aliased at 0x0000 0000h
(2) Only available in STR750Fx2

Reserved

6.3 Operating conditions

6.3.1 General operating conditions

Subject to general operating conditions for V_{DD_IO}, and T_A unless otherwise specified.

Table 10. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB Clock frequency	Accessing SRAM with 0 wait states	0	64	MHz
		Accessing Flash in burst mode, $T_A \leq 85°$ C	0	60	
		Accessing Flash in burst mode $T_A > 85°$ C		56	
		Accessing Flash with 0 wait states	0	32	
		Write access to Flash registers(1)	0	30	
		Accessing Flash in RWW mode	0	16	
f_{PCLK}	Internal APB Clock frequency		0	32	MHz
V_{DD_IO}	Standard Operating Voltage Power Scheme 1 & 2		3.0	3.6	V
	Standard Operating Voltage Power Scheme 3 & 4		4.5	5.5	
V_{18}	Standard Operating Voltage Power Scheme 2 & 4		1.65	1.95	
P_D	Power dissipation at $T_A = 85°$ C for suffix 6 or $T_A = 105°$ C for suffix 7(2)	LQFP100		434	mW
		LQFP64		444	
		LFBGA100		487	
		LFBGA64		344	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
		Low power dissipation(3)	-40	105	°C
	Ambient temperature for 7 suffix version	Maximum power dissipation	-40	105	°C
		Low power dissipation (3)	-40	125	°C
T_J	Junction temperature range	6 Suffix Version	-40	105	°C
		7 Suffix Version	-40	125	°C

1. Write access to Flash registers is either a program, erase, set protection or un-set protection operation.
2. If T_A is lower, higher PD values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.2: Thermal characteristics on page 79*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.2: Thermal characteristics on page 79*).

Table 16. Dual supply supply typical power consumption in Run, WFI, Slow and Slow-WFI modes

To calculate the power consumption in Dual supply mode, refer to the values given in *Table 15*. and consider that this consumption is split as follows:

$I_{DD(single\ supply)} \sim I_{DD(dual\ supply)} = I_{DD\_V18} + I_{DD(VDD\_IO)}$

For 3.3V range: $I_{DD(VDD\_IO)}$ ~ 1 to 2 mA

For 5V range: $I_{DD(VDD\_IO)}$ ~ 2 to 3 mA

Therefore most of the consumption is sunk on the V_{18} power supply

This formula does not apply in STOP and STANDBY modes, refer to *Table 17*.

Subject to general operating conditions for V_{DD_IO}, and T_A

Table 17. Typical power consumption in STOP and STANDBY modes

Symbol	Parameter	Conditions		3.3V Typ(1)	5V Typ(2)	Unit
I_{DD}(3)	Supply current in STOP mode(4)	LP_PARAM bits: ALL OFF(5)		12	15	µA
		LP_PARAM bits : MVREG ON, OSC4M OFF, FLASH OFF(6)		130	135	
		LP_PARAM bits: MVREG ON, OSC4M ON , FLASH OFF(6)		1950	1930	
		LP_PARAM bits: MVREG ON, OSC4M OFF, FLASH ON (6)		630	635	
		LP_PARAM bits: MVREG ON, OSC4M ON, FLASH ON (6)		2435	2425	
	Supply current in STOP mode(7)	LPPARAM bits: ALL OFF, with V_{18}=1.8 V	I_{DD_V18} I_{DD_V33}	5 <1	5 <1	µA
		LP_PARAM bits: OSC4M ON, FLASH OFF	I_{DD_V18} I_{DD_V33}	410 1475	410 1435	
		LP_PARAM bits: OSC4M OFF, FLASH ON	I_{DD_V18} I_{DD_V33}	550 <1	550 1	
		LP_PARAM bits: OSC4M ON, FLASH ON	I_{DD_V18} I_{DD_V33}	910 1475	910 1445	
	Supply current in STANDBY mode(4)	RTC OFF		11	14	µA
		RTC ON clocked by OSC32K		14	18	

1. Typical data are based on T_A=25°C, V_{DD_IO}=3.3 V and V_{18}=1.8 V unless otherwise indicated in the table.
2. Typical data are based on T_A=25°C, V_{DD_IO}=5.0 V and V_{18}=1.8 V unless otherwise indicated in the table.
3. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4 on page 36*.
4. Single supply scheme see *Figure 12*.
5. In this mode, the whole digital circuitry is powered internally by the LPVREG at approximately 1.4 V, which significantly reduces the leakage currents.
6. In this mode, the whole digital circuitry is powered internally by the MVREG at 1.8 V.
7. Dual supply scheme see *Figure 13*.

Supply and clock manager power consumption

Table 18. Supply and clock manager power consumption

Symbol	Parameter	Conditions[1]	3.3V Typ	5V Typ	Unit
$I_{DD(OSC4M)}$	Supply current of resonator oscillator in STOP or WFI mode (LP_PARAM bit: OSC4M ON)	External components specified in: *4/8 MHz crystal / ceramic resonator oscillator (XT1/XT2) on page 46*	1815	1795	µA
$I_{DD(FLASH)}$	FLASH static current consumption in STOP or WFI mode (LP_PARAM bit FLASH ON)		515	515	
$I_{DD(MVREG)}$	Main Voltage Regulator static current consumption in STOP mode (LP_PARAM bit: MVREG ON)		130	135	
$I_{DD(LPVREG)}$	Low Power Voltage Regulator + RSM current static current consumption	STOP mode includes leakage where V_{18} is internally set to 1.4 V	12	15	
		STANDBY mode where V_{18BKP} and V_{18} are internally set to 1.4 V and 0 V respectively	11	14	

1. Measurements performed in 3.3V single supply mode see *Figure 12*

difference between N+1 consecutive clock rising edges and T_{min} is the minimum time difference between N+1 consecutive clock rising edges.

N should be kept sufficiently large to have a long term jitter (ex: thousands).

For N=1, this becomes the single period jitter.

See *Figure 23*

- Cycle-to-cycle jitter (N period jitter)

  This corresponds to the time variation between adjacent cycles over a random sample of adjacent clock cycles pairs. Jitter(cycle-to-cycle) = Max(Tcycle n- Tcycle n-1) for n=1 to N.

  See *Figure 24*

Figure 23. Self-referred jitter (single and long term)

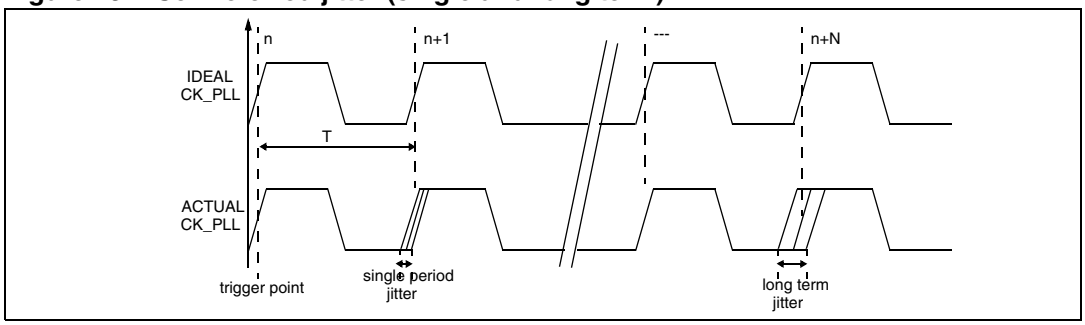
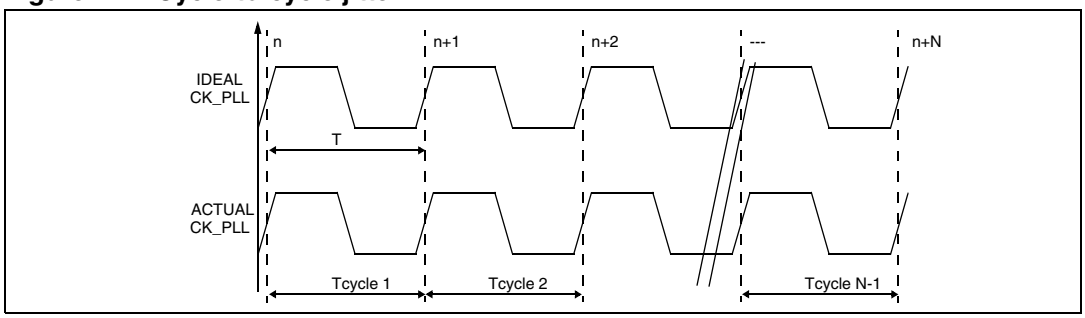


Figure 24. Cycle-to-cycle jitter



PLL characteristics

Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 24. PLL characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock			4.0		MHz
	PLL input clock duty cycle		40		60	%
f_{PLL_OUT}	PLL multiplier output clock	f_{PLL_IN}x 24			165	MHz
f_{VCO}	VCO frequency range	When PLL operates (locked)	336		960	MHz
t_{LOCK}	PLL lock time				300	µs
$\Delta t_{JITTER1}$(2)(3)	Single period jitter (+/-3Σ peak to peak)	f_{PLL_IN} = 4 MHz(4) V_{DD_IO} is stable			+/-250	ps
$\Delta t_{JITTER2}$(2)(3)	Long term jitter (+/-3Σ peak to peak)	f_{PLL_IN} = 4 MHz(4) V_{DD_IO} is stable			+/-2.5	ns
$\Delta t_{JITTER3}$(2)(3)	Cycle to cycle jitter (+/-3Σ peak to peak)	f_{PLL_IN} = 4 MHz(4) V_{DD_IO} is stable			+/-500	ps

1. Data based on product characterisation, not tested in production.
2. Refer to jitter terminology in *: PLL characteristics on page 47* for details on how jitter is specified.
3. The jitter specification holds true only up to 50mV (peak-to-peak) noise on V_{DDA_PLL} and V_{18} supplies. Jitter will increase if the noise is more than 50mV. In addition, it assumes that the input clock has no jitter.
4. The PLL parameters (MX1, MX0, PRESC1, PRESC2) must respect the constraints described in*: PLL characteristics on page 47*.

Internal RC oscillators (FREEOSC & LPOSC)

Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 25. Internal RC oscillators (FREEOSC & LPOSC)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{CK\_FREEOSC}$	FREEOSC Oscillator Frequency		3	5	8	MHz
f_{CK_LPOSC}	LPOSC Oscillator Frequency		150	300	500	kHz

Electro magnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 29. EMI characteristics

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f_{OSC4M}/f_{HCLK}]		Unit
				4/32MHz	4/60MHz	
S_{EMI}	Peak level	Flash devices: V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, LQFP64 package conforming to SAE J 1752/3	0.1 MHz to 30 MHz	22	26	dBµV
			30 MHz to 130 MHz	31	26	
			130 MHz to 1 GHz	19	23	
			SAE EMI Level	>4	>4	-

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electro-Static discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard.

Table 30. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25° C	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)		200	
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charge Device Model)		750	

1. Data based on product characterisation, not tested in production.

Table 37. PWM Timer (PWM)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(PWM)}$	PWM resolution time	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
		$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	16.6(1)			ns
Res_{PWM}	PWM resolution				16	bit
V_{OS}(1)	PWM/DAC output step voltage	V_{DD_IO}=3.3 V, Res=16-bits		50(1)		µV
		V_{DD_IO}=5.0 V, Res=16-bits		76(1)		µV
$t_{COUNTER}$	Timer clock period when internal clock is selected		1		65536	t_{CK_TIM}
		f_{CK_TIM}=60 MHz	0.0166		1087	µs
t_{MAX_COUNT}	Maximum Possible Count				65536x 65536	t_{CK_TIM}
		$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s

1. Take into account the frequency limitation due to the I/O speed capability when outputting the PWM to an I/O pin, as described in *: Output speed on page 57*.

Figure 31. TI configuration - master mode, single transfer

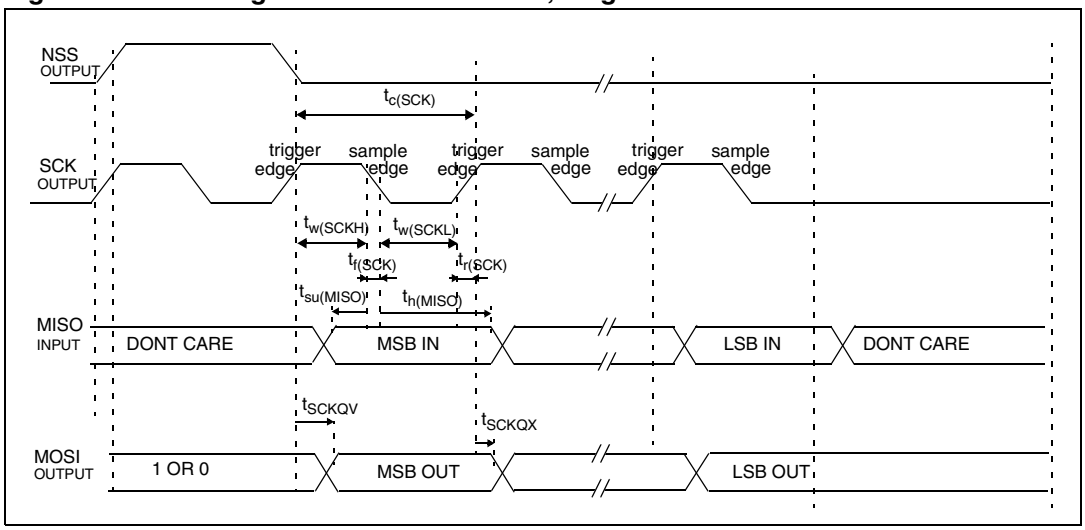
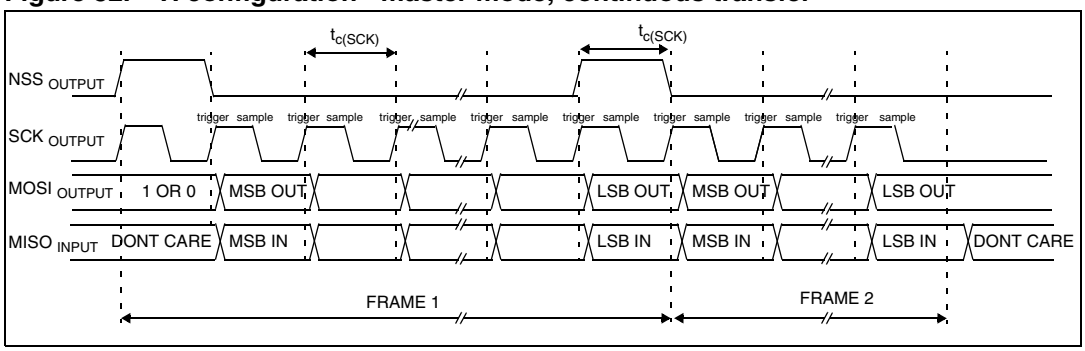


Figure 32. TI configuration - master mode, continuous transfer



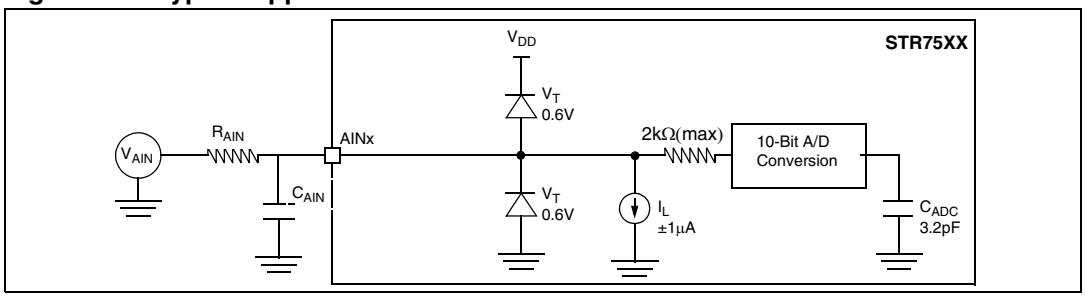
ADC accuracy vs. negative injection current

Injecting negative current on specific pins listed in *Table 46* (generally adjacent to the analog input pin being converted) should be avoided as this significantly reduces the accuracy of the conversion being performed. It is recommended to add a Schottky diode (pin to ground) to pins which may potentially inject negative current.

Table 46. List of adjacent pins

Analog input	Related adjacent pins
a	None
AIN1/P0.03	None
AIN2/P0.12	P0.11
AIN3/P0.17	P0.18 and P0.16
AIN4/P0.19	P0.24
AIN5/P0.22	None
AIN6/P0.23	P2.04
AIN7/P0.27	P1.11 and P0.26
AIN8/P0.29	P0.30 and P0.28
AIN9/P1.04	None
AIN10/P1.06	P1.05
AIN11/P1.08	P1.04 and P1.13
AIN12/P1.11	P2.17 and P0.27
AIN13/P1.12	None
AIN14/P1.13	P1.14 and P1.01
AIN15/P1.14	None

Figure 42. Typical application with ADC



Analog power supply and reference pins

The V_{DDA_ADC} and V_{SSA_ADC} pins are the analog power supply of the A/D converter cell.

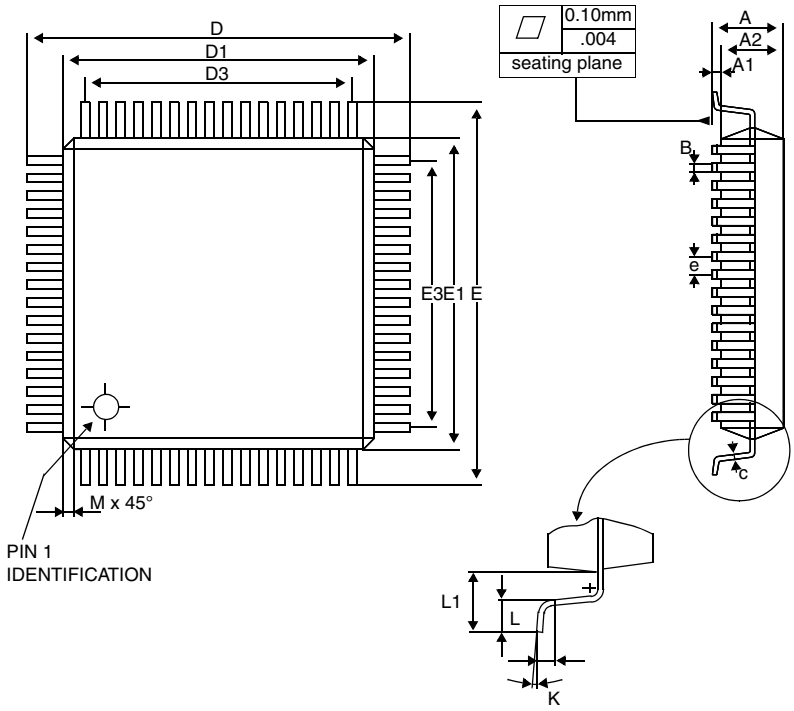
Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see *: General PCB design guidelines on page 74*).

7 Package characteristics

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 Package mechanical data

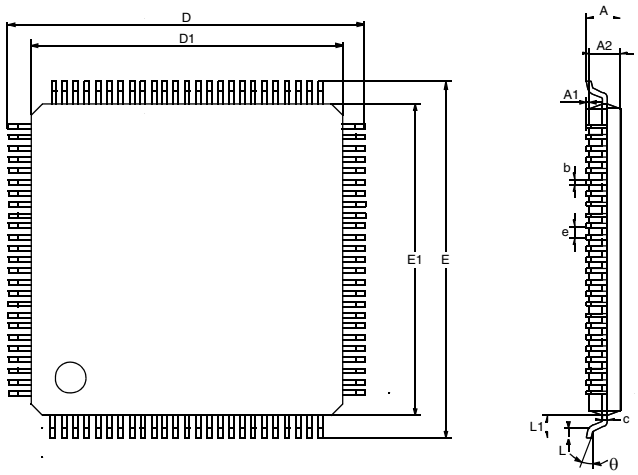
Figure 45. 64-pin low profile quad flat package (10x10)



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of pins					
N	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

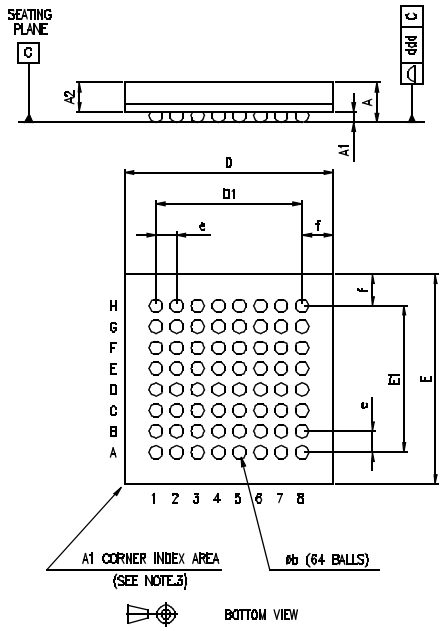
Figure 46. 100-pin low profile flat package (14x14)



Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		16.00			0.6299	
D1		14.00			0.5512	
E		16.00			0.6299	
E1		14.00			0.5512	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of Pins					
N	100					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47. 64-ball low profile fine pitch ball grid array package



Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	1.210		1.700	0.0476		0.0669
A1	0.270			0.0106		
A2		1.120			0.0441	
b	0.450	0.500	0.550	0.0177	0.0197	0.0217
D	7.750	8.000	8.150	0.3051	0.3150	0.3209
D1		5.600			0.2205	
E	7.750	8.000	8.150	0.3051	0.3150	0.3209
E1		5.600			0.2205	
e	0.720	0.800	0.880	0.0283	0.0315	0.0346
f	1.050	1.200	1.350	0.0413	0.0472	0.0531
ddd			0.120			0.0047
	Number of Pins					
N	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 10: General operating conditions on page 34*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in ° C/W,
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$),
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum Power Dissipation on Output Pins.
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 48. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 100 - 14 x 14 mm / 0.5 mm pitch	46	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 100 - 10 x 10 x 1.7mm	41	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

9 Revision history

Table 50. Document revision history

Date	Revision	Description of Changes
25-Sep-2006	1	Initial release
30-Oct-2006	2	Added power consumption data for 5V operation in *Section 6*
04-Jul-2007	3	Changed datasheet title from STR750F to STR750FXX STR751Fxx STR752Fxx STR755xx. Added *Table 1: Device summary on page 1* Added note 1 to *Table 6* Added STOP mode IDD max. values in *Table 14* Updated XT2 driving current in *Table 23.* Updated RPD in *Table 32* Updated *Table 21: XRTC1 external clock source on page 45* Updated *Table 34: Output speed on page 57* Added characteristics for *SSP synchronous serial peripheral in master mode (SPI or TI mode) on page 62* and *SSP synchronous serial peripheral in slave mode (SPI or TI mode) on page 65* Added characteristics for *SMI - serial memory interface on page 68* Added *Table 42: USB startup time on page 70*
23-Oct-2007	4	Updated *Section 6.2.3: Thermal characteristics on page 33* Updated P_D, T_J and T_A in *Section 6.3: Operating conditions on page 34* Updated *Table 20: XT1 external clock source on page 44* Updated *Table 21: XRTC1 external clock source on page 45* Updated *Section 7: Package characteristics on page 76* (inches rounded to 4 decimal digits instead of 3) Updated Ordering information *Section 8: Order codes on page 81*
17-Feb-2009	5	Modified note 3 below *Table 8: Current characteristics on page 33* Added AHB clock frequency for write access to Flash registers in *Table 10: General operating conditions on page 34* Modified note 3 below *Table 41: SDA and SCL characteristics on page 69*