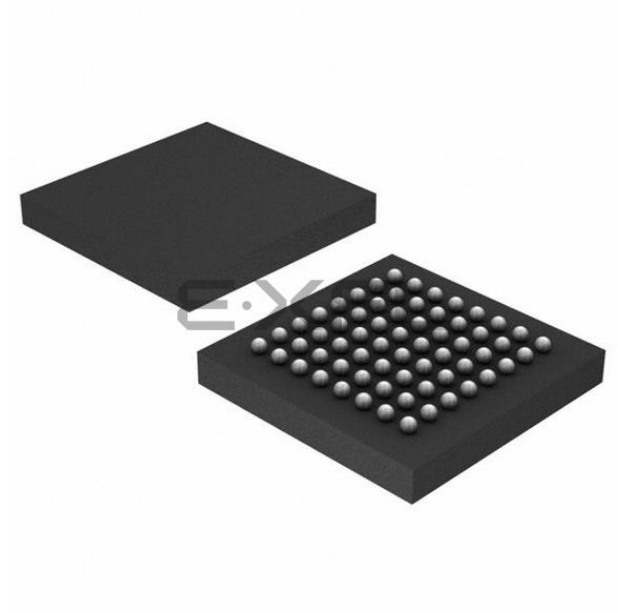

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, SPI, SSI, SSP, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str755fr1h6

Contents

1 Description

The STR750 family of 32-bit microcontrollers combines the industry-standard ARM7TDMI® 32-bit RISC core, featuring high performance, very low power, and very dense code, with a comprehensive set of peripherals and ST's latest 0.18µ embedded Flash technology. The STR750 family comprises a range of devices integrating a common set of peripherals as well as USB, CAN and some key innovations like clock failure detection and an advanced motor control timer. It supports both 3.3V and 5V, and it is also available in an extended temperature range (-40 to +105°C). This makes it a genuine general purpose microcontroller family, suitable for a wide range of applications:

- Appliances, brushless motor drives
- USB peripherals, UPS, alarm systems
- Programmable logic controllers, circuit breakers, inverters
- Medical and portable equipment

2 Device overview

Table 2. Device overview

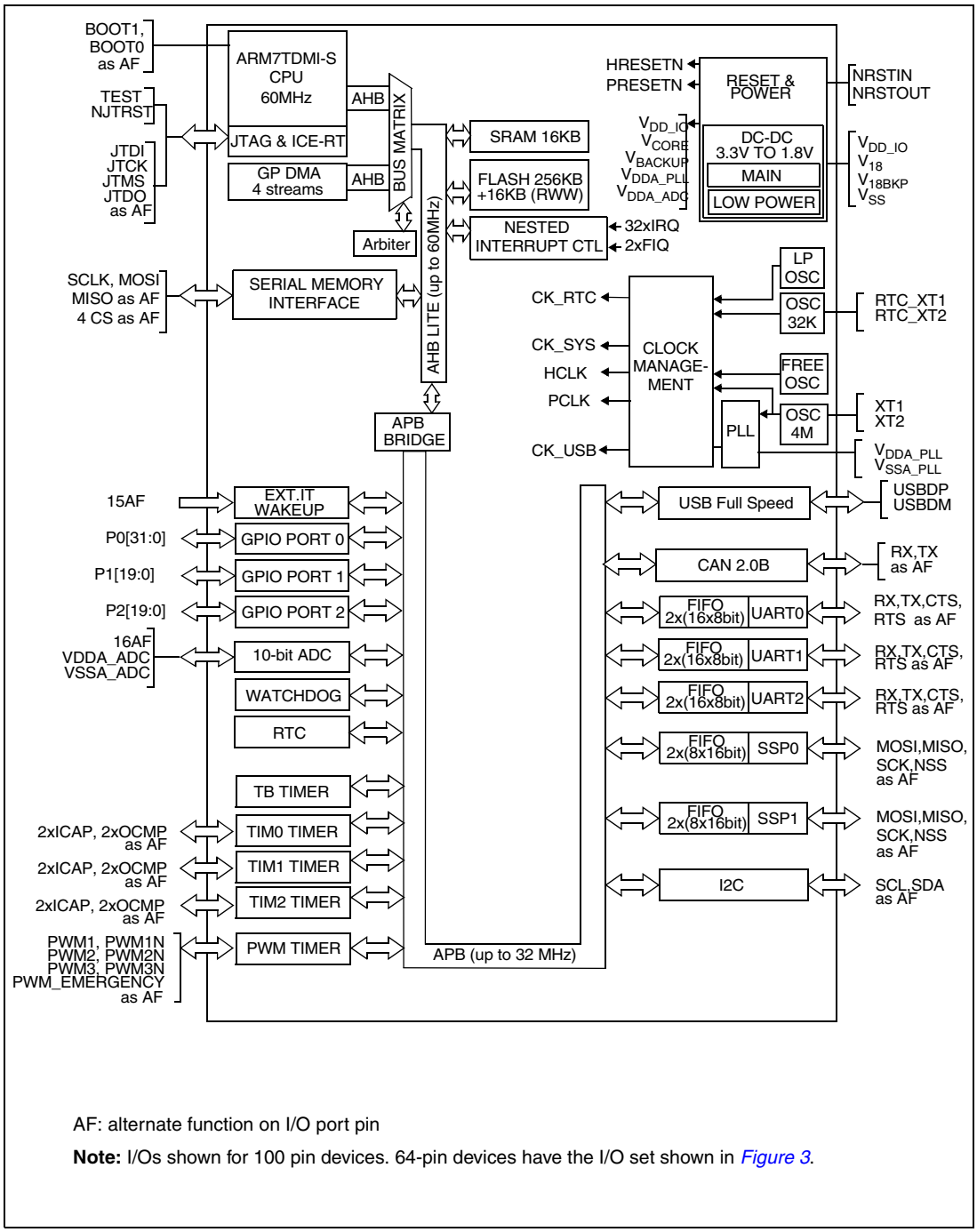
Features	STR755FR0 STR755FR1 STR755FR2	STR751FR0/ STR751FR1/ STR751FR2	STR752FR0/ STR752FR1/ STR752FR2	STR755FV0 STR755FV1/ STR755FV2	STR750FV0/ STR750FV1/ STR750FV2
Flash - Bank 0 (bytes)	64K/128K/256K				
Flash - Bank 1 (bytes)	16K RWW				
RAM (bytes)	16K				
Operating Temperature.	Ambient temp.:-40 to +85°C / -40 to +105°C (see *Table 49*) Junction temp. -40 to + 125 °C (see *Table 10*)				
Common Peripherals	3 UARTs, 2 SSPs, 1 I2C, 3 timers 1 PWM timer, 38 I/Os 13 Wake-up lines, 11 A/D Channels			3 UARTs, 2 SSPs, 1 I^2C, 3 timers 1 PWM timer, 72 I/Os 15 Wake-up lines, 16 A/D Channels	
USB/CAN peripherals	None	USB	CAN	None	USB+CAN
Operating Voltage	3.3V or 5V	3.3V	3.3V or 5V		
Packages (**x**)	**T**=LQFP64 10x10, **H**=LFBGA64			**T**=LQFP100 14x14, **H**=LFBGA100	

GPIOs (general purpose input/output)

Each of the 72 GPIO pins (38 GPIOs in 64-pin devices) can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as Peripheral Alternate Function. Port 1.15 is an exception, it can be used as general-purpose input only or wake-up from STANDBY mode (WKP_STDBY). Most of the GPIO pins are shared with digital or analog alternate functions.

3.2 Block diagram

Figure 1. STR750 block diagram



AF: alternate function on I/O port pin

Note: I/Os shown for 100 pin devices. 64-pin devices have the I/O set shown in *Figure 3*.

4.1 Pin description table

Legend / abbreviations for *Table 6*:

Type:	I = input, O = output, S = supply,
Input levels:	All Inputs are LVTTL at V_{DD_IO} = 3.3V+/-0.3V or TTL at V_{DD_IO} = 5V± 0.5V. In both cases, T_T means V_{ILmax} =0.8V V_{IHmin}=2.0V
Inputs:	All inputs can be configured as floating or with internal weak pull-up or pull down (pu/pd)
Outputs:	All Outputs can be configured as Open Drain (OD) or Push-Pull (PP) (see also note 6 below *Table 6*). There are 3 different types of Output with different drives and speed characteristics: – O8: f_{max} = 40 MHz on C_L=50pF and 8 mA static drive capability for V_{OL}=0.4V and up to 20 mA for V_{OL}=1.3V (see*Output driving current on page 55*) – O4: f_{max} = 20 MHz on C_L=50pF and 4 mA static drive capability for V_{OL}=0.4V (see*Output driving current on page 55*) – O2: f_{max} = 10 MHz on C_L=50pF and 2 mA static drive capability of for V_{OL}=0.4V (see*Output driving current on page 55*)
External interrupts/wake-up lines:	EITx

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
7	D1	5	D1	P0.29 / TIM1_TI1 / ADC_IN8	I/O	T_T	**X**	X		O2	X	X		**Port 0.29**	TIM1: Input Capture 1	ADC: Analog input 8
8	E1	6	D2	P0.28 / TIM1_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 0.28**	TIM1: Output Compare 1	
9	E5	7	D3	TEST	I									Reserved, must be tied to ground		
10	E4	8	D4	VSS_IO	S									Ground Voltage for digital I/Os		
11	E2			P0.23 / UART1_RTS / ADC_IN6	I/O	T_T	**X**	X		O2	X	X		**Port 0.23**	UART1: Ready To Send output(4)	ADC analog input 6
12	F5			P2.04 / TIM2_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 2.04**	TIM2: Output Compare 1(4)	
13	F1			P2.03 / UART1_RTS	I/O	T_T	**X**	X		O2	X	X		**Port 2.03**	UART1: Ready To Send output(4)	
14	F4			P2.02	I/O	T_T	**X**	X		O2	X	X		**Port 2.02**		
15	E3			P0.22 / UART1_CTS / ADC_IN5	I/O	T_T	**X**	X		O2	X	X		**Port 0.22**	UART1: Clear To Send input	ADC: Analog input 5
16	F2	9	E4	P0.21 / UART1_TX	I/O	T_T	**X**	X		O2	X	X		**Port 0.21**	UART1: Transmit data output (remappable to P0.15)(4)	
17	F3	10	E3	P0.20 / UART1_RX	I/O	T_T	**X**	X		O2	X	X		**Port 0.20**	UART1: Receive data input (remappable to P0.14)(4)	
18	G3	11	E2	P1.19 / JTMS	I/O	T_T	X	X		O2	X	X		**JTAG mode selection input(6)**	Port 1.19	
19	G2	12	E1	P1.18 / JTCK	I/O	T_T	X	X		O2	X	X		**JTAG clock input(6)**	Port 1.18	
20	H3	13	F4	P1.17 / JTDO	I/O	T_T	X	X		O8	X	X		**JTAG data output(6)**	Port 1.17	
21	H2	14	F3	P1.16 / JTDI	I/O	T_T	X	X		O2	X	X		**JTAG data input(6)**	Port 1.16	
22	G1	15	F2	NJTRST	I	T_T								JTAG reset input(5)		
23	G4			P2.01	I/O	T_T	**X**	X		O2	X	X		**Port 2.01**		
24	G5			P2.00	I/O	T_T	**X**	X		O2	X	X		**Port 2.00**		
25	H1	16	F1	P0.13 / RTCK / UART0_RTS UART2_TX	I/O	T_T	X	X		O8	X	X		**JTAG return clock output(6)**	Port 0.13 / UART0: Ready To Send output(4)	UART2: Transmit Data output (when remapped)(8)

Table 6. STR750F pin description (continued)

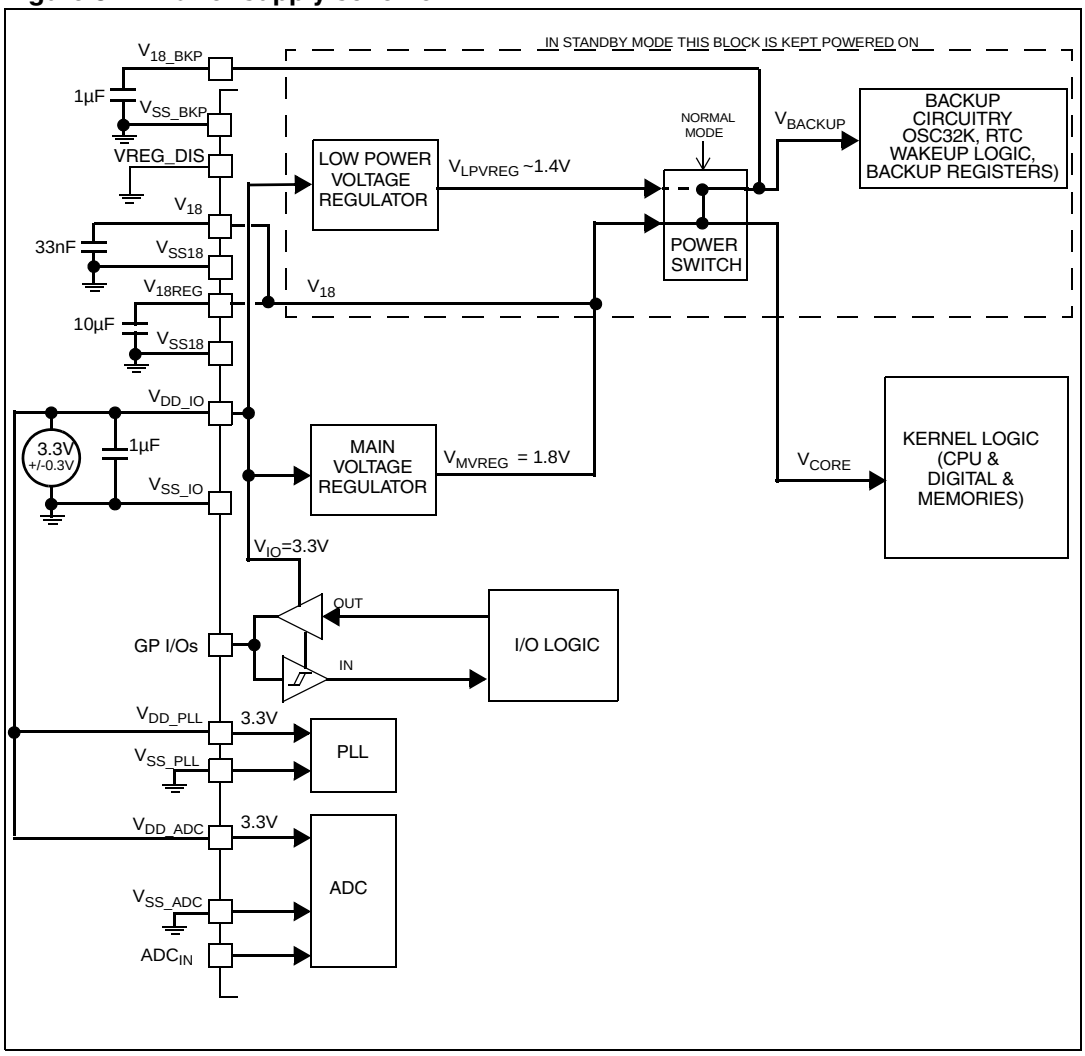
Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
26	J2	17	G2	P0.12 / UART2_RX / UART0_CTS / ADC_IN2 / SMI_CS1	I/O	T_T	X	X		O4	X	X		**Port 0.12**	UART0: Clear To Send input	ADC: Analog input 2
															Serial Memory Interface: chip select output 1	UART2: Receive Data input (when remapped)(8)
27	J1	18	G1	P0.11 / UART0_TX / BOOT1 / SMI_CS2	I/O	T_T	X	X		O4	X	X		**Port 0.11/Boot mode selection input 1**	UART0: Transmit data output	Serial Memory Interface: chip select output 2
28	K1	19	H1	P0.10 / UART0_RX / SMI_CS3	I/O	T_T	X	X	EIT4	O2	X	X		**Port 0.10**	UART0: Receive Data input	Serial Memory Interface: chip select output 3
29	K2	20	H2	P0.09 / I2C_SDA	I/O	T_T	X	X		O4	X	X		**Port 0.09**	I2C: Serial Data	
30	K3	21	H3	P0.08 / I2C_SCL	I/O	T_T	X	X	EIT3	O4	X	X		**Port 0.08**	I2C: Serial clock	
31	H4			P2.19	I/O	T_T	X	X		O2	X	X		**Port 2.19**		
32	H5			P2.18	I/O	T_T	X	X		O2	X	X		**Port 2.18**		
33	H6			P2.17 / UART2_RTS	I/O	T_T	X	X		O2	X	X		**Port 2.17**	UART2: Ready To Send output(4)	
34	J3	22	G3	P1.11 /UART0_RTS ADC_IN12	I/O	T_T	X	X	EIT11	O8	X	X		**Port 1.11**	UART0: Ready To Send output(4)	ADC: Analog input 12
35	J4			P0.27 / UART2_RTS / ADC_IN7	I/O	T_T	X	X		O2	X	X		**Port 0.27**	UART2: Ready To Send output(8)	ADC: Analog input 7
36	J6			P0.26 / UART2_CTS	I/O	T_T	X	X		O2	X	X		**Port 0.26**	UART2: Clear To Send input	
37	J7			P0.25 / UART2_TX	I/O	T_T	X	X		O2	X	X		**Port 0.25**	UART2: Transmit data output (remappable to P0.13)(8)	
38	H7			P0.24 / UART2_RX	I/O	T_T	X	X		O2	X	X		**Port 0.24**	UART2: Receive data input (remappable to P0.12)(8)	
39	J5	23	G4	P0.19 / USB_CK / SSP1_NSS / ADC_IN4	I/O	T_T	X	X	EIT6	O2	X	X		**Port 0.19**	SSP1: Slave select input (remappable to P0.11)(8)	ADC: Analog input 4
															USB: 48 MHz Clock input	
40	K4	24	H5	P0.18 / SSP1_MOSI	I/O	T_T	X	X		O2	X	X		**Port 0.18**	SSP1: Master out/slave in data (remappable to P0.10)(8)	
41	K5	25	H4	P0.17 / SSP1_MISO / ADC_IN3	I/O	T_T	X	X		O2	X	X		**Port 0.17**	SSP1: Master in/slave out data (remappable to P0.09)(8)	ADC: Analog input 3
42	K6	26	H6	P0.16 / SSP1_SCLK	I/O	T_T	X	X		O2	X	X		**Port 0.16**	SSP1: serial clock (remappable to P0.08)(8)	

6.1.6 Power supply schemes

When mentioned, some electrical parameters can refer to a dedicated power scheme among the four possibilities. The four different power schemes are described below.

Power supply scheme 1: Single external 3.3 V power source

Figure 8. Power supply scheme 1



6.3.4 Supply current characteristics

The current consumption is measured as described in *Figure 12 on page 30* and *Figure 13 on page 30*.

Subject to general operating conditions for V_{DD_IO}, and T_A

Maximum power consumption

For the measurements in *Table 13* and *Table 14*, the MCU is placed under the following conditions:

- All I/O pins are configured in output push-pull 0
- All peripherals are disabled except if explicitly mentioned.
- Embedded Regulators are used to provide 1.8 V (except if explicitly mentioned).

Table 13. Maximum power consumption in RUN and WFI modes

Symbol	Parameter	Conditions (1)		Typ (2)	Max (3)	Unit
I_{DD}	Supply current in RUN mode	External Clock with PLL multiplication, code running from RAM, all peripherals enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz Single supply scheme see *Figure 12* / *Figure 14*	3.3V and 5V range	80	90	mA
	Supply current in WFI mode	External Clock, code running from RAM: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz Single supply scheme see *Figure 12*./ *Figure 14* Parameter setting BURST=1, WFI_FLASHEN=1	3.3V and 5V range	62	67	mA

1. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4*.
2. Typical data are based on T_A=25°C, V_{DD_IO}=3.3V or 5.0V and V_{18}=1.8V unless otherwise specified.
3. Data based on product characterisation, tested in production at V_{DD_IO} max and V_{18} max (1.95V in dual supply mode or regulator output value in single supply mode) and T_A max.

6.3.5 Clock and timing characteristics

XT1 external clock source

Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 20. XT1 external clock source

Symbol	Parameter	Conditions(1) (2)	Min	Typ	Max	Unit
f_{XT1}	External clock source frequency	see *Figure 20*		4	60	MHz
V_{XT1H}	XT1 input pin high level voltage		$0.7xV_{DD\_IO}$		V_{DD_IO}	V
V_{XT1L}	XT1 input pin low level voltage		V_{SS}		$0.3xV_{DD\_IO}$	
$t_{w(XT1H)}$ $t_{w(XT1L)}$	XT1 high or low time (3)		6			ns
$t_{r(XT1)}$ $t_{f(XT1)}$	XT1 rise or fall time (3)				20	
I_L	XTx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD\_IO}$			±1	µA
$C_{IN(XT1)}$	XT1 input capacitance(3)			5		pF
$DuCy_{(XT1)}$	Duty cycle		45		55	%

1. Data based on typical application software.
2. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.
3. Data based on design simulation and/or technology characteristics, not tested in production.

XRTC1 external clock source

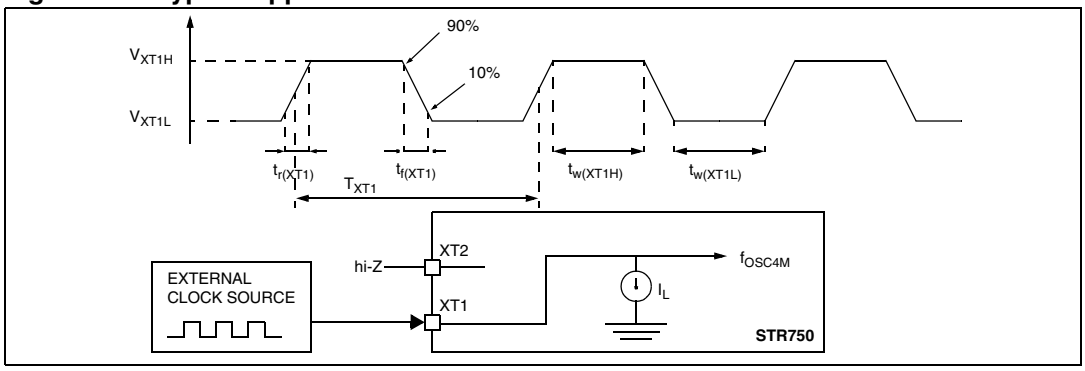
Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 21. XRTC1 external clock source

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
f_{XRTC1}	External clock source frequency	see *Figure 20*		32.768	500	kHz
V_{XRTC1H}	XRTC1 input pin high level voltage		$0.7xV_{DD\_IO}$		V_{DD_IO}	V
V_{XRTC1L}	XRTC1 input pin low level voltage		V_{SS}		$0.3xV_{DD\_IO}$	
$t_{w(XRTC1H)}$ $t_{w(XRTC1L)}$	XRTC1 high or low time(2)		900			ns
$t_{r(XRTC1)}$ $t_{f(XRTC1)}$	XRTC1 rise or fall time(2)				50	
I_L	XRTCx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD\_IO}$			±1	µA
$C_{IN(RTC1)}$	XRTC1 input capacitance(2)			5		pF
$DuCy_{(RTC1)}$	Duty cycle		30		70	%

1. Data based on typical application software.
2. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 20. Typical application with an external clock source



difference between N+1 consecutive clock rising edges and T_{min} is the minimum time difference between N+1 consecutive clock rising edges.

N should be kept sufficiently large to have a long term jitter (ex: thousands).

For N=1, this becomes the single period jitter.

See *Figure 23*

- Cycle-to-cycle jitter (N period jitter)

  This corresponds to the time variation between adjacent cycles over a random sample of adjacent clock cycles pairs. Jitter(cycle-to-cycle) = Max(Tcycle n- Tcycle n-1) for n=1 to N.

  See *Figure 24*

Figure 23. Self-referred jitter (single and long term)

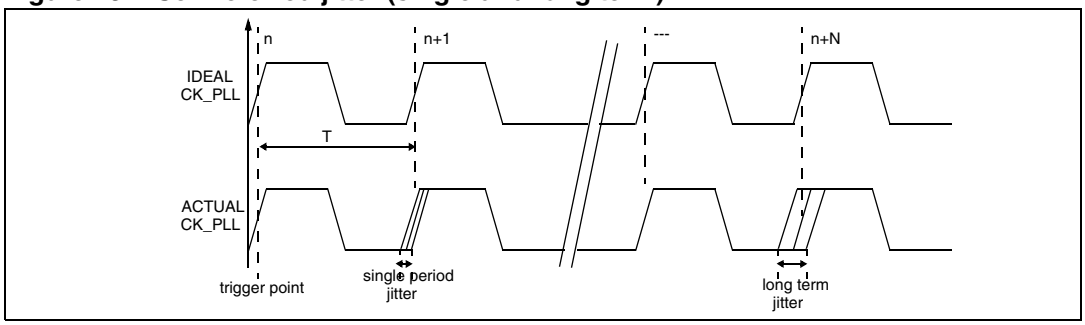
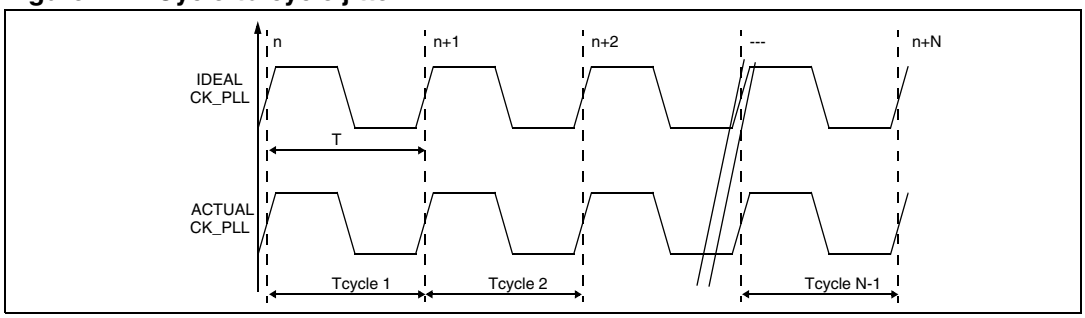


Figure 24. Cycle-to-cycle jitter



6.3.6 Memory characteristics

Flash memory

Subject to general operating conditions for V_{DD_IO} and V_{18}, T_A = -40 to 105 °C unless otherwise specified.

Table 26. Flash memory characteristics

Symbol	Parameter	Test Conditions	Value		Unit
			Typ	Max(1)	
t_{PW}	Word Program		35		µs
t_{PDW}	Double Word Program		60		µs
t_{PB0}	Bank 0 Program (256K)	Single Word programming of a checker-board pattern	2	4.9(2)	s
t_{PB1}	Bank 1 Program (16K)	Single Word programming of a checker-board pattern	125	224(2)	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed (all 1) Preprogrammed (all 0)	1.54 1.176	2.94(2) 2.38(2)	s
t_{ES}	Sector Erase (8K)	Not preprogrammed (all 1) Preprogrammed (all 0)	392 343	560(2) 532(2)	ms
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed (all 1) Preprogrammed (all 0)	8.0 6.6	13.7 11.2	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed (all 1) Preprogrammed (all 0)	0.9 0.8	1.5 1.3	s
t_{RPD}	Recovery when disabled			20	µs
t_{PSL}	Program Suspend Latency			10	µs
t_{ESL}	Erase Suspend Latency			300	µs

1. Data based on characterisation not tested in production
2. 10K program/erase cycles.

Table 27. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END_B0}	Endurance (Bank 0 sectors)		10			kcycles
N_{END_B1}	Endurance (Bank 1 sectors)		100			kcycles
Y_{RET}	Data Retention	T_A=85° C	20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

1. Data based on characterisation not tested in production.

Electro magnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 29. EMI characteristics

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f_{OSC4M}/f_{HCLK}]		Unit
				4/32MHz	4/60MHz	
S_{EMI}	Peak level	Flash devices: V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, LQFP64 package conforming to SAE J 1752/3	0.1 MHz to 30 MHz	22	26	dBµV
			30 MHz to 130 MHz	31	26	
			130 MHz to 1 GHz	19	23	
			SAE EMI Level	>4	>4	-

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electro-Static discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard.

Table 30. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25° C	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)		200	
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charge Device Model)		750	

1. Data based on product characterisation, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 31. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A=+25° C T_A=+85° C T_A=+105° C	Class A
DLU	Dynamic latch-up class	V_{DD}= 5.5 V, f_{OSC4M}=4 MHz, f_{CK_SYS}=32 MHz, T_A=+25° C	Class A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

Table 37. PWM Timer (PWM)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(PWM)}$	PWM resolution time	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
		$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	16.6(1)			ns
Res_{PWM}	PWM resolution				16	bit
V_{OS}(1)	PWM/DAC output step voltage	V_{DD_IO}=3.3 V, Res=16-bits		50(1)		µV
		V_{DD_IO}=5.0 V, Res=16-bits		76(1)		µV
$t_{COUNTER}$	Timer clock period when internal clock is selected		1		65536	t_{CK_TIM}
		f_{CK_TIM}=60 MHz	0.0166		1087	µs
t_{MAX_COUNT}	Maximum Possible Count				65536x 65536	t_{CK_TIM}
		$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s

1. Take into account the frequency limitation due to the I/O speed capability when outputting the PWM to an I/O pin, as described in *: Output speed on page 57*.

6.3.10 Communication interface characteristics

SSP synchronous serial peripheral in master mode (SPI or TI mode)

General operating conditions: V_{33}, 3.0V to 3.3V, V18 =1.8V, $C_L \approx 45$ pF.

Table 38. SSP master mode characteristics(1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK}	SPI clock frequency(2)		SSP0		16	MHz
			SSP1		8	
$t_{r(SCK)}$	SPI clock rise time		SSP0		14	ns
			SSP1		33	
$t_{f(SCK)}$	SPI clock fall time		SSP0		11	
			SSP1		30	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time		SSP0		19	
			SSP1		30	
t_{NSSLQV}	NSS low to Data Output MOSI valid time		SSP0		$0.5t_{SCK}$+15ns	
			SSP1		$0.5t_{SCK}$+30ns	
$t_{SCKNSSH}$	SCK last edge to NSS high	CPHA = 0	SSP0		$0.5t_{SCK}$+15ns	
			SSP1		$0.5t_{SCK}$+30ns	
		CPHA = 1	SSP0		t_{SCK}+15ns	
			SSP1		t_{SCK}+30ns	
t_{SCKQV}	SCK trigger edge to data output MOSI valid time		SSP0		15	
			SSP1		30	
t_{SCKQX}	SCK trigger edge to data output MOSI invalid time		SSP0	0		
			SSP1	0		
t_{su}	Data input (MISO) setup time w.r.t SCK sampling edge		SSP0	25		
			SSP1	25		
t_h	Data input (MISO) hold time w.r.t SCK sampling edge		SSP0	0		
			SSP1	0		

1. Data based on characterisation results, not tested in production.
2. Max frequency for the 2 SSPs is $f_{PCLK}/2$; f_{PCLK} max = 32 MHz. This takes into account the frequency limitation due to I/O speed capability. SSP0 uses IO4 type while SSP1 uses IO2 type I/Os.

SSP synchronous serial peripheral in slave mode (SPI or TI mode)

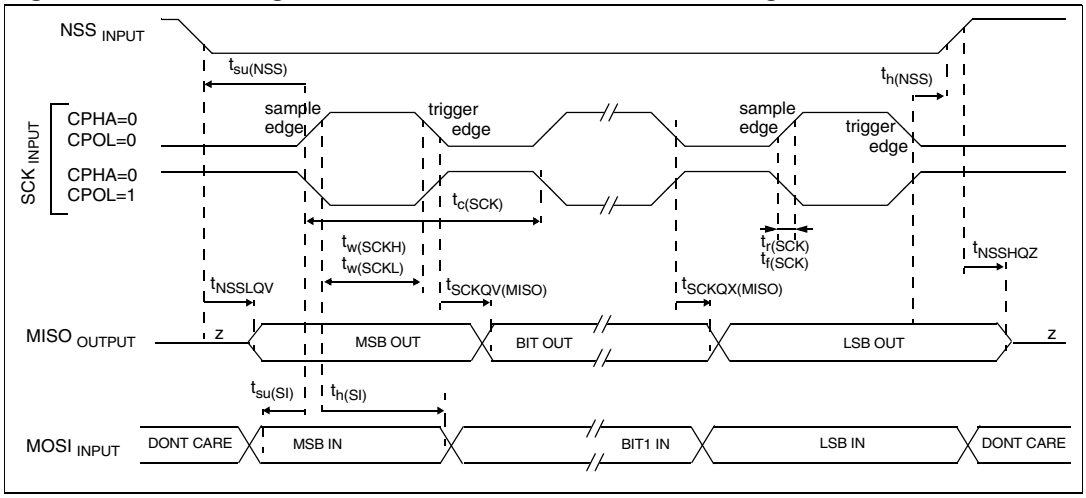
Subject to general operating conditions with $C_L \approx 45$ pF

Table 39. SSP slave mode characteristics(1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK}	SPI clock frequency		SSP0		2.66 MHz (f_{PLCK}/12)	MHz
			SSP1			
$t_{su(NSS)}$	NSS input setup time w.r.t SCK first edge		SSP0	0		ns
			SSP1	0		
$t_{h(NSS)}$	NSS input hold time w.r.t SCK last edge		SSP0	t_{PCLK}+15ns		
			SSP1	t_{PCLK}+15ns		
t_{NSSLQV}	NSS low to Data Output MISO valid time		SSP0	$2t_{PCLK}$	$3t_{PCLK}$+30 ns	
			SSP1	$2t_{PCLK}$	$3t_{PCLK}$+30 ns	
t_{NSSLQZ}	NSS low to Data Output MISO invalid time		SSP0	$2t_{PCLK}$	$3t_{PCLK}$+15 ns	
			SSP1	$2t_{PCLK}$	$3t_{PCLK}$+15 ns	
t_{SCKQV}	SCK trigger edge to data output MISO valid time		SSP0		15	
			SSP1		30	
t_{SCKQX}	SCK trigger edge to data output MISO invalid time		SSP0	$2t_{PCLK}$		
			SSP1	$2t_{PCLK}$		
$t_{su(MOSI)}$	MOSI setup time w.r.t SCK sampling edge		SSP0	0		
			SSP1	0		
$t_{h(MOSI)}$	MOSI hold time w.r.t SCK sampling edge		SSP0	$3t_{PCLK}$+15 ns		
			SSP1	$3t_{PCLK}$+15 ns		

1. Data based on characterisation results, not tested in production.

Figure 33. SPI configuration, slave mode with CPHA=0, single transfer



6.3.11 USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 42. USB startup time

Symbol	Parameter	Conditions	Max	Unit
$t_{STARTUP}$	USB transceiver startup time		1	µs

Table 43. USB characteristics

USB DC Electrical Characteristics					
Symbol	**Parameter**	**Conditions**	**Min.(1)(2)**	**Max.(1)(2)**	**Unit**
Input Levels					
V_{DI}	Differential Input Sensitivity	I(DP, DM)	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	
V_{SE}	Single Ended Receiver Threshold		1.3	2.0	
Output Levels					
V_{OL}	Static Output Level Low	R_L of 1.5 kΩ to 3.6V(3)		0.3	V
V_{OH}	Static Output Level High	R_L of 15 kΩ to V_{SS}(3)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. It is important to be aware that the DP/DM pins are not 5 V tolerant. As a consequence, in case of a a shortcut with Vbus (typ: 5.0V), the protection diodes of the DP/DM pins will be direct biased . This will not damage the device if not more than 50 mA is sunk for longer than 24 hours but the reliability may be affected.
3. R_L is the load connected on the USB drivers

Figure 41. USB: data signal rise and fall time

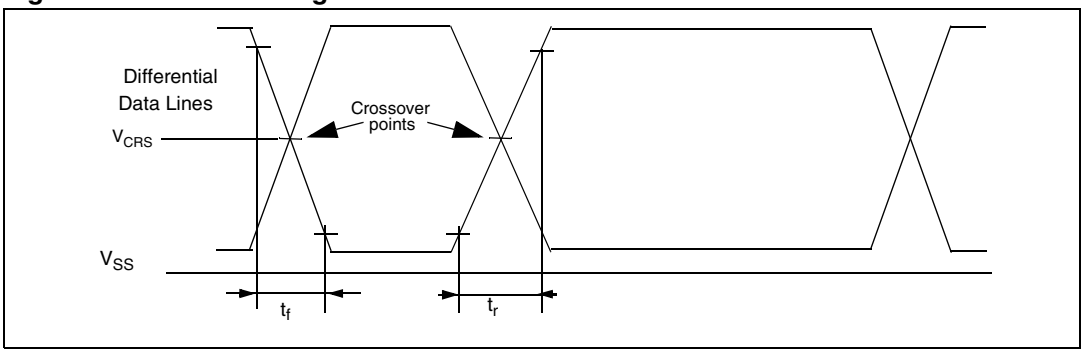


Table 44. USB: Full speed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Driver characteristics:					
t_r	Rise time(1)	C_L=50 pF	4	20	ns
t_f	Fall Time1)	C_L=50 pF	4	20	ns

7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code *Table 49: Order codes on page 81*.

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax}= 82 °C (measured according to JESD51-2), I_{DDmax}=8 mA, V_{DD} = 5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

$$P_{INTmax} = 8 \text{ mA} \times 5 \text{ V} = 400 \text{ mW}$$

$$P_{IOmax} = 20 \times 8 \text{ mA} \times 0.4\text{V} = 64 \text{ mW}$$

This gives: P_{INTmax}= 400 mW and P_{IOmax} 64 mW:

$$P_{Dmax} = 400 \text{ mW} + 64 \text{ mW}$$

Thus: P_{Dmax} = 464 mW

Using the values obtained in *Table 48* T_{Jmax} is calculated as follows:

– For LQFP100, 46°C/W

T_{Jmax} = 82° C + (46° C/W x 464 mW) = 82°C + 21°C = 103° C

This is within the range of the suffix 6 version parts (-40 < T_J < 105° C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 49: Order codes on page 81*).

– For BGA64, 58°C/W

T_{Jmax} = 82° C + (58° C/W x 464 mW) = 82°C + 27°C = 109° C

This is within the range of the suffix 7 version parts (-40 < T_J < 125° C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 49: Order codes on page 81*).

Figure 50. LQFP100 P_{Dmax} vs T_A