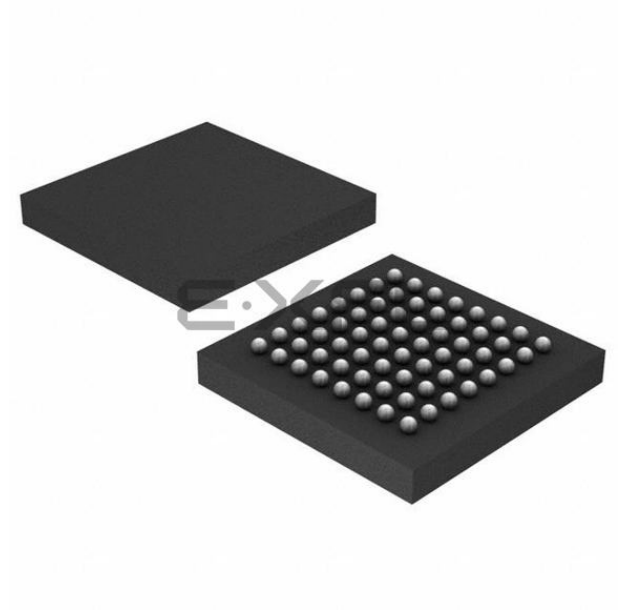

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

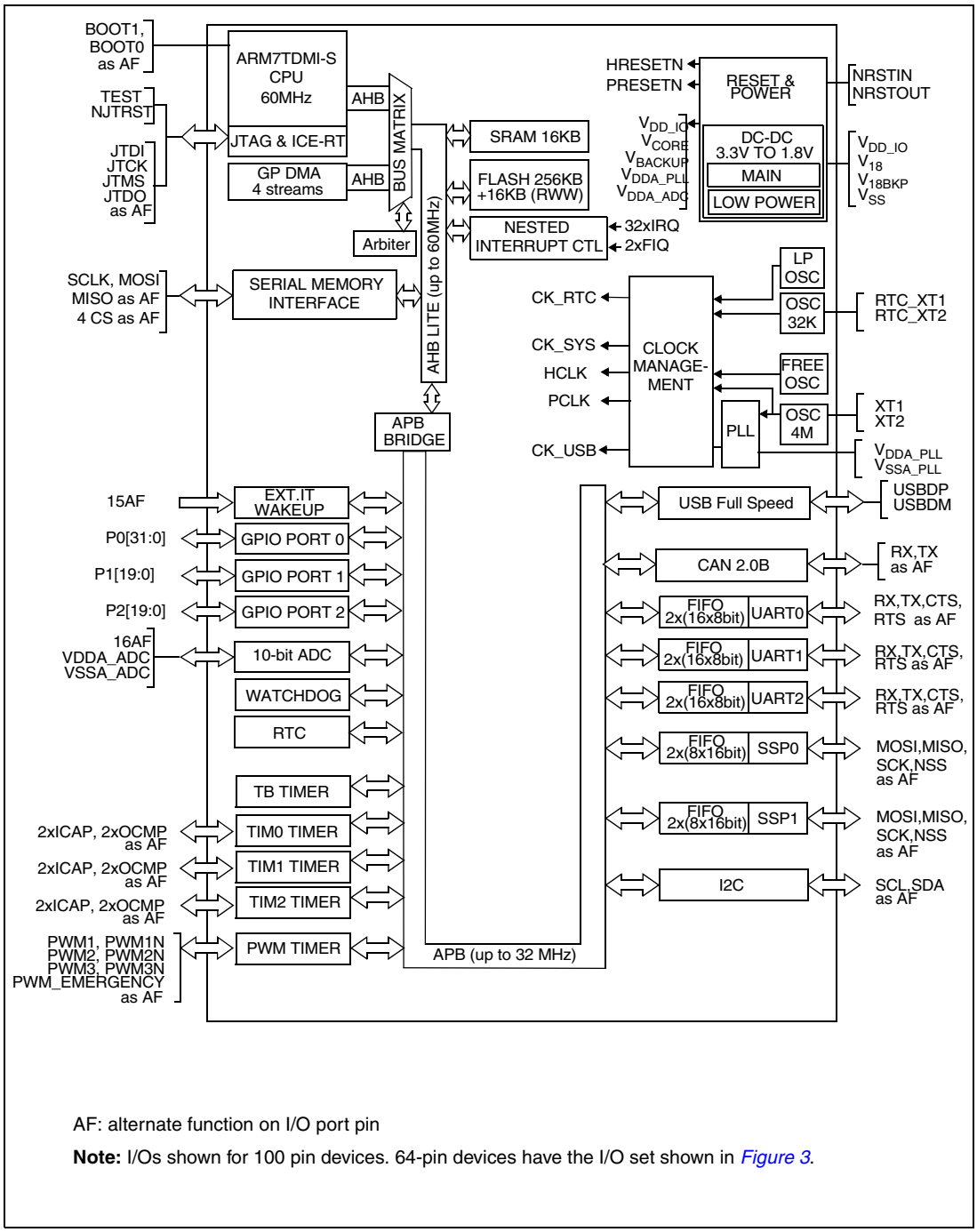
Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, SPI, SSI, SSP, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str755fr2h6

GPIOs (general purpose input/output)

Each of the 72 GPIO pins (38 GPIOs in 64-pin devices) can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as Peripheral Alternate Function. Port 1.15 is an exception, it can be used as general-purpose input only or wake-up from STANDBY mode (WKP_STDBY). Most of the GPIO pins are shared with digital or analog alternate functions.

3.2 Block diagram

Figure 1. STR750 block diagram



AF: alternate function on I/O port pin

Note: I/Os shown for 100 pin devices. 64-pin devices have the I/O set shown in *Figure 3*.

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
26	J2	17	G2	P0.12 / UART2_RX / UART0_CTS / ADC_IN2 / SMI_CS1	I/O	T_T	X	X		O4	X	X		**Port 0.12**	UART0: Clear To Send input	ADC: Analog input 2
															Serial Memory Interface: chip select output 1	UART2: Receive Data input (when remapped)(8)
27	J1	18	G1	P0.11 / UART0_TX / BOOT1 / SMI_CS2	I/O	T_T	X	X		O4	X	X		**Port 0.11/Boot mode selection input 1**	UART0: Transmit data output	Serial Memory Interface: chip select output 2
28	K1	19	H1	P0.10 / UART0_RX / SMI_CS3	I/O	T_T	X	X	EIT4	O2	X	X		**Port 0.10**	UART0: Receive Data input	Serial Memory Interface: chip select output 3
29	K2	20	H2	P0.09 / I2C_SDA	I/O	T_T	X	X		O4	X	X		**Port 0.09**	I2C: Serial Data	
30	K3	21	H3	P0.08 / I2C_SCL	I/O	T_T	X	X	EIT3	O4	X	X		**Port 0.08**	I2C: Serial clock	
31	H4			P2.19	I/O	T_T	X	X		O2	X	X		**Port 2.19**		
32	H5			P2.18	I/O	T_T	X	X		O2	X	X		**Port 2.18**		
33	H6			P2.17 / UART2_RTS	I/O	T_T	X	X		O2	X	X		**Port 2.17**	UART2: Ready To Send output(4)	
34	J3	22	G3	P1.11 /UART0_RTS ADC_IN12	I/O	T_T	X	X	EIT11	O8	X	X		**Port 1.11**	UART0: Ready To Send output(4)	ADC: Analog input 12
35	J4			P0.27 / UART2_RTS / ADC_IN7	I/O	T_T	X	X		O2	X	X		**Port 0.27**	UART2: Ready To Send output(8)	ADC: Analog input 7
36	J6			P0.26 / UART2_CTS	I/O	T_T	X	X		O2	X	X		**Port 0.26**	UART2: Clear To Send input	
37	J7			P0.25 / UART2_TX	I/O	T_T	X	X		O2	X	X		**Port 0.25**	UART2: Transmit data output (remappable to P0.13)(8)	
38	H7			P0.24 / UART2_RX	I/O	T_T	X	X		O2	X	X		**Port 0.24**	UART2: Receive data input (remappable to P0.12)(8)	
39	J5	23	G4	P0.19 / USB_CK / SSP1_NSS / ADC_IN4	I/O	T_T	X	X	EIT6	O2	X	X		**Port 0.19**	SSP1: Slave select input (remappable to P0.11)(8)	ADC: Analog input 4
															USB: 48 MHz Clock input	
40	K4	24	H5	P0.18 / SSP1_MOSI	I/O	T_T	X	X		O2	X	X		**Port 0.18**	SSP1: Master out/slave in data (remappable to P0.10)(8)	
41	K5	25	H4	P0.17 / SSP1_MISO / ADC_IN3	I/O	T_T	X	X		O2	X	X		**Port 0.17**	SSP1: Master in/slave out data (remappable to P0.09)(8)	ADC: Analog input 3
42	K6	26	H6	P0.16 / SSP1_SCLK	I/O	T_T	X	X		O2	X	X		**Port 0.16**	SSP1: serial clock (remappable to P0.08)(8)	

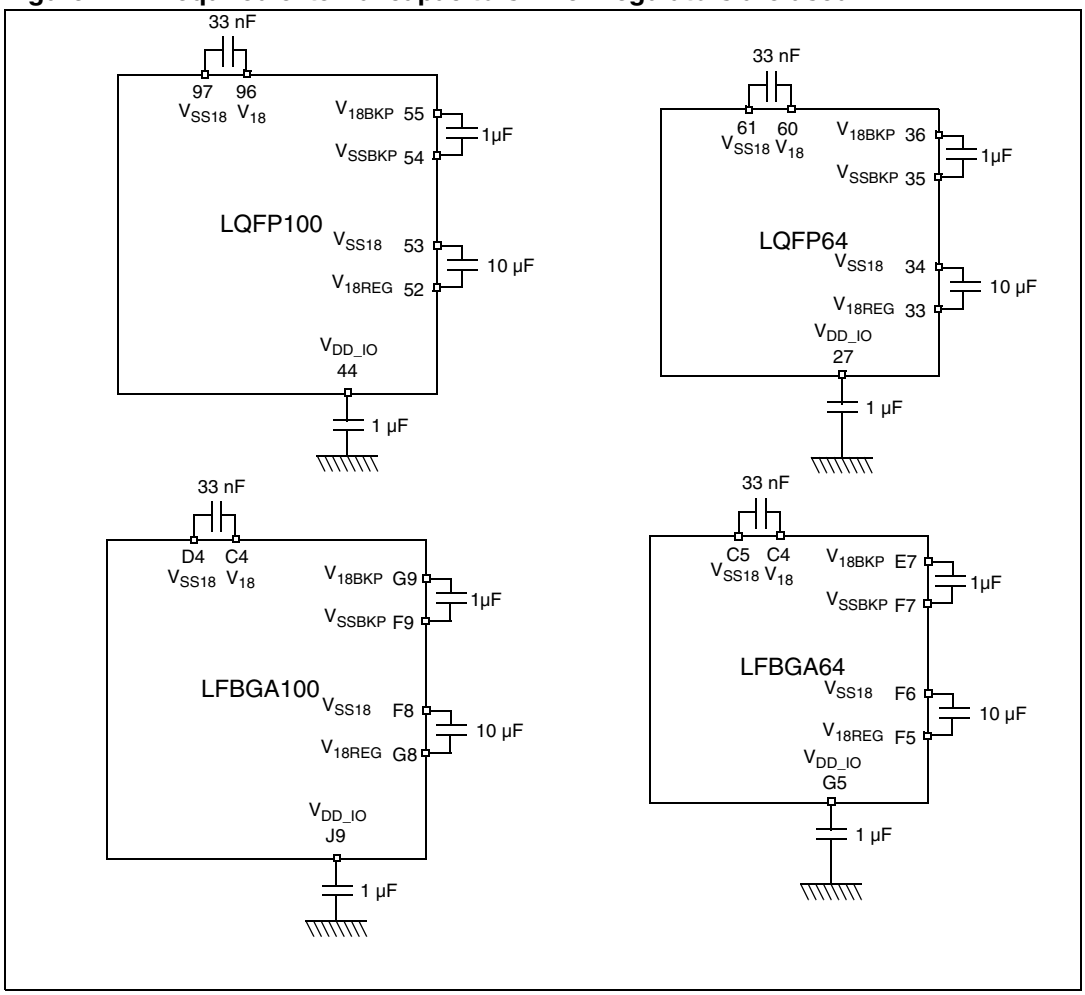
Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
91	A4	59	A3	P1.04 / PWM3N / ADC_IN9	I/O	T_T	**X**	X		O4	X	X		**Port 1.04**	PWM: PWM3 complementary output(4)	ADC: analog input 9
92	A3			P1.14 / ADC_IN15	I/O	T_T	**X**	X		O8	X	X		**Port 1.14**	ADC: analog input 15	
93	A2			P1.13 / ADC_IN14	I/O	T_T	**X**	X	EIT13	O8	X	X		**Port 1.13**	ADC: analog input 14	
94	D5			P1.01 / TIM0_TI2	I/O	T_T	**X**	X		O2	X	X		**Port 1.01**	TIM0: Input Capture / trigger / external clock 2 (remappable to P0.05)(8)	
95	E6			P1.00 / TIM0_OC2	I/O	T_T	**X**	X		O2	X	X		**Port 1.00**	TIM0: Output compare 2 (remappable to P0.04)(8)	
96	C4	60	C4	V18	S									Stabilization for main voltage regulator. Requires external capacitors 33nF between V18 and VSS18. See *Figure 4.2*. To be connected to the 1.8V external power supply when embedded regulators are not used.		
97	D4	61	C5	VSS18	S									Ground Voltage for the main voltage regulator.		
98	D3	62	A2	VSS_IO	S									Ground Voltage for digital I/Os		
99	C3	63	B2	VDD_IO	S									Supply Voltage for digital I/Os		
100	A1	64	A1	P0.03 / TIM2_TI1 / ADC_IN1	I/O	T_T	**X**	X		O2	X	X		**Port 0.03**	TIM2: Input Capture / trigger / external clock 1	ADC: analog input 1

1. For STR755FVx part numbers, the USB pins must be left unconnected.
2. The non available pins on LQPFP64 and LFBGA64 packages are internally tied to low level.
3. None of the I/Os are True Open Drain: when configured as Open Drain, there is always a protection diode between the I/O pin and VDD_IO.
4. In the 100-pin package, this Alternate Function is duplicated on two ports. You can configure one port to use this AF, the other port is then free for general purpose I/O (GPIO), external interrupt/wake-up lines, or analog input (ADC_IN) where these functions are listed in the table.
5. It is mandatory that the NJTRST pin is reset to ground during the power-up phase. It is recommended to connect this pin to NRSTOUT pin (if available) or NRSTIN.
6. After reset, these pins are enabled as JTAG alternate function see (*Port reset state on page 16*). To use these ports as general purpose I/O (GPIO), the DBGOFF control bit in the GPIO_REMAP0R register must be set by software (in this case, debugging these I/Os via JTAG is not possible).
7. There are two different TQFP and BGA 64-pin packages: in the first one, pins 41 and 42 are mapped to USB DN/DP while for the second one, they are mapped to P0.15/CAN_TX and P0.14/CAN_RX.
8. For details on remapping these alternate functions, refer to the GPIO_REMAP0R register description.

4.2 External components

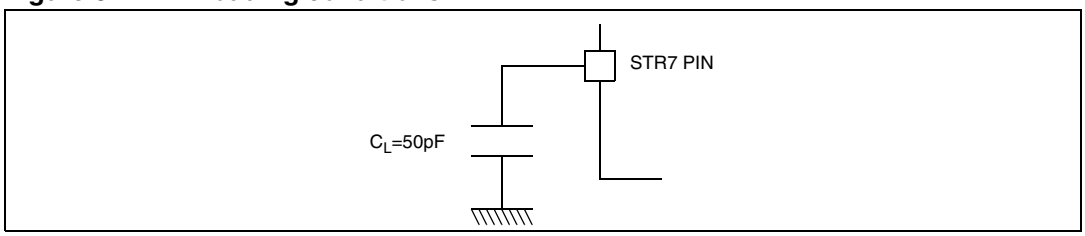
Figure 4. Required external capacitors when regulators are used



6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

Figure 6. Pin loading conditions



6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 7. Pin input voltage

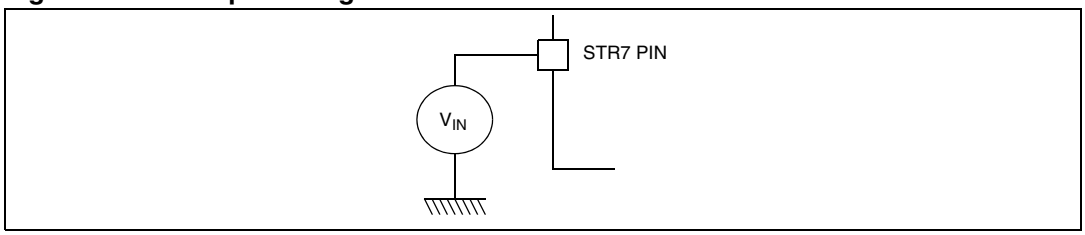


Figure 16. Power consumption in STOP mode in Single supply scheme (3.3 V range)

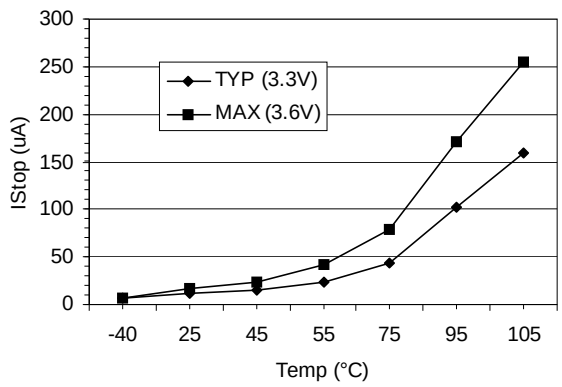


Figure 17. Power consumption in STOP mode Single supply scheme (5 V range)

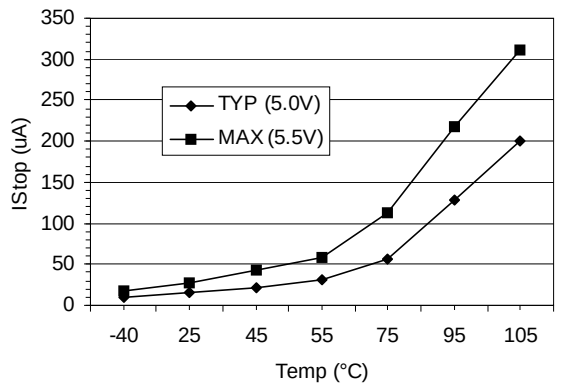


Figure 18. Power consumption in STANDBY mode (3.3 V range)

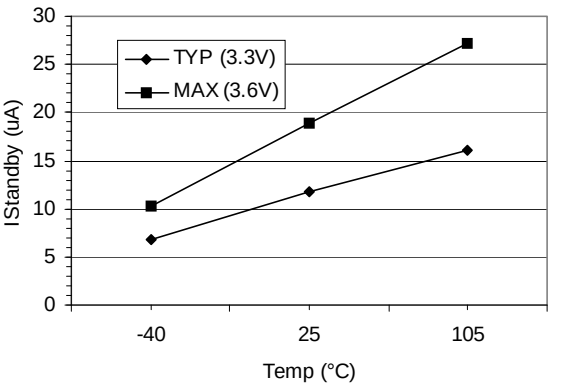
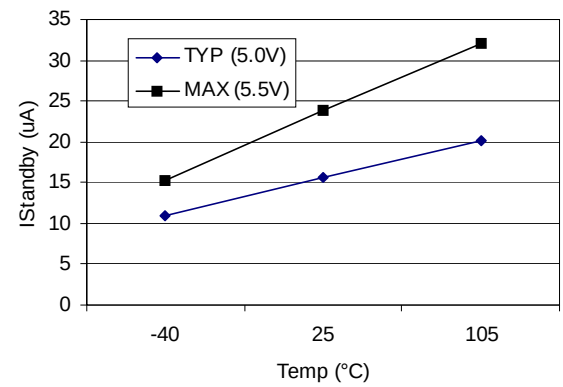


Figure 19. Power consumption in STANDBY mode (5 V range)



Typical power consumption

The following measurement conditions apply to *Table 15*, *Table 16* and *Table 17*.

In RUN mode:

- Program is executed from Flash (except if especially mentioned). The program consists of an infinite loop. When f_{HCLK} > 32 MHz, burst mode is activated.
- A standard 4 MHz crystal source is used.
- In all cases the PLL is used to multiply the frequency.
- All measurements are done in the single supply scheme with internal regulators used (see *Figure 12*)

In WFI Mode:

- In WFI Mode the measurement conditions are similar to RUN mode (OSC4M and PLL enabled). In addition, the Flash can be disabled depending on burst mode activation:
  - For AHB frequencies greater than 32 MHz, burst mode is activated and the Flash is kept enabled by setting the WFI_FLASH_EN bit (this bit cannot be reset when burst mode is activated).
  - For AHB frequencies less than or equal to 32 MHz, burst mode is deactivated, WFI_FLASH_EN is reset and the LP_PARAM14 bit is set (Flash is disabled in WFI mode).

In SLOW mode:

- The same program as in RUN mode is executed from Flash. The CPU is clocked by the FREEOSC, OSC4M, LPOSC or OSC32K. Only EXTIT peripheral is enabled in the MRCC_PCLKEN register.

In SLOW-WFI mode:

- In SLOW-WFI, the measurement conditions are similar to SLOW mode (CPU clocked by a low frequency clock). In addition, the LP_PARAM14 bit is set (FLASH is OFF). The WFI routine itself is executed from SRAM (it is not allowed to execute a WFI from the internal FLASH)

In STOP mode:

- Several measurements are given: in the single supply scheme with internal regulators used (see *Figure 12*): and in the dual supply scheme (see *Figure 13*).

In STANDBY mode:

- Three measurements are given:
  - The RTC is disabled, only the consumption of the LPVREG and RSM remain (almost no leakage currents)
  - The RTC is running, clocked by a standard 32.768 kHz crystal.
  - The RTC is running, clocked by the internal Low Power RC oscillator (LPOSC)
- STANDBY mode is only supported in the single supply scheme (see *Figure 12*)

Supply and clock manager power consumption

Table 18. Supply and clock manager power consumption

Symbol	Parameter	Conditions[1]	3.3V Typ	5V Typ	Unit
$I_{DD(OSC4M)}$	Supply current of resonator oscillator in STOP or WFI mode (LP_PARAM bit: OSC4M ON)	External components specified in: *4/8 MHz crystal / ceramic resonator oscillator (XT1/XT2) on page 46*	1815	1795	µA
$I_{DD(FLASH)}$	FLASH static current consumption in STOP or WFI mode (LP_PARAM bit FLASH ON)		515	515	
$I_{DD(MVREG)}$	Main Voltage Regulator static current consumption in STOP mode (LP_PARAM bit: MVREG ON)		130	135	
$I_{DD(LPVREG)}$	Low Power Voltage Regulator + RSM current static current consumption	STOP mode includes leakage where V_{18} is internally set to 1.4 V	12	15	
		STANDBY mode where V_{18BKP} and V_{18} are internally set to 1.4 V and 0 V respectively	11	14	

1. Measurements performed in 3.3V single supply mode see *Figure 12*

6.3.5 Clock and timing characteristics

XT1 external clock source

Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 20. XT1 external clock source

Symbol	Parameter	Conditions(1) (2)	Min	Typ	Max	Unit
f_{XT1}	External clock source frequency	see *Figure 20*		4	60	MHz
V_{XT1H}	XT1 input pin high level voltage		$0.7xV_{DD\_IO}$		V_{DD_IO}	V
V_{XT1L}	XT1 input pin low level voltage		V_{SS}		$0.3xV_{DD\_IO}$	
$t_{w(XT1H)}$ $t_{w(XT1L)}$	XT1 high or low time (3)		6			ns
$t_{r(XT1)}$ $t_{f(XT1)}$	XT1 rise or fall time (3)				20	
I_L	XTx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD\_IO}$			±1	µA
$C_{IN(XT1)}$	XT1 input capacitance(3)			5		pF
$DuCy_{(XT1)}$	Duty cycle		45		55	%

1. Data based on typical application software.
2. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.
3. Data based on design simulation and/or technology characteristics, not tested in production.

6.3.7 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electro magnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

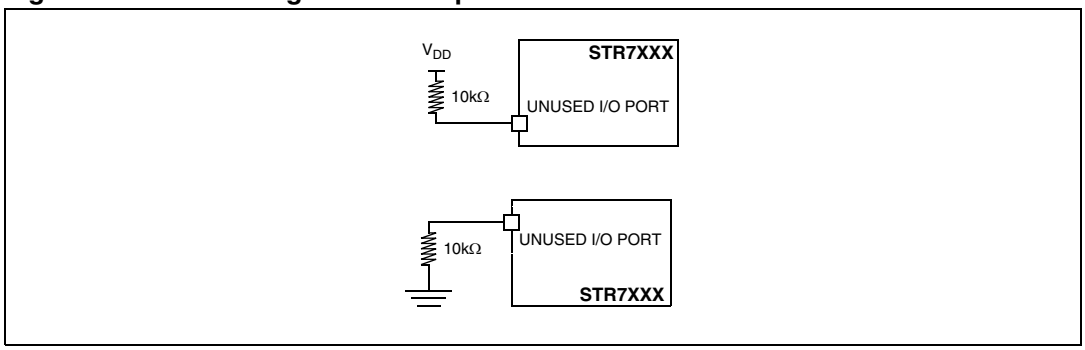
Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behaviour is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 28. EMC characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-2	Class A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-4	Class A

Figure 25. Connecting unused I/O pins



Output driving current

The GP I/Os have different drive capabilities:

- O2 outputs can sink or source up to +/-2 mA.
- O4 outputs can sink or source up to +/-4 mA.
- outputs can sink or source up to +/-8 mA or can sink +20 mA (with a relaxed V_{OL}).

In the application, the user must limit the number of I/O pins which can drive current to respect the absolute maximum rating specified in *Section 6.2.2* :

- The sum of the current sourced by all the I/Os on $V_{DD\_IO,}$ plus the maximum RUN consumption of the MCU sourced on $V_{DD\_IO,}$ can not exceed the absolute maximum rating IV_{DD_IO}.
- The sum of the current sunk by all the I/Os on V_{SS_IO} plus the maximum RUN consumption of the MCU sunk on V_{SS_IO} can not exceed the absolute maximum rating IV_{SS_IO}.

Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

6.3.9 TB and TIM timer characteristics

Subject to general operating conditions for V_{DD_IO}, f_{CK_SYS}, and T_A unless otherwise specified.

Refer to *Section 6.3.8: I/O port pin characteristics on page 54* for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

Table 36. TB and TIM timers

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time	TIM0,1,2		2			t_{CK_TIM}
$t_{res(TIM)}$	Timer resolution time(1)	TB	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	16.6(1)			ns
		TIM0,1,2	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60MHz	16.6(1)			ns
f_{EXT}	Timer external clock frequency on TI1 or TI2	TIM0,1,2	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	0		$f_{CK\_TIM}/4$	MHz
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0		15	MHz
Res_{TIM}	Timer resolution					16	bit
$t_{COUNTER}$	16-bit Counter clock period when internal clock is selected (16-bit Prescaler)	TB		1		65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0.0166		1092	µs
		TIM0,1,2		1		65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0.0166		1092	µs
t_{MAX_COUNT}	Maximum Possible Count	TB				65536x65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s
		TIM0,1,2				65536x65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s

1. Take into account the frequency limitation due to the I/O speed capability when outputting the PWM to I/O pin, described in *: Output speed on page 57*.

Figure 28. SPI configuration - master mode, single transfer

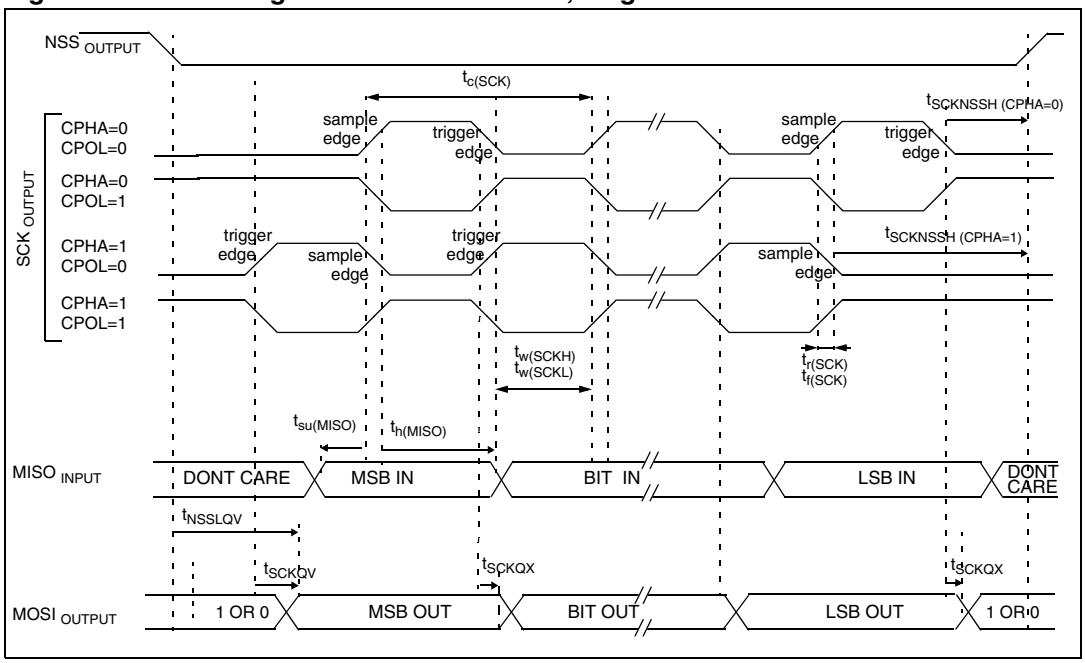


Figure 29. SPI configuration - master mode, continuous transfer, CPHA=0

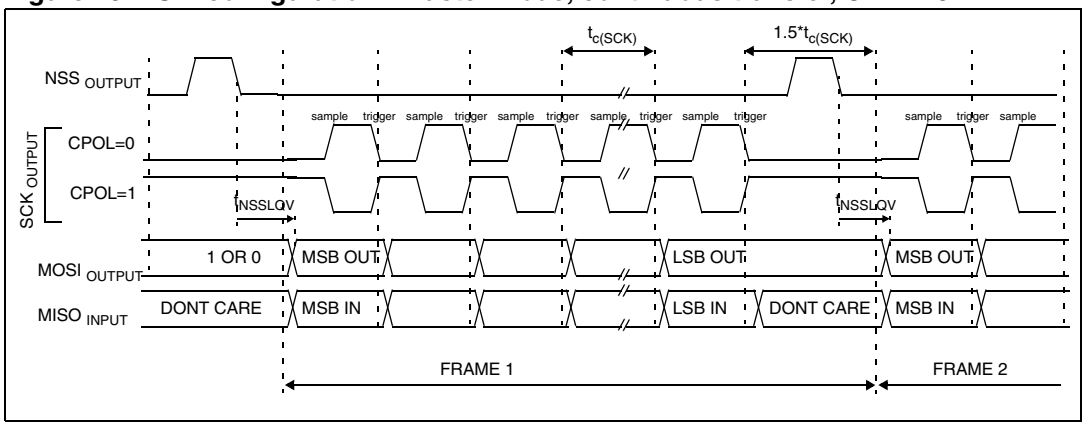
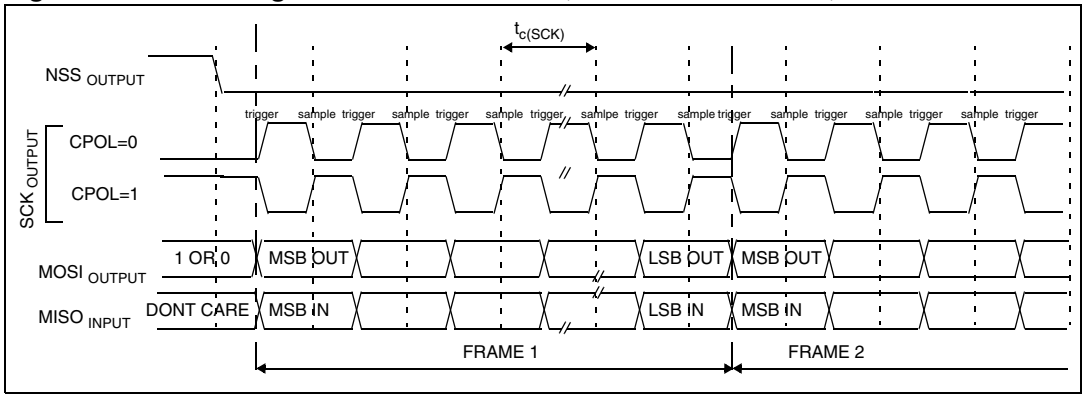


Figure 30. SPI configuration - master mode, continuous transfer, CPHA=1



not possible to power off the STR7x while some another I^2C master node remains powered on: otherwise, the STR7x will be powered by the protection diode.

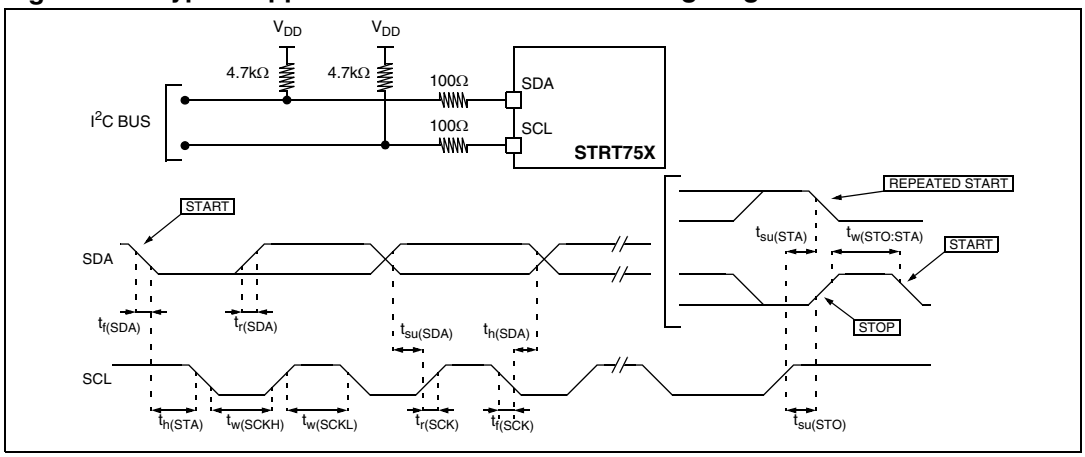
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 41. SDA and SCL characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20+0.1C_b	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20+0.1C_b	300	ns
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		µs
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. f_{PCLK}, must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
2. Data based on standard I^2C protocol requirement, not tested in production.
3. The maximum hold time $t_{h(SDA)}$ is not applicable
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 40. Typical application with I^2C bus and timing diagram



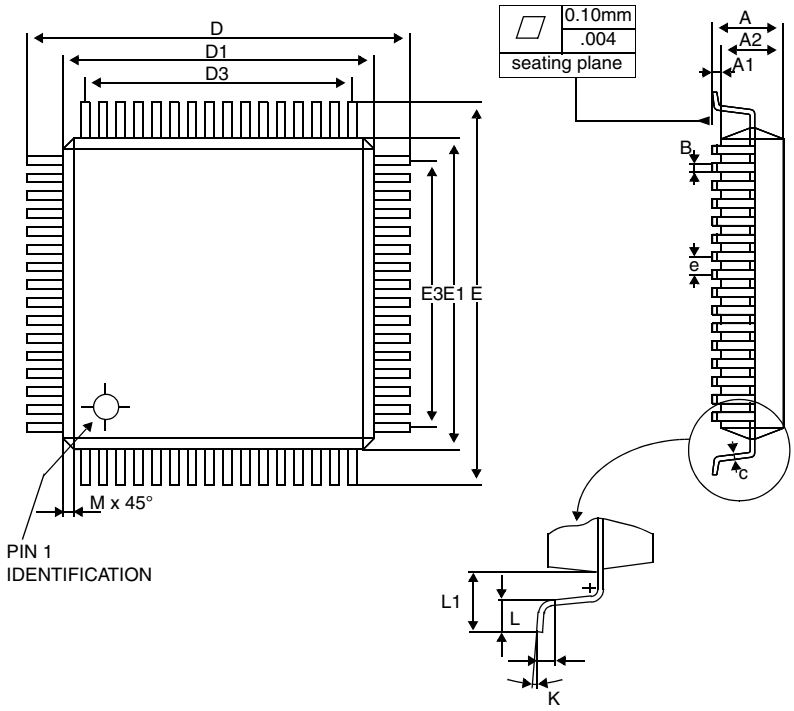
1. Measurement points are done at CMOS levels: 0.3xV_{DD} and 0.7xV_{DD}.

7 Package characteristics

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 Package mechanical data

Figure 45. 64-pin low profile quad flat package (10x10)



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of pins					
N	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 10: General operating conditions on page 34*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in ° C/W,
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$),
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum Power Dissipation on Output Pins.
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 48. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 100 - 14 x 14 mm / 0.5 mm pitch	46	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 100 - 10 x 10 x 1.7mm	41	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

9 Revision history

Table 50. Document revision history

Date	Revision	Description of Changes
25-Sep-2006	1	Initial release
30-Oct-2006	2	Added power consumption data for 5V operation in *Section 6*
04-Jul-2007	3	Changed datasheet title from STR750F to STR750FXX STR751Fxx STR752Fxx STR755xx. Added *Table 1: Device summary on page 1* Added note 1 to *Table 6* Added STOP mode IDD max. values in *Table 14* Updated XT2 driving current in *Table 23.* Updated RPD in *Table 32* Updated *Table 21: XRTC1 external clock source on page 45* Updated *Table 34: Output speed on page 57* Added characteristics for *SSP synchronous serial peripheral in master mode (SPI or TI mode) on page 62* and *SSP synchronous serial peripheral in slave mode (SPI or TI mode) on page 65* Added characteristics for *SMI - serial memory interface on page 68* Added *Table 42: USB startup time on page 70*
23-Oct-2007	4	Updated *Section 6.2.3: Thermal characteristics on page 33* Updated P_D, T_J and T_A in *Section 6.3: Operating conditions on page 34* Updated *Table 20: XT1 external clock source on page 44* Updated *Table 21: XRTC1 external clock source on page 45* Updated *Section 7: Package characteristics on page 76* (inches rounded to 4 decimal digits instead of 3) Updated Ordering information *Section 8: Order codes on page 81*
17-Feb-2009	5	Modified note 3 below *Table 8: Current characteristics on page 33* Added AHB clock frequency for write access to Flash registers in *Table 10: General operating conditions on page 34* Modified note 3 below *Table 41: SDA and SCL characteristics on page 69*

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