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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, SPI, SSI, SSP, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	72
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str755fv0h6

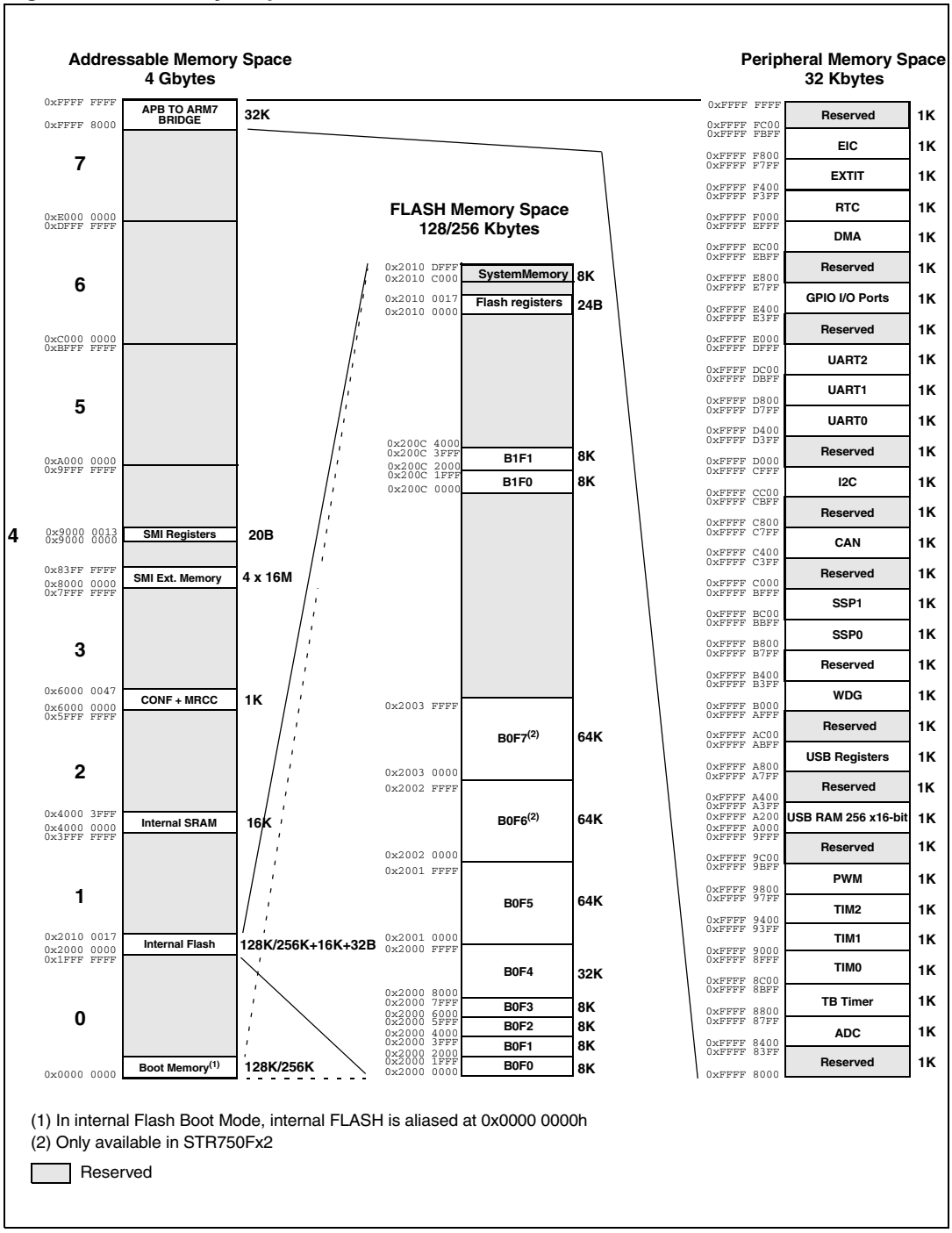
Contents

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
68	A10			P1.02 / TIM2_OC2	I/O	T_T	X	X		O2	X	X		**Port 1.02**	TIM2: Output compare 2 (remappable to P0.06)(8)	
69	D7	44	C6	VDD_IO	S									Supply Voltage for digital I/Os		
70	D8	45	D6	VDDA_ADC	S									Supply Voltage for A/D converter		
71	C9			P2.11	I/O	T_T	X	X		O2	X	X		**Port 2.11**		
72	B10			P2.10	I/O	T_T	X	X		O2	X	X		**Port 2.10**		
73	C8	46	D7	VSSA_ADC	S									Ground Voltage for A/D converter		
74	C7	47	C7	VSS_IO	S									Ground Voltage for digital I/Os		
75	E8	48	D5	VREG_DIS	I	T_T								Voltage Regulator Disable input		
76	A9	49	A8	P0.07 / SMI_DOUT / SSP0_MOSI	I/O	T_T	X	X	EIT2	O4	X	X		**Port 0.07**	Serial Memory Interface: data output	SSP0: Master out Slave in data
77	A8	50	A7	P0.06 / SMI_DIN / SSP0_MISO	I/O	T_T	X	X		O4	X	X		**Port 0.06**	Serial Memory Interface: data input	SSP0: Master in Slave out data
78	A7	51	A6	P0.05 / SSP0_SCLK / SMI_CK	I/O	T_T	X	X	EIT1	O4	X	X		**Port 0.05**	SSP0: Serial clock	Serial Memory Interface: Serial clock output
79	B7	52	B6	P0.04 / SMI_CS0 / SSP0_NSS	I/O	T_T	X	X		O4	X	X		**Port 0.04**	Serial Memory Interface: chip select output 0	SSP0: Slave select input
80	C5	53	B7	P1.10 PWM_EMERGENCY	I/O	T_T	X	X	EIT10	O2	X	X		**Port 1.10**	PWM: Emergency input	
81	B6	54	B5	P1.09 / PWM1	I/O	T_T	X	X	EIT9	O4	X	X		**Port 1.09**	PWM: PWM1 output	
82	C6			P2.09 / PWM1N	I/O	T_T	X	X		O2	X	X		**Port 2.09**	PWM: PWM1 complementary output(4)	
83	G7			P2.08 / PWM2	I/O	T_T	X	X		O2	X	X		**Port 2.08**	PWM: PWM2 output(4)	
84	G6			P2.07 / PWM2N	I/O	T_T	X	X		O2	X	X		**Port 2.07**	PWM: PWM2 complementary output(4)	
85	F7			P2.06 / PWM3	I/O	T_T	X	X		O2	X	X		**Port 2.06**	PWM: PWM3 output(4)	
86	F6			P2.05 / PWM3N	I/O	T_T	X	X		O2	X	X		**Port 2.05**	PWM: PWM3 complementary output(4)	
87	A6	55	A5	P1.08 / PWM1N / ADC_IN11	I/O	T_T	X	X		O4	X	X		**Port 1.08**	PWM: PWM1 complementary output(8)	ADC: analog input 11
88	B5	56	B4	P1.07 / PWM2	I/O	T_T	X	X	EIT8	O4	X	X		**Port 1.07**	PWM: PWM2 output(4)	
89	A5	57	A4	P1.06 / PWM2N / ADC_IN10	I/O	T_T	X	X		O4	X	X		**Port 1.06**	PWM: PWM2 complementary output(4)	ADC: analog input 10
90	B4	58	B3	P1.05 / PWM3	I/O	T_T	X	X	EIT7	O4	X	X		**Port 1.05**	PWM: PWM3 output(4)	

5 Memory map

Figure 5. Memory map



(1) In internal Flash Boot Mode, internal FLASH is aliased at 0x0000 0000h
(2) Only available in STR750Fx2

Reserved

6 Electrical parameters

6.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$max (given by the selected temperature range).

Data based on product characterisation, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25° C, V_{DD_IO}=3.3 V (for the 3.0 V≤V_{DD_IO}≤3.6 V voltage range) and V_{18}=1.8 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

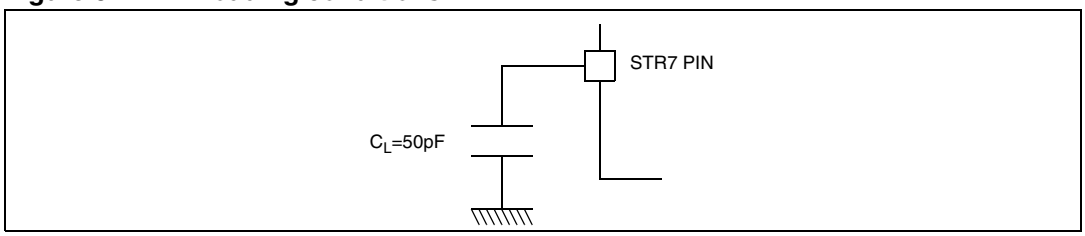
6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

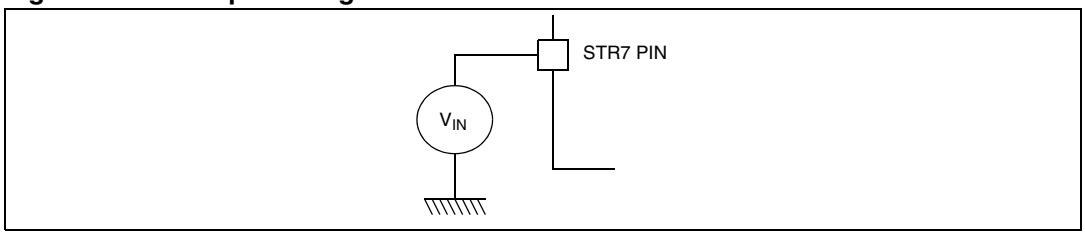
Figure 6. Pin loading conditions



6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 7. Pin input voltage



Power supply scheme 3: Single external 5 V power source

Figure 10. Power supply scheme 3

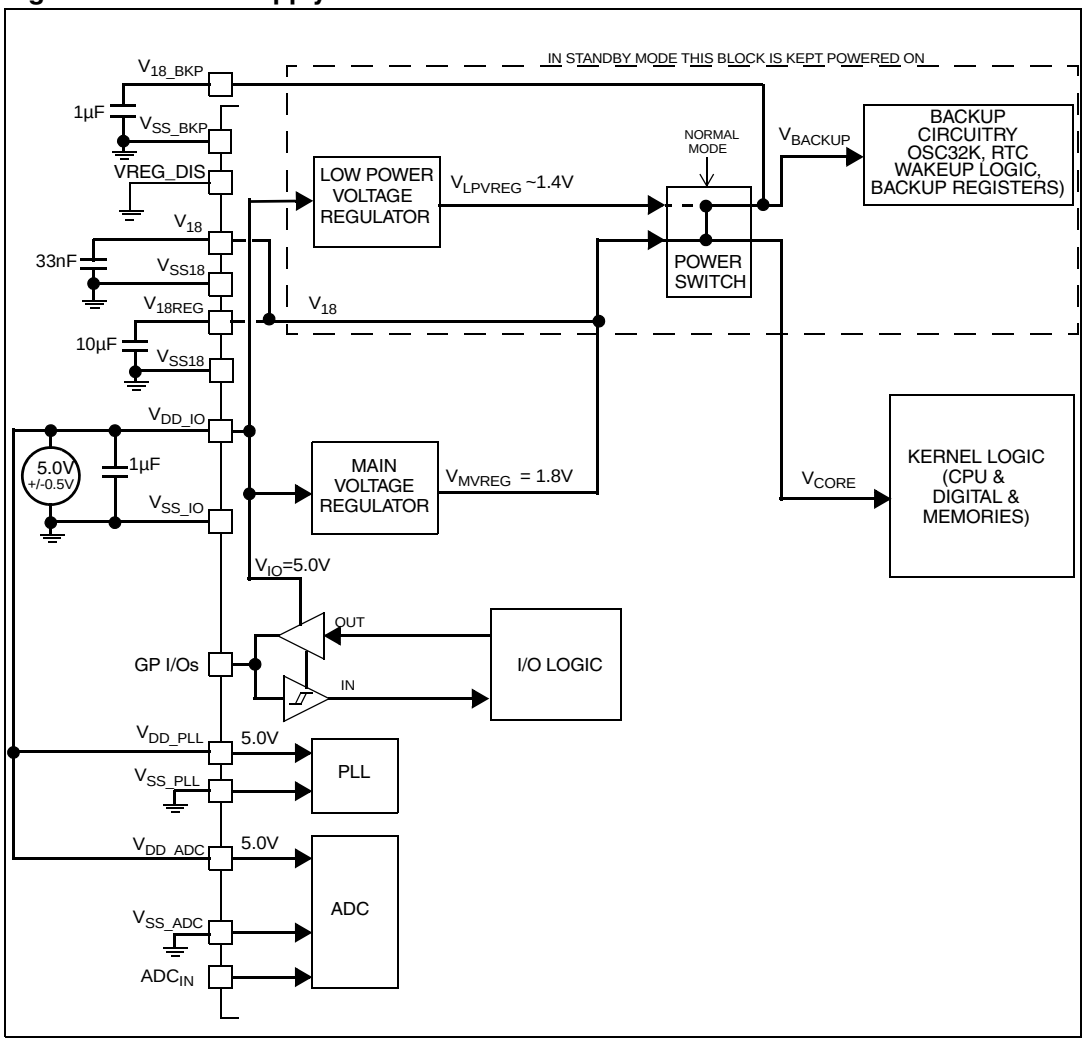


Figure 16. Power consumption in STOP mode in Single supply scheme (3.3 V range)

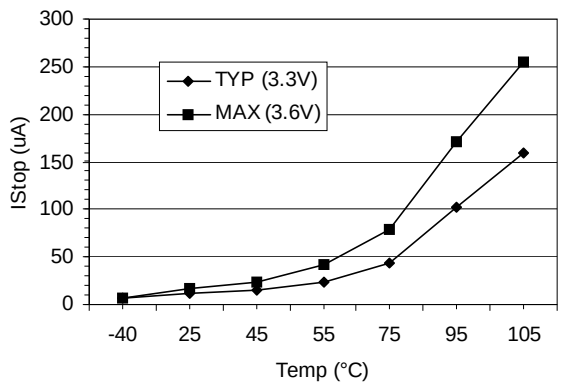


Figure 17. Power consumption in STOP mode Single supply scheme (5 V range)

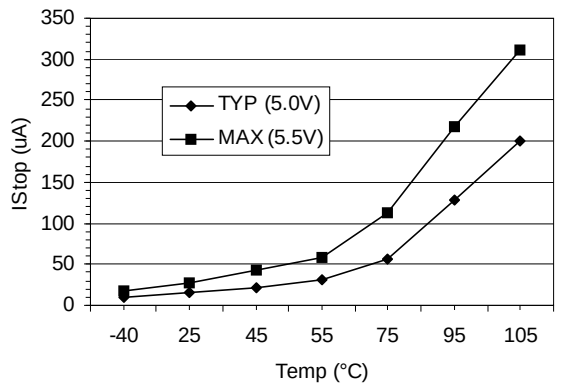


Figure 18. Power consumption in STANDBY mode (3.3 V range)

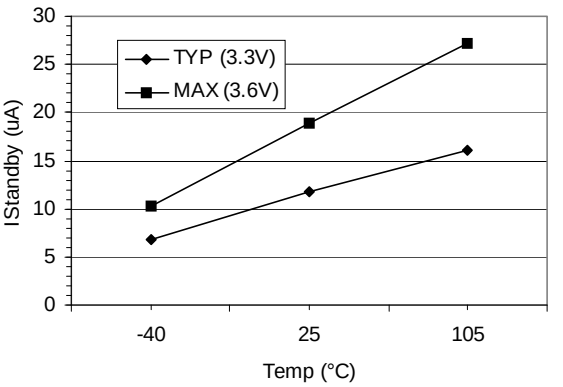
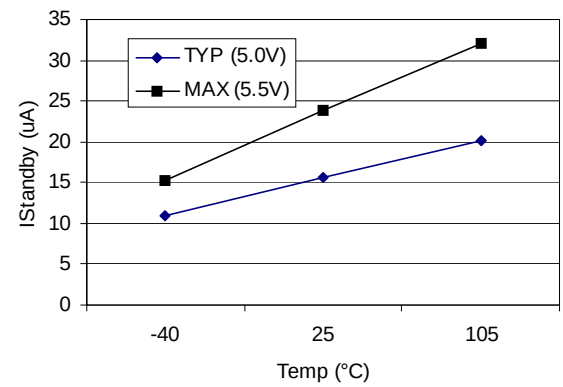


Figure 19. Power consumption in STANDBY mode (5 V range)



Typical power consumption

The following measurement conditions apply to *Table 15*, *Table 16* and *Table 17*.

In RUN mode:

- Program is executed from Flash (except if especially mentioned). The program consists of an infinite loop. When f_{HCLK} > 32 MHz, burst mode is activated.
- A standard 4 MHz crystal source is used.
- In all cases the PLL is used to multiply the frequency.
- All measurements are done in the single supply scheme with internal regulators used (see *Figure 12*)

In WFI Mode:

- In WFI Mode the measurement conditions are similar to RUN mode (OSC4M and PLL enabled). In addition, the Flash can be disabled depending on burst mode activation:
  - For AHB frequencies greater than 32 MHz, burst mode is activated and the Flash is kept enabled by setting the WFI_FLASH_EN bit (this bit cannot be reset when burst mode is activated).
  - For AHB frequencies less than or equal to 32 MHz, burst mode is deactivated, WFI_FLASH_EN is reset and the LP_PARAM14 bit is set (Flash is disabled in WFI mode).

In SLOW mode:

- The same program as in RUN mode is executed from Flash. The CPU is clocked by the FREEOSC, OSC4M, LPOSC or OSC32K. Only EXTIT peripheral is enabled in the MRCC_PCLKEN register.

In SLOW-WFI mode:

- In SLOW-WFI, the measurement conditions are similar to SLOW mode (CPU clocked by a low frequency clock). In addition, the LP_PARAM14 bit is set (FLASH is OFF). The WFI routine itself is executed from SRAM (it is not allowed to execute a WFI from the internal FLASH)

In STOP mode:

- Several measurements are given: in the single supply scheme with internal regulators used (see *Figure 12*): and in the dual supply scheme (see *Figure 13*).

In STANDBY mode:

- Three measurements are given:
  - The RTC is disabled, only the consumption of the LPVREG and RSM remain (almost no leakage currents)
  - The RTC is running, clocked by a standard 32.768 kHz crystal.
  - The RTC is running, clocked by the internal Low Power RC oscillator (LPOSC)
- STANDBY mode is only supported in the single supply scheme (see *Figure 12*)

Subject to general operating conditions for V_{DD_IO}, and T_A

Table 15. Single supply typical power consumption in Run, WFI, Slow and Slow-WFI modes

Symbol	Para meter	Conditions	3.3V typ(1)	5V typ(2)	Unit
I_{DD} (3)	Supply current in RUN mode(4)	Clocked by OSC4M with PLL multiplication, all peripherals enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz f_{HCLK}=56 MHz, f_{PCLK}=28 MHz f_{HCLK}=48 MHz, f_{PCLK}=24 MHz f_{HCLK}=32 MHz, f_{PCLK}=32 MHz f_{HCLK}=16 MHz, f_{PCLK}=16 MHz f_{HCLK}=8 MHz, f_{PCLK}=8 MHz	 80 75 65 59 34 20	 82 77 67 61 37 22	mA
		Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz f_{HCLK}=56 MHz, f_{PCLK}=28 MHz f_{HCLK}=48 MHz, f_{PCLK}=24 MHz f_{HCLK}=32 MHz, f_{PCLK}=32 MHz f_{HCLK}=16 MHz, f_{PCLK}=16 MHz f_{HCLK}=8 MHz, f_{PCLK}=8 MHz	 65 60 54 42 22 16	 67 62 55 44 24 18	mA
	Supply current in WFI mode(4)	Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz(5) f_{HCLK}=56 MHz, f_{PCLK}=28 MHz(5) f_{HCLK}=48 MHz, f_{PCLK}=24 MHz(5) f_{HCLK}=32 MHz, f_{PCLK}=32 MHz(6) f_{HCLK}=16 MHz, f_{PCLK}= 16 MHz (6) f_{HCLK}= 8 MHz, f_{PCLK}= 8 MHz(6)	 62 59 53 22 13 10	 63 60 54 23 15 11	mA
	Supply current in SLOW mode(4)	Clocked by FREEOSC: f_{HCLK}=f_{PCLK}=~5 MHz, Clocked by OSC4M: f_{HCLK}=f_{PCLK}=4 MHz Clocked by LPOSC: f_{HCLK}=f_{PCLK}=~300 kHz Clocked by OSC32K: f_{HCLK}=f_{PCLK}=32.768 kHz	9 8 3.65 3.5	10 9 3.9 4.2	mA
	Supply current in SLOW-WFI mode(4)(7)	Clocked by FREEOSC: f_{HCLK}=f_{PCLK}=~5 MHz Clocked by OSC4M: f_{HCLK}=f_{PCLK}=4 MHz Clocked by LPOSC: f_{HCLK}=f_{PCLK}=~300 kHz Clocked by OSC32K: f_{HCLK}=f_{PCLK}=32.768 kHz	3.5 3.1 1.15 0.98	4.0 3.75 1.65 1.5	mA

1. Typical data based on T_A=25° C and V_{DD_IO}=3.3V.
2. Typical data based on T_A=25° C and V_{DD_IO}=5.0V.
3. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4 on page 36*.
4. Single supply scheme see *Figure 14*.
5. Parameter setting BURST=1, WFI_FLASHEN=1
6. Parameter setting BURST=0, WFI_FLASHEN=0
7. Parameter setting WFI_FLASHEN=0, OSC4MOFF=1

difference between N+1 consecutive clock rising edges and T_{min} is the minimum time difference between N+1 consecutive clock rising edges.

N should be kept sufficiently large to have a long term jitter (ex: thousands).

For N=1, this becomes the single period jitter.

See *Figure 23*

- Cycle-to-cycle jitter (N period jitter)

  This corresponds to the time variation between adjacent cycles over a random sample of adjacent clock cycles pairs. Jitter(cycle-to-cycle) = Max(Tcycle n- Tcycle n-1) for n=1 to N.

  See *Figure 24*

Figure 23. Self-referred jitter (single and long term)

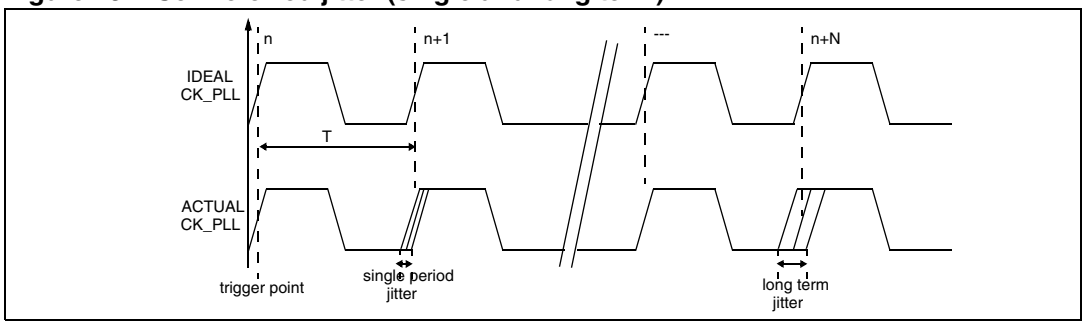
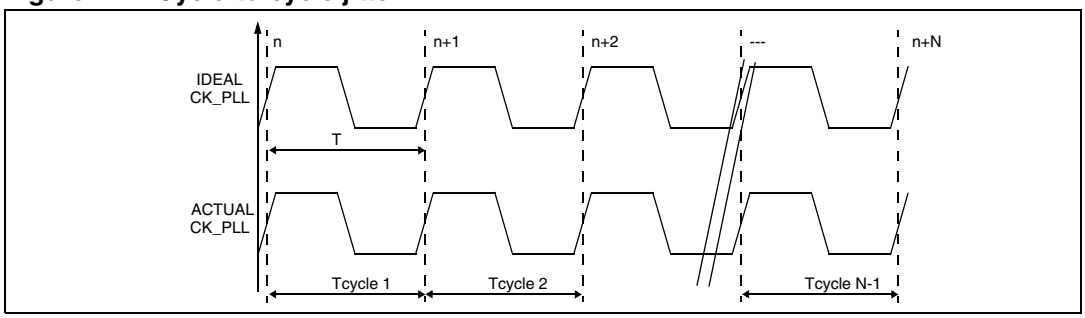


Figure 24. Cycle-to-cycle jitter



6.3.7 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electro magnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behaviour is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 28. EMC characteristics

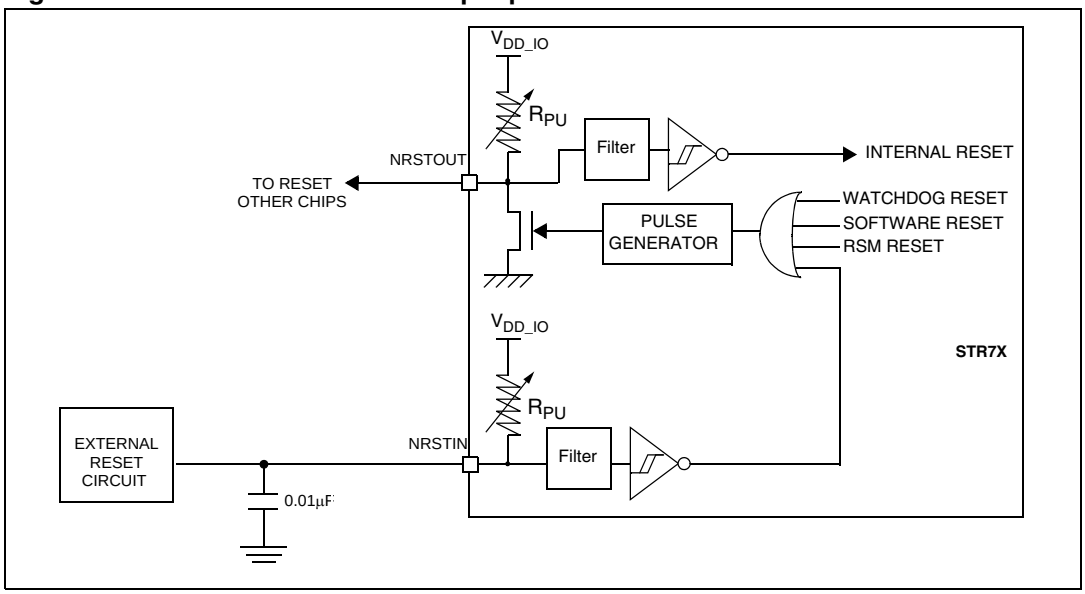
Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-2	Class A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-4	Class A

Table 33. Output driving current

I/O Output drive characteristics for V_{DD_IO} = 3.0 to 3.6 V and EN33 bit =1 or V_{DD_IO} = 4.5 to 5.5 V and EN33 bit =0						
I/O Type	**Symbol**	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
O2	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+2 mA		0.4	V
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-2 mA	V_{DD_IO}-0.8		
O4	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+4 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-4 mA	V_{DD_IO}-0.8		
O8	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+8 mA		0.4	
		Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time	I_{IO}=+20 mA, $T_A \leq 85°C$ $T_A \geq 85°C$		1.3 1.5	
			I_{IO}=+8 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-8 mA	V_{DD_IO}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS_IO}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD_IO}.

Figure 27. Recommended NRSTIN pin protection



1. The user must ensure that the level on the NRSTIN pin can go below the $V_{IL(NRSTIN)}$ max. level specified in *NRSTIN and NRSTOUT pins on page 58*. Otherwise the reset will not be taken into account internally.

SSP synchronous serial peripheral in slave mode (SPI or TI mode)

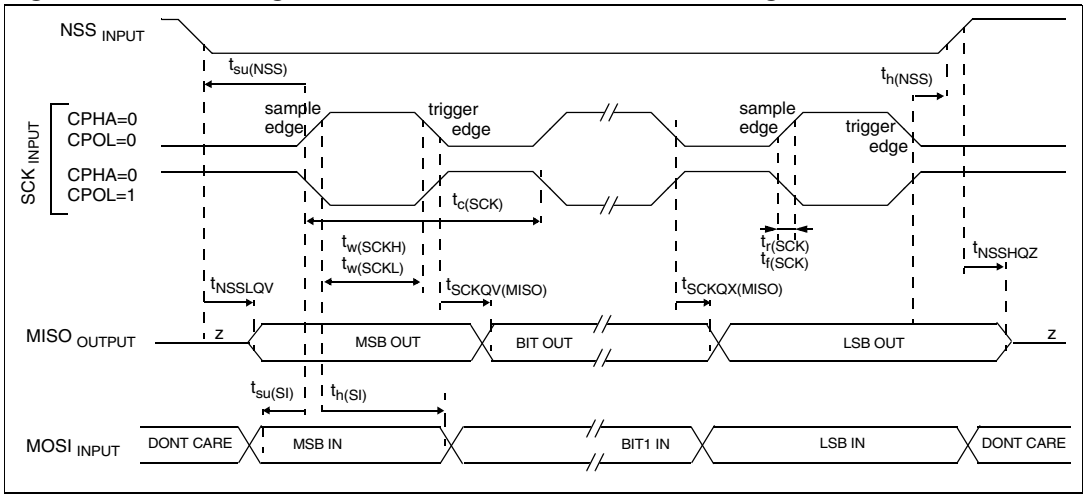
Subject to general operating conditions with $C_L \approx 45$ pF

Table 39. SSP slave mode characteristics(1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK}	SPI clock frequency		SSP0		2.66 MHz (f_{PLCK}/12)	MHz
			SSP1			
$t_{su(NSS)}$	NSS input setup time w.r.t SCK first edge		SSP0	0		ns
			SSP1	0		
$t_{h(NSS)}$	NSS input hold time w.r.t SCK last edge		SSP0	t_{PCLK}+15ns		
			SSP1	t_{PCLK}+15ns		
t_{NSSLQV}	NSS low to Data Output MISO valid time		SSP0	$2t_{PCLK}$	$3t_{PCLK}$+30 ns	
			SSP1	$2t_{PCLK}$	$3t_{PCLK}$+30 ns	
t_{NSSLQZ}	NSS low to Data Output MISO invalid time		SSP0	$2t_{PCLK}$	$3t_{PCLK}$+15 ns	
			SSP1	$2t_{PCLK}$	$3t_{PCLK}$+15 ns	
t_{SCKQV}	SCK trigger edge to data output MISO valid time		SSP0		15	
			SSP1		30	
t_{SCKQX}	SCK trigger edge to data output MISO invalid time		SSP0	$2t_{PCLK}$		
			SSP1	$2t_{PCLK}$		
$t_{su(MOSI)}$	MOSI setup time w.r.t SCK sampling edge		SSP0	0		
			SSP1	0		
$t_{h(MOSI)}$	MOSI hold time w.r.t SCK sampling edge		SSP0	$3t_{PCLK}$+15 ns		
			SSP1	$3t_{PCLK}$+15 ns		

1. Data based on characterisation results, not tested in production.

Figure 33. SPI configuration, slave mode with CPHA=0, single transfer



SMI - serial memory interface

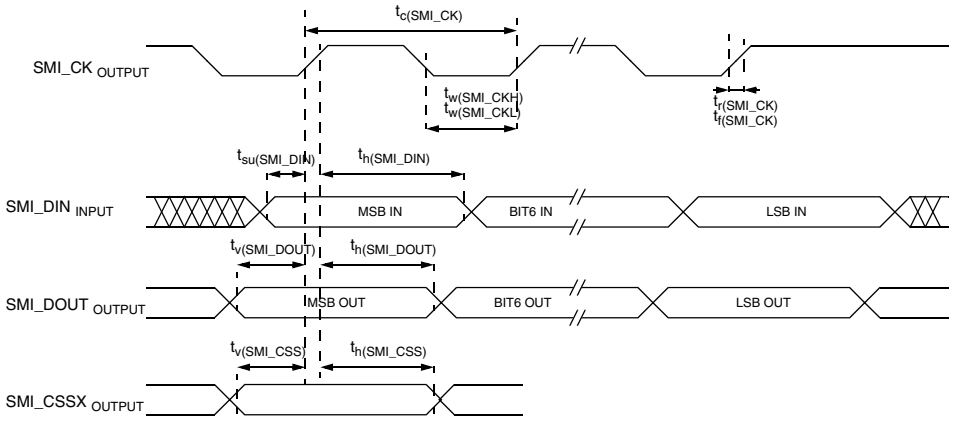
Subject to general operating conditions with $C_L \approx 30$ pF.

Table 40. SMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
f_{SMI_CK}	SMI clock frequency		32(2)(3)	MHz
			48(4)	
$t_{r(SMI\_CK)}$	SMI clock rise time		10	ns
$t_{f(SMI\_CK)}$	SMI clock fall time		8	
$t_{v(SMI\_DOUT)}$	Data output valid time		10	
$t_{h(SMI\_DOUT)}$	Data output hold time		0	
$t_{v(SMI\_CSSx)}$	CSS output valid time		10	
$t_{h(SMI\_CSSx)}$	CSS output hold time		0	
$t_{su(SMI\_DIN)}$	Data input setup time	0		
$t_{h(SMI\_DIN)}$	Data input hold time	5		

1. Data based on characterisation results, not tested in production.
2. Max. frequency = $f_{PCLK}/2 = 64/2 = 32$ MHz.
3. Valid for all temperature ranges: -40 to 105 °C, with 30 pF load capacitance.
4. Valid up to 60 °C, with 10 pF load capacitance.

Figure 39. SMI timing diagram



I²C - Inter IC control interface

Subject to general operating conditions for V_{DD_IO}, f_{PCLK}, and T_A unless otherwise specified.

The I²C interface meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Restriction: The I/O pins which SDA and SCL are mapped to are not “True” Open-Drain: when configured as open-drain, the PMOS connected between the I/O pin and V_{DD_IO} is disabled, but it is still present. Also, there is a protection diode between the I/O pin and V_{DD_IO}. Consequently, when using this I²C in a multi-master network, it is

6.3.12 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA_ADC}, f_{PCLK}, and T_A unless otherwise specified.

Table 45. 10-bit ADC characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
f_{ADC}	ADC clock frequency		0.4		8	MHz
V_{AIN}	Conversion voltage range(2)		V_{SSA_ADC}		V_{DDA_ADC}	V
R_{AIN}	External input impedance(3)(4)				10	kΩ
C_{AIN}	External capacitor on analog input(3)(4)				6.8	pF
I_{lkg}	Induced input leakage current	+400 µA injected on any pin			1	µA
		-400 µA injected on any pin except specific adjacent pins in *Table 46*			1	µA
		-400µA injected on specific adjacent pins in *Table 46*		40		µA
C_{ADC}	Internal sample and hold capacitor			3.5		pF
t_{CAL}	Calibration Time	f_{CK_ADC}=8 MHz	725.25			µs
			5802			$1/f_{ADC}$
t_{CONV}	Total Conversion time (including sampling time)	f_{CK_ADC}=8 MHz	3.75			µs
			30 (11 for sampling + 19 for Successive Approximation)			$1/f_{ADC}$
I_{ADC}		Sunk on V_{DDA_ADC}		3.7		mA

1. Unless otherwise specified, typical data are based on T_A=25°C. They are given only as design guidelines and are not tested.
2. Calibration is needed once after each power-up.
3. $C_{PARASITIC}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
4. Depending on the input signal variation (f_{AIN}), C_{AIN} can be increased for stabilization time and reduced to allow the use of a larger serial resistor (R_{AIN}). It is valid for all f_{ADC} frequencies ≤ 8 MHz.

General PCB design guidelines

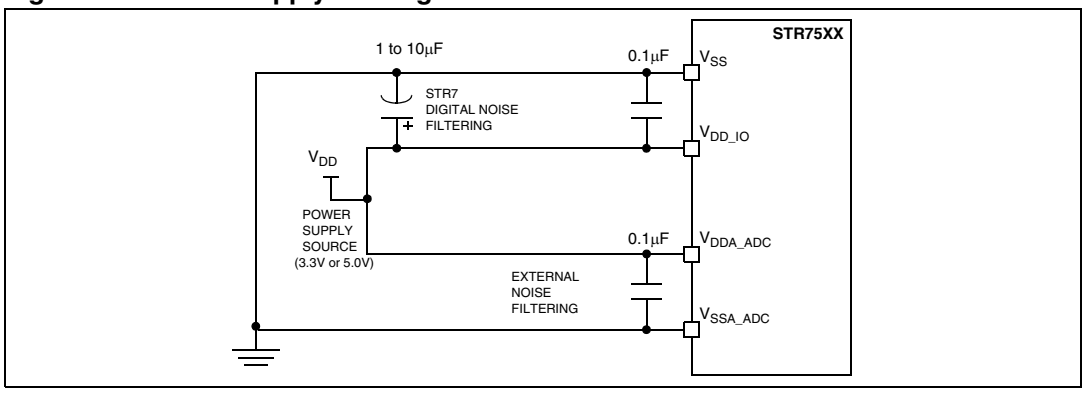
To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 µF and optionally, if needed 10 pF capacitors as close as possible to the STR7 power supply pins and a 1 to 10 µF capacitor close to the power source (see *Figure 43*).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{DDA_ADC} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs near the A/D input being converted.

Software filtering of spurious conversion results

For EMC performance reasons, it is recommended to filter A/D conversion outliers using software filtering techniques.

Figure 43. Power supply filtering

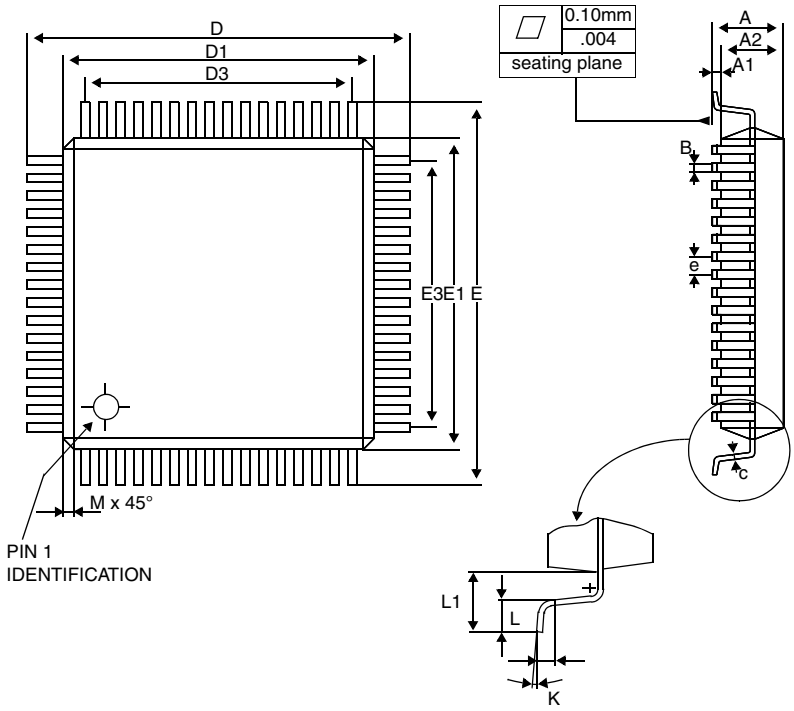


7 Package characteristics

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 Package mechanical data

Figure 45. 64-pin low profile quad flat package (10x10)



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of pins					
N	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 10: General operating conditions on page 34*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in ° C/W,
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$),
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum Power Dissipation on Output Pins.
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 48. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 100 - 14 x 14 mm / 0.5 mm pitch	46	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 100 - 10 x 10 x 1.7mm	41	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

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