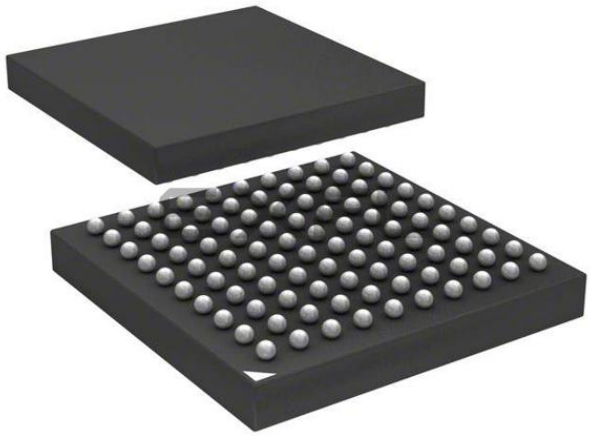

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, SPI, SSI, SSP, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str755fv2h6

Serial memory interface (SMI)

The Serial Memory interface is directly able to access up to 4 serial FLASH devices. It can be used to access data, execute code directly or boot the application from external memory. The memory is addressed as 4 banks of up to 16 Mbytes each.

Clocks and start-up

After RESET or when exiting from Low Power Mode, the CPU is clocked immediately by an internal RC oscillator (FREEOSC) at a frequency centered around 5 MHz, so the application code can start executing without delay. In parallel, the 4/8 MHz Oscillator is enabled and its stabilization time is monitored using a dedicated counter.

An oscillator failure detection is implemented: when the clock disappears on the XT1 pin, the circuit automatically switches to the FREEOSC oscillator and an interrupt is generated.

In Run mode, the AHB and APB clock speeds can be set at a large number of different frequencies thanks to the PLL and various prescalers: up to 60 MHz for AHB and up to 32 MHz for APB when fetching from Flash (64 MHz and 32 MHz when fetching from SRAM).

In SLOW mode, the AHB clock can be significantly decreased to reduce power consumption.

The built-in Clock Controller also provides the 48 MHz USB clock directly without any extra oscillators or PLL. For instance, starting from the 4 MHz crystal source, it is possible to obtain in parallel 60 MHz for the AHB clock, 48 MHz for the USB clock and 30 MHz for the APB peripherals.

Boot modes

At start-up, boot pins are used to select one of five boot options:

- Boot from internal flash
- Boot from external serial Flash memory
- Boot from internal boot loader
- Boot from internal SRAM

Booting from SMI memory allows booting from a serial flash. This way, a specific boot monitor can be implemented. Alternatively, the STR750F can boot from the internal boot loader that implements a boot from UART.

Power supply schemes

You can connect the device in any of the following ways depending on your application.

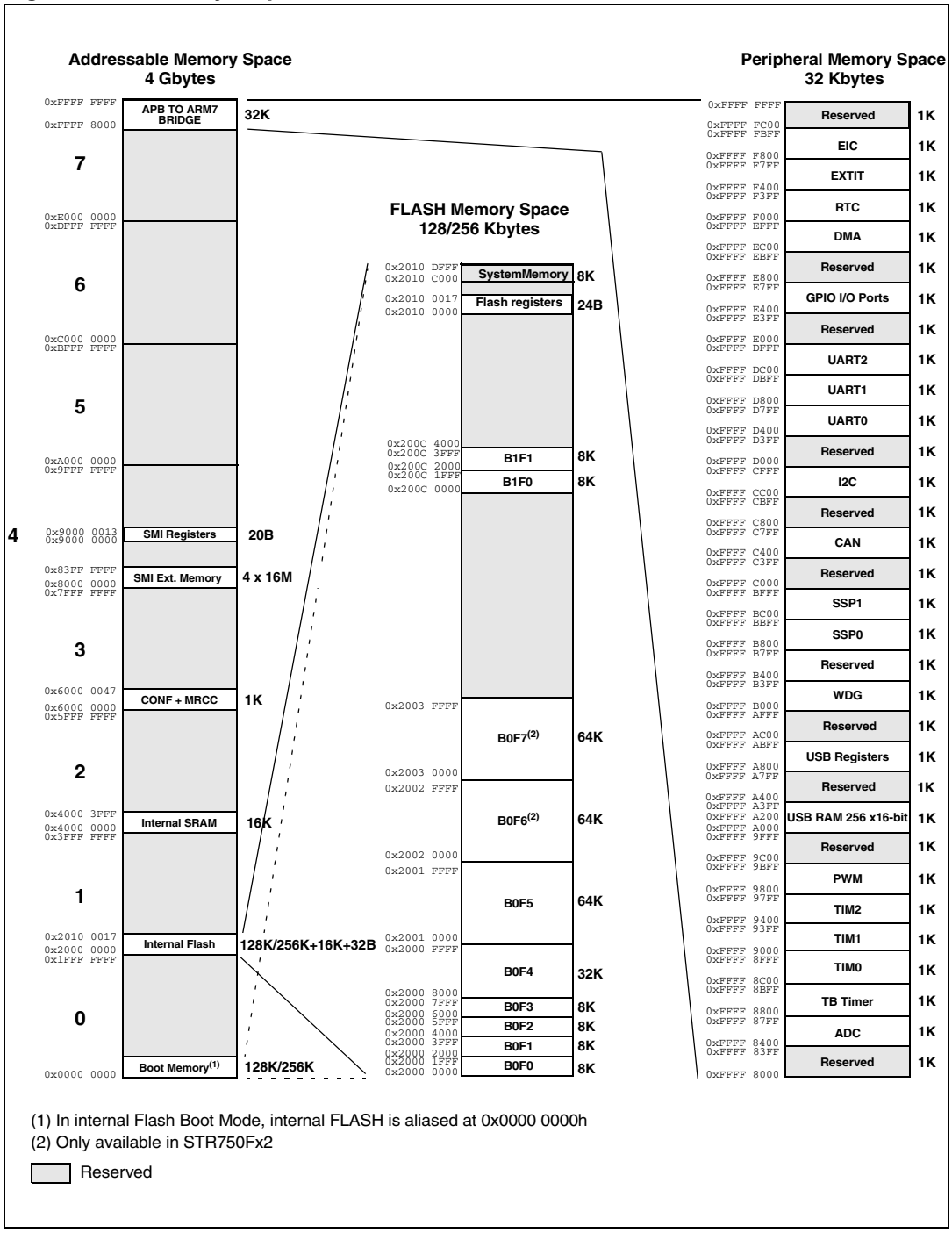
- **Power Scheme 1: Single external 3.3V power source**. In this configuration the V_{CORE} supply required for the internal logic is generated internally by the main voltage regulator and the V_{BACKUP} supply is generated internally by the low power voltage regulator. This scheme has the advantage of requiring only one 3.3V power source.
- **Power Scheme 2: Dual external 3.3V and 1.8V power sources.** In this configuration, the internal voltage regulators are switched off by forcing the VREG_DIS pin to high level. V_{CORE} is provided externally through the V_{18} and V_{18REG} power pins and V_{BACKUP} through the V_{18_BKP} pin. This scheme is intended to save power consumption for applications which already provide an 1.8V power supply.
- **Power Scheme 3: Single external 5.0V power source.** In this configuration the V_{CORE} supply required for the internal logic is generated internally by the main voltage

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
7	D1	5	D1	P0.29 / TIM1_TI1 / ADC_IN8	I/O	T_T	**X**	X		O2	X	X		**Port 0.29**	TIM1: Input Capture 1	ADC: Analog input 8
8	E1	6	D2	P0.28 / TIM1_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 0.28**	TIM1: Output Compare 1	
9	E5	7	D3	TEST	I									Reserved, must be tied to ground		
10	E4	8	D4	VSS_IO	S									Ground Voltage for digital I/Os		
11	E2			P0.23 / UART1_RTS / ADC_IN6	I/O	T_T	**X**	X		O2	X	X		**Port 0.23**	UART1: Ready To Send output(4)	ADC analog input 6
12	F5			P2.04 / TIM2_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 2.04**	TIM2: Output Compare 1(4)	
13	F1			P2.03 / UART1_RTS	I/O	T_T	**X**	X		O2	X	X		**Port 2.03**	UART1: Ready To Send output(4)	
14	F4			P2.02	I/O	T_T	**X**	X		O2	X	X		**Port 2.02**		
15	E3			P0.22 / UART1_CTS / ADC_IN5	I/O	T_T	**X**	X		O2	X	X		**Port 0.22**	UART1: Clear To Send input	ADC: Analog input 5
16	F2	9	E4	P0.21 / UART1_TX	I/O	T_T	**X**	X		O2	X	X		**Port 0.21**	UART1: Transmit data output (remappable to P0.15)(4)	
17	F3	10	E3	P0.20 / UART1_RX	I/O	T_T	**X**	X		O2	X	X		**Port 0.20**	UART1: Receive data input (remappable to P0.14)(4)	
18	G3	11	E2	P1.19 / JTMS	I/O	T_T	X	X		O2	X	X		**JTAG mode selection input(6)**	Port 1.19	
19	G2	12	E1	P1.18 / JTCK	I/O	T_T	X	X		O2	X	X		**JTAG clock input(6)**	Port 1.18	
20	H3	13	F4	P1.17 / JTDO	I/O	T_T	X	X		O8	X	X		**JTAG data output(6)**	Port 1.17	
21	H2	14	F3	P1.16 / JTDI	I/O	T_T	X	X		O2	X	X		**JTAG data input(6)**	Port 1.16	
22	G1	15	F2	NJTRST	I	T_T								JTAG reset input(5)		
23	G4			P2.01	I/O	T_T	**X**	X		O2	X	X		**Port 2.01**		
24	G5			P2.00	I/O	T_T	**X**	X		O2	X	X		**Port 2.00**		
25	H1	16	F1	P0.13 / RTCK / UART0_RTS UART2_TX	I/O	T_T	X	X		O8	X	X		**JTAG return clock output(6)**	Port 0.13 / UART0: Ready To Send output(4)	UART2: Transmit Data output (when remapped)(8)

5 Memory map

Figure 5. Memory map

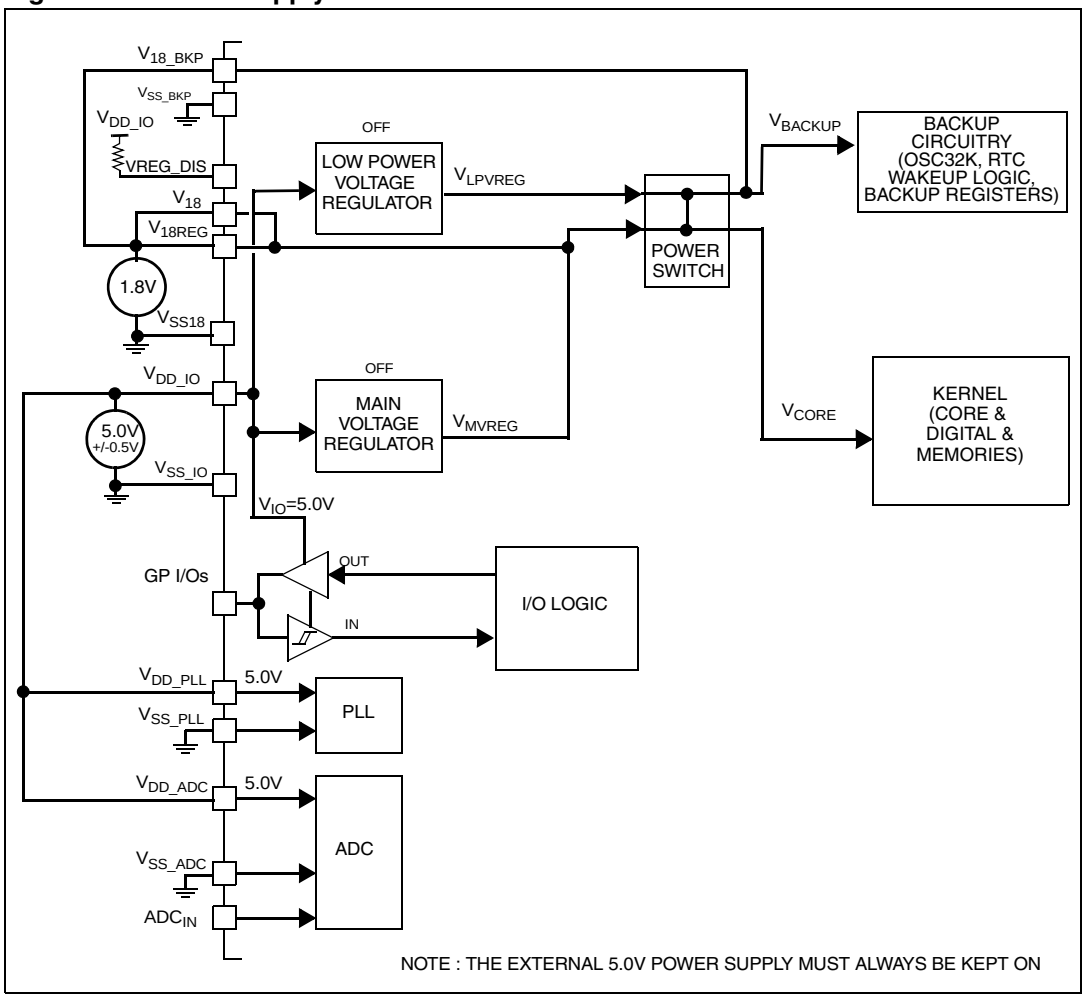


(1) In internal Flash Boot Mode, internal FLASH is aliased at 0x0000 0000h
(2) Only available in STR750Fx2

Reserved

Power supply scheme 4: Dual external 1.8 V and 5.0 V supply

Figure 11. Power supply scheme 4



6.1.7 I/O characteristics versus the various power schemes (3.3V or 5.0V)

Unless otherwise mentioned, all the I/O characteristics are valid for both

- V_{DD_IO}=3.0 V to 3.6 V with bit EN33=1
- V_{DD_IO}=4.5 V to 5.5 V with bit EN33=0

When V_{DD_IO}=3.0 V to 3.6 V, I/Os are not 5V tolerant.

6.1.8 Current consumption measurements

All the current consumption measurements mentioned below refer to Power scheme 1 and 2 as described in *Figure 12* and *Figure 13*

Figure 14. Power consumption measurements in power scheme 3 (regulators enabled)

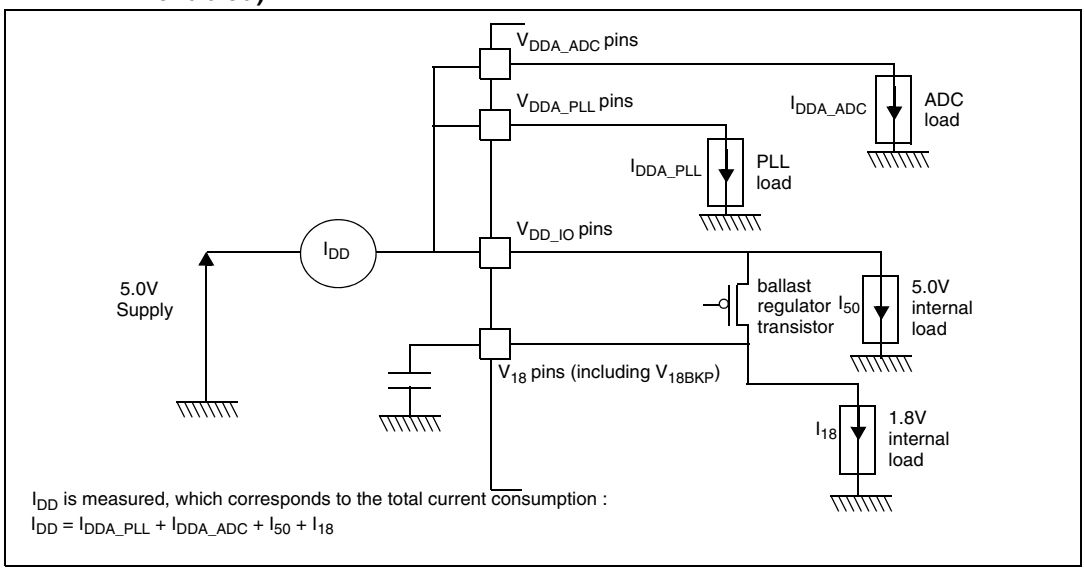
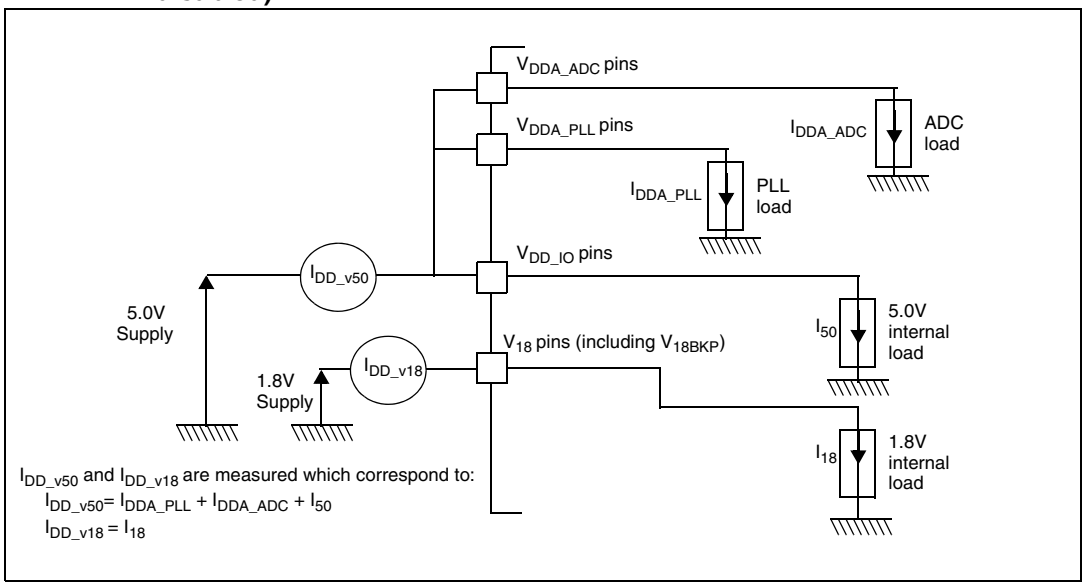


Figure 15. Power consumption measurements in power scheme 4 (regulators disabled)



6.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

6.2.1 Voltage characteristics

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD_x} - V_{SS_X} (1)	Including V_{DDA_ADC} and V_{DDA_PLL}	-0.3	6.5	V
V_{18} - V_{SS18}	Digital 1.8 V Supply voltage on all V_{18} power pins (when 1.8 V is provided externally)	-0.3	2.0	
V_{IN}	Input voltage on any pin (2)	V_{SS}-0.3 to V_{DD_IO}+0.3	V_{SS}-0.3 to V_{DD_IO}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different 3.3 V or 5.0 V power pins		50	mV
$\lvert\Delta V_{18x}\rvert$	Variations between different 1.8 V power pins(3)		25	
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 52*	see *: Absolute maximum ratings (electrical sensitivity) on page 52*	
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)			

1. All 3.3 V or 5.0 V power (V_{DD_IO}, V_{DDA_ADC}, V_{DDA_PLL}) and ground (V_{SS_IO}, V_{SSA_ADC}, V_{DDA_ADC}) pins must always be connected to the external 3.3V or 5.0V supply. When powered by 3.3V, I/Os are not 5V tolerant.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
3. Only when using external 1.8 V power supply. All the power (V_{18}, V_{18REG}, V_{18BKP}) and ground (V_{SS18}, V_{SSBKP}) pins must always be connected to the external 1.8 V supply.

6.2.2 Current characteristics

Table 8. Current characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD_IO} (1)	Total current into V_{DD_IO} power lines (source) (2)	150	mA
I_{VSS_IO} (1)	Total current out of V_{SS} ground lines (sink) (2)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ (3) & (4)	Injected current on NRSTIN pin	± 5	
	Injected current on XT1 and XT2 pins	± 5	
	Injected current on any other pin (5)	± 5	
$\Sigma I_{INJ(PIN)}$ (3)	Total injected current (sum of all I/O and control pins) (5)	± 25	

1. The user can use GPIOs to source or sink high current (up to 20 mA for O8 type High Sink I/Os). In this case, the user must ensure that these absolute max. values are not exceeded (taking into account the RUN power consumption) and must follow the rules described in *Section 6.3.8: I/O port pin characteristics on page 54*.
2. All 3.3 V or 5.0 V power (V_{DD_IO}, V_{DDA_ADC}, V_{DDA_PLL}) and ground (V_{SS_IO}, V_{SSA_ADC}, V_{DDA_ADC}) pins must always be connected to the external 3.3V or 5.0V supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Data based on T_A=25°C.
4. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.12: 10-bit ADC characteristics on page 72*.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

6.2.3 Thermal characteristics

Table 9. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3.4 Supply current characteristics

The current consumption is measured as described in *Figure 12 on page 30* and *Figure 13 on page 30*.

Subject to general operating conditions for V_{DD_IO}, and T_A

Maximum power consumption

For the measurements in *Table 13* and *Table 14*, the MCU is placed under the following conditions:

- All I/O pins are configured in output push-pull 0
- All peripherals are disabled except if explicitly mentioned.
- Embedded Regulators are used to provide 1.8 V (except if explicitly mentioned).

Table 13. Maximum power consumption in RUN and WFI modes

Symbol	Parameter	Conditions (1)		Typ (2)	Max (3)	Unit
I_{DD}	Supply current in RUN mode	External Clock with PLL multiplication, code running from RAM, all peripherals enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz Single supply scheme see *Figure 12* / *Figure 14*	3.3V and 5V range	80	90	mA
	Supply current in WFI mode	External Clock, code running from RAM: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz Single supply scheme see *Figure 12*./ *Figure 14* Parameter setting BURST=1, WFI_FLASHEN=1	3.3V and 5V range	62	67	mA

1. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4*.
2. Typical data are based on T_A=25°C, V_{DD_IO}=3.3V or 5.0V and V_{18}=1.8V unless otherwise specified.
3. Data based on product characterisation, tested in production at V_{DD_IO} max and V_{18} max (1.95V in dual supply mode or regulator output value in single supply mode) and T_A max.

Figure 16. Power consumption in STOP mode in Single supply scheme (3.3 V range)

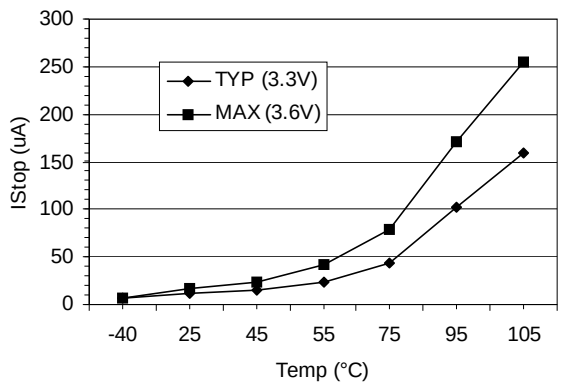


Figure 17. Power consumption in STOP mode Single supply scheme (5 V range)

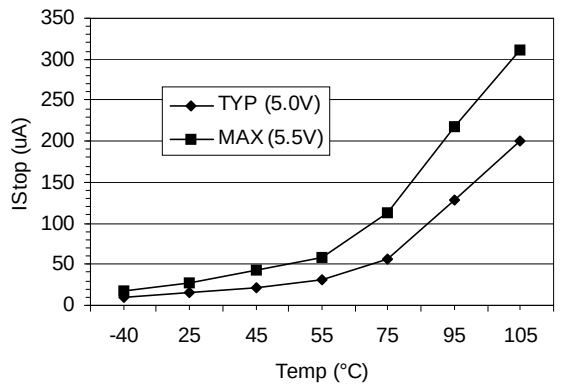


Figure 18. Power consumption in STANDBY mode (3.3 V range)

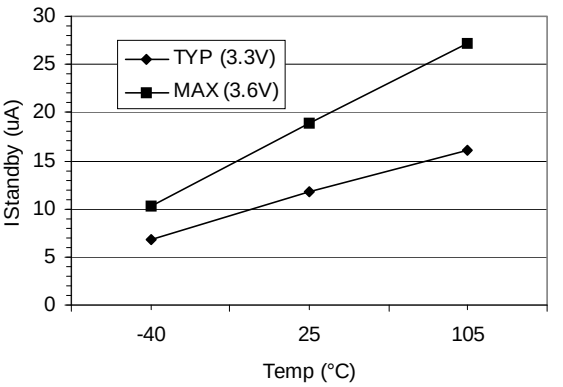


Figure 19. Power consumption in STANDBY mode (5 V range)

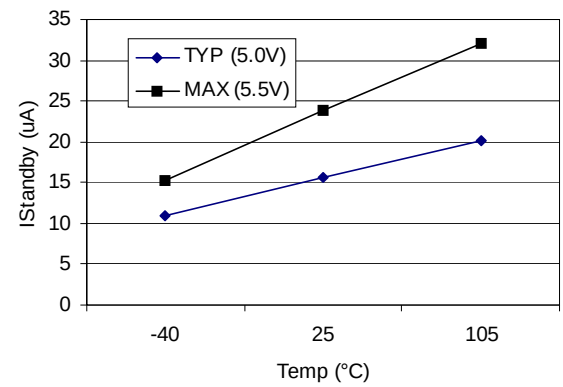


Table 16. Dual supply supply typical power consumption in Run, WFI, Slow and Slow-WFI modes

To calculate the power consumption in Dual supply mode, refer to the values given in *Table 15*. and consider that this consumption is split as follows:

$I_{DD(single\ supply)} \sim I_{DD(dual\ supply)} = I_{DD\_V18} + I_{DD(VDD\_IO)}$

For 3.3V range: $I_{DD(VDD\_IO)}$ ~ 1 to 2 mA

For 5V range: $I_{DD(VDD\_IO)}$ ~ 2 to 3 mA

Therefore most of the consumption is sunk on the V_{18} power supply

This formula does not apply in STOP and STANDBY modes, refer to *Table 17*.

Subject to general operating conditions for V_{DD_IO}, and T_A

Table 17. Typical power consumption in STOP and STANDBY modes

Symbol	Parameter	Conditions		3.3V Typ(1)	5V Typ(2)	Unit
I_{DD}(3)	Supply current in STOP mode(4)	LP_PARAM bits: ALL OFF(5)		12	15	µA
		LP_PARAM bits : MVREG ON, OSC4M OFF, FLASH OFF(6)		130	135	
		LP_PARAM bits: MVREG ON, OSC4M ON , FLASH OFF(6)		1950	1930	
		LP_PARAM bits: MVREG ON, OSC4M OFF, FLASH ON (6)		630	635	
		LP_PARAM bits: MVREG ON, OSC4M ON, FLASH ON (6)		2435	2425	
	Supply current in STOP mode(7)	LPPARAM bits: ALL OFF, with V_{18}=1.8 V	I_{DD_V18} I_{DD_V33}	5 <1	5 <1	µA
		LP_PARAM bits: OSC4M ON, FLASH OFF	I_{DD_V18} I_{DD_V33}	410 1475	410 1435	
		LP_PARAM bits: OSC4M OFF, FLASH ON	I_{DD_V18} I_{DD_V33}	550 <1	550 1	
		LP_PARAM bits: OSC4M ON, FLASH ON	I_{DD_V18} I_{DD_V33}	910 1475	910 1445	
	Supply current in STANDBY mode(4)	RTC OFF		11	14	µA
		RTC ON clocked by OSC32K		14	18	

1. Typical data are based on T_A=25°C, V_{DD_IO}=3.3 V and V_{18}=1.8 V unless otherwise indicated in the table.
2. Typical data are based on T_A=25°C, V_{DD_IO}=5.0 V and V_{18}=1.8 V unless otherwise indicated in the table.
3. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4 on page 36*.
4. Single supply scheme see *Figure 12*.
5. In this mode, the whole digital circuitry is powered internally by the LPVREG at approximately 1.4 V, which significantly reduces the leakage currents.
6. In this mode, the whole digital circuitry is powered internally by the MVREG at 1.8 V.
7. Dual supply scheme see *Figure 13*.

Supply and clock manager power consumption

Table 18. Supply and clock manager power consumption

Symbol	Parameter	Conditions[1]	3.3V Typ	5V Typ	Unit
$I_{DD(OSC4M)}$	Supply current of resonator oscillator in STOP or WFI mode (LP_PARAM bit: OSC4M ON)	External components specified in: *4/8 MHz crystal / ceramic resonator oscillator (XT1/XT2) on page 46*	1815	1795	µA
$I_{DD(FLASH)}$	FLASH static current consumption in STOP or WFI mode (LP_PARAM bit FLASH ON)		515	515	
$I_{DD(MVREG)}$	Main Voltage Regulator static current consumption in STOP mode (LP_PARAM bit: MVREG ON)		130	135	
$I_{DD(LPVREG)}$	Low Power Voltage Regulator + RSM current static current consumption	STOP mode includes leakage where V_{18} is internally set to 1.4 V	12	15	
		STANDBY mode where V_{18BKP} and V_{18} are internally set to 1.4 V and 0 V respectively	11	14	

1. Measurements performed in 3.3V single supply mode see *Figure 12*

XRTC1 external clock source

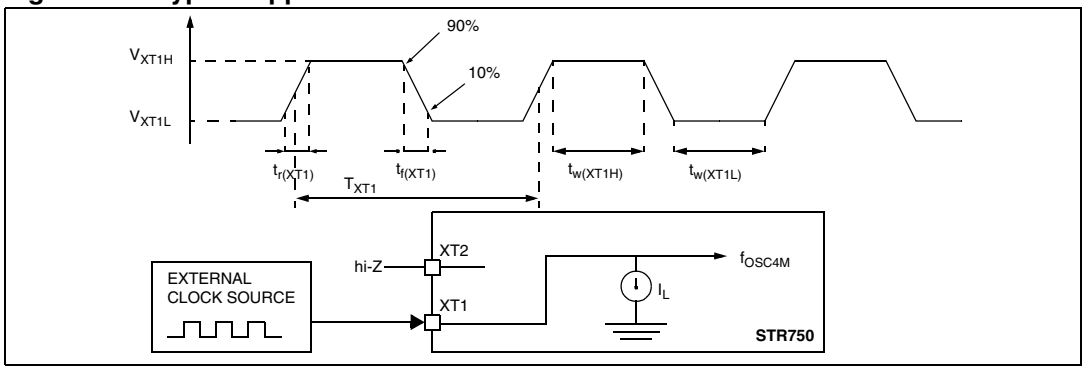
Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 21. XRTC1 external clock source

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
f_{XRTC1}	External clock source frequency	see *Figure 20*		32.768	500	kHz
V_{XRTC1H}	XRTC1 input pin high level voltage		$0.7xV_{DD\_IO}$		V_{DD_IO}	V
V_{XRTC1L}	XRTC1 input pin low level voltage		V_{SS}		$0.3xV_{DD\_IO}$	
$t_{w(XRTC1H)}$ $t_{w(XRTC1L)}$	XRTC1 high or low time(2)		900			ns
$t_{r(XRTC1)}$ $t_{f(XRTC1)}$	XRTC1 rise or fall time(2)				50	
I_L	XRTCx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD\_IO}$			±1	µA
$C_{IN(RTC1)}$	XRTC1 input capacitance(2)			5		pF
$DuCy_{(RTC1)}$	Duty cycle		30		70	%

1. Data based on typical application software.
2. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 20. Typical application with an external clock source



4/8 MHz crystal / ceramic resonator oscillator (XT1/XT2)

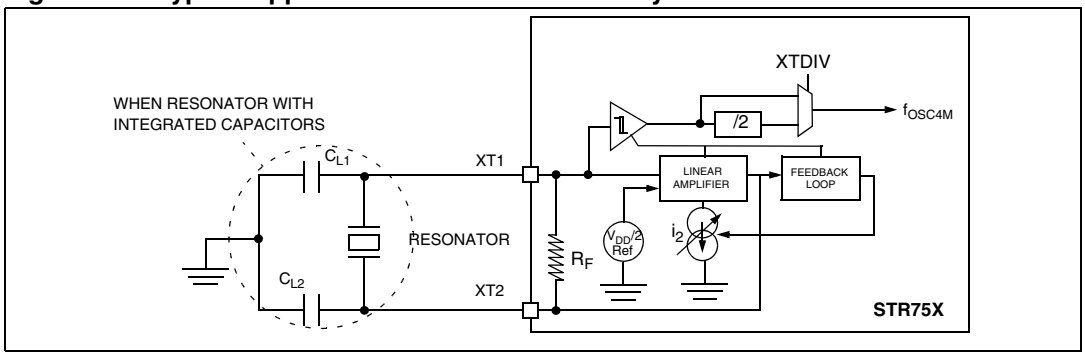
The STR750 system clock or the input of the PLL can be supplied by a OSC4M which is a 4 MHz clock generated from a 4 MHz or 8 MHz crystal or ceramic resonator. If using an 8 MHz oscillator, software set the XTDIV bit to enable a divider by 2 and generate a 4 MHz OSC4M clock. All the information given in this paragraph are based on product characterisation with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

Table 22. 4/8 MHz crystal / ceramic resonator oscillator (XT1/XT2)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC4M}	Oscillator frequency	4 MHz Crystal/Resonator Oscillator connected on XT1/XT2 XTDIV=0 or 8 MHz Crystal/Resonator Oscillator connected on XT1/XT2 XTDIV=1		4		MHz
R_F	Feedback resistor		200	240	270	kΩ
C_{L1}(2) C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal or ceramic resonator (R_S)(3)	R_S=200Ω			60	pF
i_2	XT2 driving current	V_{DD_IO}=3.3 V or 5.0 V		425		µA
$t_{SU(OSC4M)}$(4)	Startup time at V_{DD_IO} power-up			1		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5-pF to 25-pF range (typ.) designed for high-frequency applications and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included when sizing C_{L1} and C_{L2} (10 pF can be used as a rough estimate of the combined pin and board capacitance).
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(OSC4M)}$ is the typical start-up time measured from the moment V_{DD_IO} is powered (with a quick V_{DD_IO} ramp-up from 0 to 3.3V (<50µs) to a stabilized 4MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal/ceramic resonator manufacturer.

Figure 21. Typical application with a 4 or 8 MHz crystal or ceramic resonator



PLL characteristics

Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 24. PLL characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock			4.0		MHz
	PLL input clock duty cycle		40		60	%
f_{PLL_OUT}	PLL multiplier output clock	f_{PLL_IN}x 24			165	MHz
f_{VCO}	VCO frequency range	When PLL operates (locked)	336		960	MHz
t_{LOCK}	PLL lock time				300	µs
$\Delta t_{JITTER1}$(2)(3)	Single period jitter (+/-3Σ peak to peak)	f_{PLL_IN} = 4 MHz(4) V_{DD_IO} is stable			+/-250	ps
$\Delta t_{JITTER2}$(2)(3)	Long term jitter (+/-3Σ peak to peak)	f_{PLL_IN} = 4 MHz(4) V_{DD_IO} is stable			+/-2.5	ns
$\Delta t_{JITTER3}$(2)(3)	Cycle to cycle jitter (+/-3Σ peak to peak)	f_{PLL_IN} = 4 MHz(4) V_{DD_IO} is stable			+/-500	ps

1. Data based on product characterisation, not tested in production.
2. Refer to jitter terminology in *: PLL characteristics on page 47* for details on how jitter is specified.
3. The jitter specification holds true only up to 50mV (peak-to-peak) noise on V_{DDA_PLL} and V_{18} supplies. Jitter will increase if the noise is more than 50mV. In addition, it assumes that the input clock has no jitter.
4. The PLL parameters (MX1, MX0, PRESC1, PRESC2) must respect the constraints described in*: PLL characteristics on page 47*.

Internal RC oscillators (FREEOSC & LPOSC)

Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 25. Internal RC oscillators (FREEOSC & LPOSC)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{CK\_FREEOSC}$	FREEOSC Oscillator Frequency		3	5	8	MHz
f_{CK_LPOSC}	LPOSC Oscillator Frequency		150	300	500	kHz

6.3.6 Memory characteristics

Flash memory

Subject to general operating conditions for V_{DD_IO} and V_{18}, T_A = -40 to 105 °C unless otherwise specified.

Table 26. Flash memory characteristics

Symbol	Parameter	Test Conditions	Value		Unit
			Typ	Max(1)	
t_{PW}	Word Program		35		µs
t_{PDW}	Double Word Program		60		µs
t_{PB0}	Bank 0 Program (256K)	Single Word programming of a checker-board pattern	2	4.9(2)	s
t_{PB1}	Bank 1 Program (16K)	Single Word programming of a checker-board pattern	125	224(2)	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed (all 1) Preprogrammed (all 0)	1.54 1.176	2.94(2) 2.38(2)	s
t_{ES}	Sector Erase (8K)	Not preprogrammed (all 1) Preprogrammed (all 0)	392 343	560(2) 532(2)	ms
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed (all 1) Preprogrammed (all 0)	8.0 6.6	13.7 11.2	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed (all 1) Preprogrammed (all 0)	0.9 0.8	1.5 1.3	s
t_{RPD}	Recovery when disabled			20	µs
t_{PSL}	Program Suspend Latency			10	µs
t_{ESL}	Erase Suspend Latency			300	µs

1. Data based on characterisation not tested in production
2. 10K program/erase cycles.

Table 27. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END_B0}	Endurance (Bank 0 sectors)		10			kcycles
N_{END_B1}	Endurance (Bank 1 sectors)		100			kcycles
Y_{RET}	Data Retention	T_A=85° C	20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

1. Data based on characterisation not tested in production.

6.3.8 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

Table 32. General characteristics

I/O static characteristics							
Symbol	**Parameter**	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
V_{IL}	Input low level voltage	TTL ports				0.8	V
V_{IH}	Input high level voltage			2			
V_{hys}	Schmitt trigger voltage hysteresis(1)				400		mV
$I_{INJ(PIN)}$	Injected Current on any I/O pin					± 4	mA
$\Sigma I_{INJ(PIN}$ (2)	Total injected current (sum of all I/O and control pins)					± 25	
I_{lkg}	Input leakage current on robust pins	See *Section 6.3.12 on page 72*					
	Input leakage current(3)	$V_{SS} \le V_{IN} \le V_{DD\_IO}$				±1	µA
I_S	Static current consumption(4)	Floating input mode			200		
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN}=V_{SS}$	V_{DD_IO}=3.3 V	50	95	200	kΩ
			V_{DD_IO}=5 V	20	58	150	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN}=V_{DD\_IO}$	V_{DD_IO}=3.3 V	25	80	180	kΩ
			V_{DD_IO}=5 V	20	50	120	kΩ
C_{IO}	I/O pin capacitance				5		pF
$t_{w(IT)in}$	External interrupt/wake-up lines pulse time(6)			2			T_{APB}

1. Hysteresis voltage between Schmitt trigger switching levels.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{DD\_IO}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 6.2 on page 32* for more details.
3. Leakage could be higher than max. if negative current is injected on adjacent pins.
4. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor (see *Figure 25*). Data based on design simulation and/or technology characteristics, not tested in production.
5. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor.
6. To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

NRSTIN and NRSTOUT pins

NRSTIN Pin Input Driver is TTL/LVTTL as for all GP I/Os. A permanent pull-up is present which is the same as R_{PU} (see : General characteristics on page 54)

NRSTOUT Pin Output Driver is equivalent to the O2 type driver except that it works only as an open-drain (the P-MOS is de-activated). A permanent pull-up is present which is the same as R_{PU} (see : General characteristics on page 54)

Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

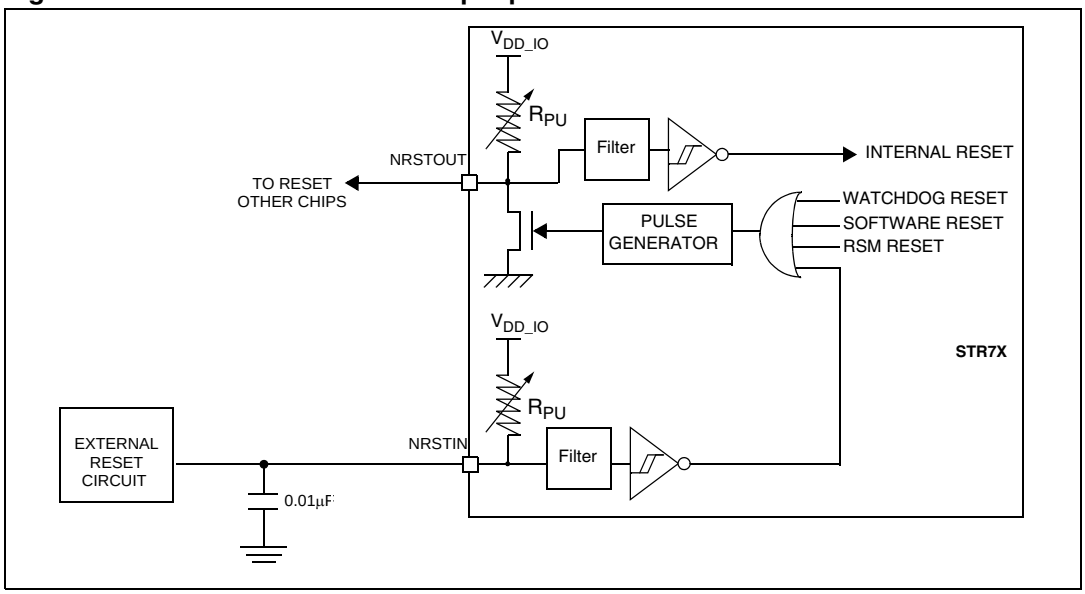
Table 35. NRSTIN and NRSTOUT pins

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
$V_{IL(NRSTIN)}$	NRSTIN Input low level voltage(1)					0.8	V
$V_{IH(NRSTIN)}$	NRSTIN Input high level voltage(1)			2			
$V_{hys(NRSTIN)}$	NRSTIN Schmitt trigger voltage hysteresis(2)				400		mV
$V_{OL(NRSTIN)}$	NRSTOUT Output low level voltage(3)	I_{IO}=+2 mA				0.4	V
$R_{PU(NRSTIN)}$	NRSTIN Weak pull-up equivalent resistor(4)	V_{IN}=V_{SS}	V_{DD_IO}=3.3 V	25	50	100	kΩ
			V_{DD_IO}=5 V	20	31	100	kΩ
$t_{w(RSTL)out}$	Generated reset pulse duration (visible at NRSTOUT pin)(5)	Internal reset source		15	20		µs
$t_{h(RSTL)in}$	External reset pulse hold time at NRSTIN pin(6)	At V_{DD_IO} power-up(5)		20			µs
		When V_{DD_IO} is established(5)		1			µs
$t_{g(RSTL)in}$	maximum negative spike duration filtered at NRSTIN pin(7)	The time between two spikes must be higher than 1/2 of the spike duration.			150		ns

1. Data based on product characterisation, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels.
3. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 6.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
4. The R_{PU} pull-up equivalent resistor are based on a resistive transistor
5. To guarantee the reset of the device, a minimum pulse of 15 µs has to be applied to the internal reset. At V_{DD_IO} power-up, the built-in reset stretcher may not generate the 15 µs pulse duration while once V_{DD_IO} is established, an external reset pulse will be internally stretched up to 15 µs thanks to the reset pulse stretcher.
6. The reset network (the resistor and two capacitors) protects the device against parasitic resets, especially in noisy environments.
7. In fact the filter is made to ignore all incoming pulses with short duration:
   - all negative spikes with a duration less than 150 ns are filtered
   - all trains of negative spikes with a ratio of 1/2 are filtered. This means that all spikes with a maximum duration of 150 ns with minimum interval between spikes of 75 ns are filtered.

   Data guaranteed by design, not tested in production.

Figure 27. Recommended NRSTIN pin protection



1. The user must ensure that the level on the NRSTIN pin can go below the $V_{IL(NRSTIN)}$ max. level specified in *NRSTIN and NRSTOUT pins on page 58*. Otherwise the reset will not be taken into account internally.

SMI - serial memory interface

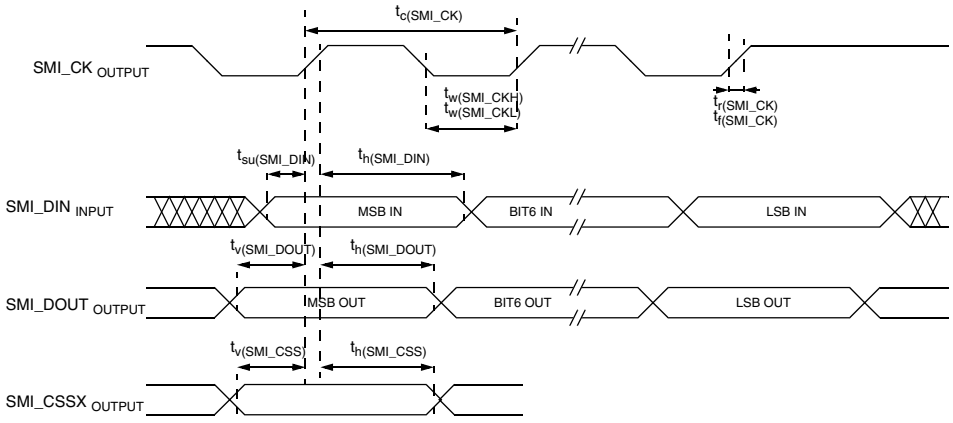
Subject to general operating conditions with $C_L \approx 30$ pF.

Table 40. SMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
f_{SMI_CK}	SMI clock frequency		32(2)(3)	MHz
			48(4)	
$t_{r(SMI\_CK)}$	SMI clock rise time		10	ns
$t_{f(SMI\_CK)}$	SMI clock fall time		8	
$t_{v(SMI\_DOUT)}$	Data output valid time		10	
$t_{h(SMI\_DOUT)}$	Data output hold time		0	
$t_{v(SMI\_CSSx)}$	CSS output valid time		10	
$t_{h(SMI\_CSSx)}$	CSS output hold time		0	
$t_{su(SMI\_DIN)}$	Data input setup time	0		
$t_{h(SMI\_DIN)}$	Data input hold time	5		

1. Data based on characterisation results, not tested in production.
2. Max. frequency = $f_{PCLK}/2 = 64/2 = 32$ MHz.
3. Valid for all temperature ranges: -40 to 105 °C, with 30 pF load capacitance.
4. Valid up to 60 °C, with 10 pF load capacitance.

Figure 39. SMI timing diagram



I²C - Inter IC control interface

Subject to general operating conditions for V_{DD_IO}, f_{PCLK}, and T_A unless otherwise specified.

The I²C interface meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Restriction: The I/O pins which SDA and SCL are mapped to are not “True” Open-Drain: when configured as open-drain, the PMOS connected between the I/O pin and V_{DD_IO} is disabled, but it is still present. Also, there is a protection diode between the I/O pin and V_{DD_IO}. Consequently, when using this I²C in a multi-master network, it is

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