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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM7® |
| Core Size | 32-Bit Single-Core |
| Speed | 60MHz |
| Connectivity | I²C, SPI, SSI, SSP, UART/USART |
| Peripherals | DMA, PWM, WDT |
| Number of I/O | 72 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/str755fv2t6 |

# 1 Description

The STR750 family of 32-bit microcontrollers combines the industry-standard ARM7TDMI® 32-bit RISC core, featuring high performance, very low power, and very dense code, with a comprehensive set of peripherals and ST's latest 0.18µ embedded Flash technology. The STR750 family comprises a range of devices integrating a common set of peripherals as well as USB, CAN and some key innovations like clock failure detection and an advanced motor control timer. It supports both 3.3V and 5V, and it is also available in an extended temperature range (-40 to +105°C). This makes it a genuine general purpose microcontroller family, suitable for a wide range of applications:

- Appliances, brushless motor drives
- USB peripherals, UPS, alarm systems
- Programmable logic controllers, circuit breakers, inverters
- Medical and portable equipment

# 2 Device overview

**Table 2. Device overview**

| Features | STR755FR0 STR755FR1 STR755FR2 | STR751FR0/ STR751FR1/ STR751FR2 | STR752FR0/ STR752FR1/ STR752FR2 | STR755FV0 STR755FV1/ STR755FV2 | STR750FV0/ STR750FV1/ STR750FV2 |
|---|---|---|---|---|---|
| Flash - Bank 0 (bytes) | 64K/128K/256K | | | | |
| Flash - Bank 1 (bytes) | 16K RWW | | | | |
| RAM (bytes) | 16K | | | | |
| Operating Temperature. | Ambient temp.:-40 to +85°C / -40 to +105°C (see *Table 49*)<br>Junction temp. -40 to + 125 °C (see *Table 10*) | | | | |
| Common Peripherals | 3 UARTs, 2 SSPs, 1 I2C, 3 timers 1 PWM timer, 38 I/Os 13 Wake-up lines, 11 A/D Channels | | | 3 UARTs, 2 SSPs, 1 $I^2C$, 3 timers 1 PWM timer, 72 I/Os 15 Wake-up lines, 16 A/D Channels | |
| USB/CAN peripherals | None | USB | CAN | None | USB+CAN |
| Operating Voltage | 3.3V or 5V | 3.3V | 3.3V or 5V | | |
| Packages (**x**) | **T**=LQFP64 10x10, **H**=LFBGA64 | | | **T**=LQFP100 14x14, **H**=LFBGA100 | |

# 4 Pin description

**Figure 2. LQFP100 pinout**

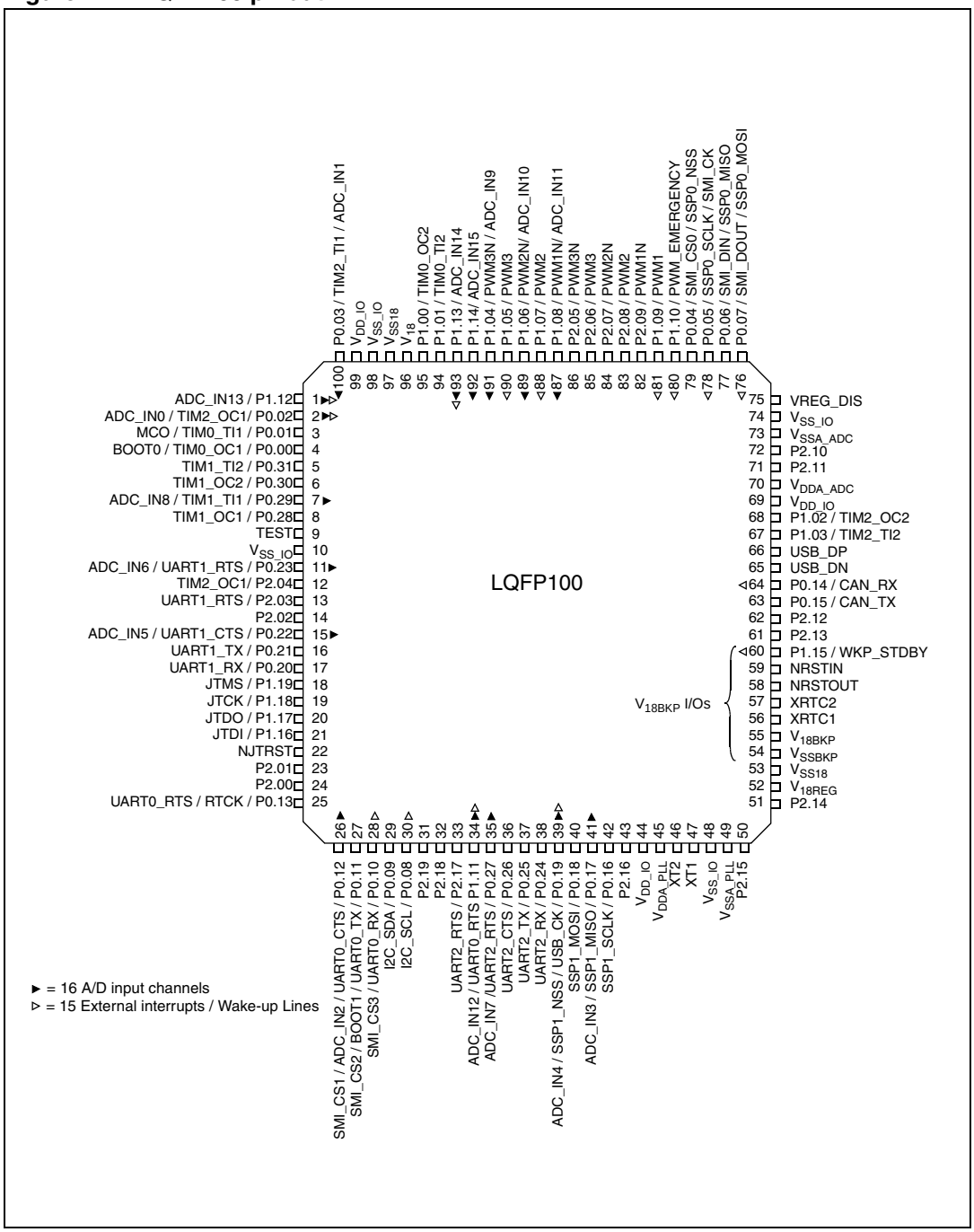


**Table 4. LFBGA100 ball connections**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| **A** | P0.03 | P1.13 | P1.14 | P1.04 | P1.06 | P1.08 | P0.05 | P0.06 | P0.07 | P1.02 |
| **B** | P1.12 | P0.02 | P0.01 | P1.05 | P1.07 | P1.09 | P0.04 | P2.13 | P1.03 | P2.10 |
| **C** | P0.31 | P0.00 | $V_{DD\_IO}$ | $V_{18}$ | P1.10 | P2.09 | $V_{SS\_IO}$ | $V_{SSA\_ADC}$ | P2.11 | USB_DP |
| **D** | P0.29 | P0.30 | $V_{SS\_IO}$ | $V_{SS18}$ | P1.01 | P1.15 | $V_{DD\_IO}$ | $V_{DDA\_ADC}$ | P2.12 | USB_DN |
| **E** | P0.28 | P0.23 | P0.22 | $V_{SS\_IO}$ | TEST | P1.00 | NRSTOUT | VREG_DIS | NRSTIN | P0.14 |
| **F** | P2.03 | P0.21 | P0.20 | P2.02 | P2.04 | P2.05 | P2.06 | $V_{SS18}$ | $V_{SSBKP}$ | P0.15 |
| **G** | NJTRST | P1.18 | P1.19 | P2.01 | P2.00 | P2.07 | 2.08 | $V_{18REG}$ | $V_{18BKP}$ | XRTC2 |
| **H** | P0.13 | P1.16 | P1.17 | P2.19 | P2.18 | P2.17 | P0.24 | P2.14 | P2.16 | XRTC1 |
| **J** | P0.11 | P0.12 | P1.11 | P0.27 | P0.19 | P0.26 | P0.25 | P2.15 | $V_{DD\_IO}$ | $V_{SS\_IO}$ |
| **K** | P0.10 | P0.09 | P0.08 | P0.18 | P0.17 | P0.16 | XT1 | XT2 | $V_{DDA\_PLL}$ | $V_{SSA\_PLL}$ |

**Table 5. LFBGA64 ball connections**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| **A** | P0.03 | $V_{SS\_IO}$ | P1.04 | P1.06 | P1.08 | P0.05 | P0.06 | P0.07 |
| **B** | P1.12 | $V_{DD\_IO}$ | P1.05 | P1.07 | P1.09 | P0.04 | P1.10 | P1.03 |
| **C** | P0.01 | P0.02 | P0.00 | $V_{18}$ | $V_{SS18}$ | $V_{DD\_IO}$ | $V_{SS\_IO}$ | P0.14 |
| **D** | P0.29 | P0.28 | TEST | $V_{SS\_IO}$ | VREG_DIS | $V_{DDA\_ADC}$ | $V_{SSA\_ADC}$ | P0.15 |
| **E** | P1.18 | P1.19 | P0.20 | P0.21 | NRSTOUT | NRSTIN | $V_{18BKP}$ | XRTC2 |
| **F** | P0.13 | NJTRST | P1.16 | P1.17 | $V_{18REG}$ | $V_{SS18}$ | $V_{SSBKP}$ | XRTC1 |
| **G** | P0.11 | P0.12 | P1.11 | P0.19 | $V_{DD\_IO}$ | $V_{SS\_IO}$ | $V_{DDA\_PLL}$ | $V_{SSA\_PLL}$ |
| **H** | P0.10 | P0.09 | P0.08 | P0.17 | P0.18 | P0.16 | XT2 | XT1 |

### Port reset state

The reset state of the I/O ports is GPIO input floating. Exceptions are P1[19:16] and P0.13 which are configured as JTAG alternate functions:

- The JTAG inputs (JTDI, JTMS and JTDI) are configured as input floating and are ready to accept JTAG sequences.
- The JTAG output JTDO is configured as floating when idle (no JTAG operation) and is configured in output push-pull only when serial JTAG data must be output.
- The JTAG output RTCK is always configured as output push-pull. It outputs '0' level during the reset phase and then outputs the JTCK input signal resynchronized 3 times by the internal AHB clock.
- The GPIO_PCx registers do not control JTAG AF selection, so the reset values of GPIO_PCx for P1[19:16] and P0. 13 are the same as other ports. Refer to the GPIO section of the STR750 Reference Manual for the register description and reset values.
- P0.11 and P0.00 are sampled by the boot logic after reset, prior to fetching the first word of user code at address 0000 0000h.
- When booting from SMI (and only in this case), the reset state of the following GPIOs is "SMI alternate function output enabled":
  - P0.07 (SMI_DOUT)
  - P0.05 (SMI_CLK)
  - P0.04 (SMI_CS0)
  - P0.06 (SMI_DIN)

  Note that the other SMI pins: SMI_CS1,2,3 (P0.12, P0.11, P0.10) are not affected.

To avoid excess power consumption, unused I/O ports must be tied to ground.

**Table 6. STR750F pin description**

| Pin n° | | | | Pin name | Type | Input | | | | Output | | | Usable in Standby | Main function (after reset) | Alternate function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100[1] | LFBGA100[1] | LQFP64[2] | LFBGA64[2] | | | Input Level | floating | pu/pd | Ext. int /Wake-up | Capability | OD [3] | PP | | | | |
| 1 | B1 | 1 | B1 | P1.12 / ADC_IN13 | I/O | $T_T$ | **X** | X | EIT12 | O8 | X | X | | **Port 1.12** | ADC: Analog input 13 | |
| 2 | B2 | 2 | C2 | P0.02 / TIM2_OC1 / ADC_IN0 | I/O | $T_T$ | **X** | X | EIT0 | O8 | X | X | | **Port 0.02** | TIM2: Output Compare 1[4] | ADC: Analog input 0 |
| 3 | B3 | 3 | C1 | P0.01 / TIM0_TI1 / MCO | I/O | $T_T$ | **X** | X | | O8 | X | X | | **Port 0.01** | TIM0: Input Capture / trigger / external clock 1 | Main Clock Output |
| 4 | C2 | 4 | C3 | P0.00 / TIM0_OC1 / BOOT0 | I/O | $T_T$ | **X** | X | | O8 | X | X | | **Port 0.00 / Boot mode selection input 0** | TIM0: Output Compare 1 | |
| 5 | C1 | | | P0.31 / TIM1_TI2 | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 0.31** | TIM1: Input Capture / trigger / external clock 2 | |
| 6 | D2 | | | P0.30 / TIM1_OC2 | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 0.30** | TIM1: Output Compare 2 | |

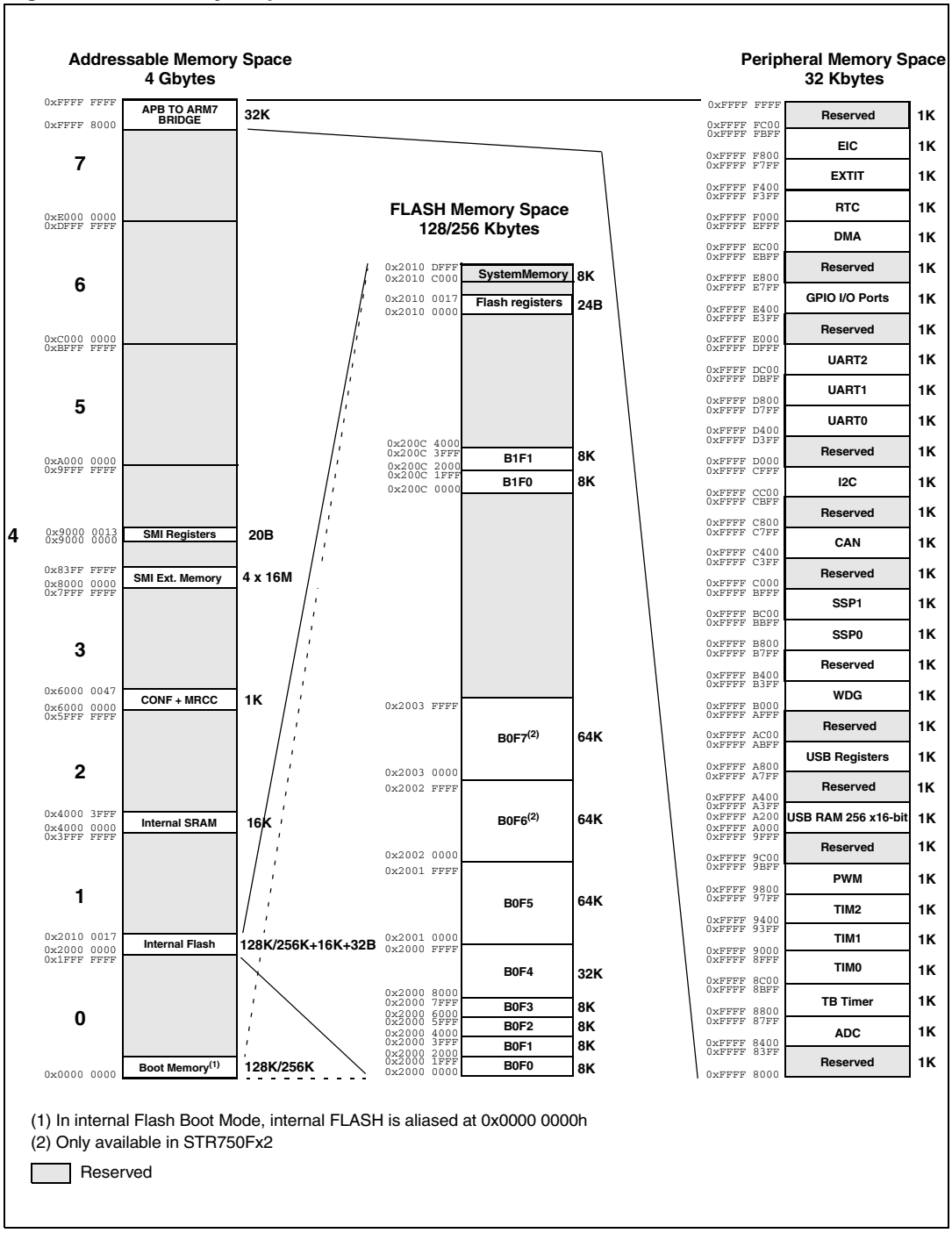
**Table 6. STR750F pin description (continued)**

| Pin n° | | | | Pin name | Type | Input | | | | Output | | | Usable in Standby | Main function (after reset) | Alternate function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100(1) | LFBGA100(1) | LQFP64(2) | LFBGA64(2) | | | Input Level | floating | pu/pd | Ext. int /Wake-up | Capability | OD (3) | PP | | | | |
| 91 | A4 | 59 | A3 | P1.04 / PWM3N / ADC_IN9 | I/O | $T_T$ | **X** | X | | O4 | X | X | | **Port 1.04** | PWM: PWM3 complementary output(4) | ADC: analog input 9 |
| 92 | A3 | | | P1.14 / ADC_IN15 | I/O | $T_T$ | **X** | X | | O8 | X | X | | **Port 1.14** | ADC: analog input 15 | |
| 93 | A2 | | | P1.13 / ADC_IN14 | I/O | $T_T$ | **X** | X | EIT13 | O8 | X | X | | **Port 1.13** | ADC: analog input 14 | |
| 94 | D5 | | | P1.01 / TIM0_TI2 | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 1.01** | TIM0: Input Capture / trigger / external clock 2 (remappable to P0.05)(8) | |
| 95 | E6 | | | P1.00 / TIM0_OC2 | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 1.00** | TIM0: Output compare 2 (remappable to P0.04)(8) | |
| 96 | C4 | 60 | C4 | V18 | S | | | | | | | | | Stabilization for main voltage regulator. Requires external capacitors 33nF between V18 and VSS18. See *Figure 4.2*. To be connected to the 1.8V external power supply when embedded regulators are not used. | | |
| 97 | D4 | 61 | C5 | VSS18 | S | | | | | | | | | Ground Voltage for the main voltage regulator. | | |
| 98 | D3 | 62 | A2 | VSS_IO | S | | | | | | | | | Ground Voltage for digital I/Os | | |
| 99 | C3 | 63 | B2 | VDD_IO | S | | | | | | | | | Supply Voltage for digital I/Os | | |
| 100 | A1 | 64 | A1 | P0.03 / TIM2_TI1 / ADC_IN1 | I/O | $T_T$ | **X** | X | | O2 | X | X | | **Port 0.03** | TIM2: Input Capture / trigger / external clock 1 | ADC: analog input 1 |

1. For STR755FVx part numbers, the USB pins must be left unconnected.
2. The non available pins on LQPFP64 and LFBGA64 packages are internally tied to low level.
3. None of the I/Os are True Open Drain: when configured as Open Drain, there is always a protection diode between the I/O pin and VDD_IO.
4. In the 100-pin package, this Alternate Function is duplicated on two ports. You can configure one port to use this AF, the other port is then free for general purpose I/O (GPIO), external interrupt/wake-up lines, or analog input (ADC_IN) where these functions are listed in the table.
5. It is mandatory that the NJTRST pin is reset to ground during the power-up phase. It is recommended to connect this pin to NRSTOUT pin (if available) or NRSTIN.
6. After reset, these pins are enabled as JTAG alternate function see (*Port reset state on page 16*). To use these ports as general purpose I/O (GPIO), the DBGOFF control bit in the GPIO_REMAP0R register must be set by software (in this case, debugging these I/Os via JTAG is not possible).
7. There are two different TQFP and BGA 64-pin packages: in the first one, pins 41 and 42 are mapped to USB DN/DP while for the second one, they are mapped to P0.15/CAN_TX and P0.14/CAN_RX.
8. For details on remapping these alternate functions, refer to the GPIO_REMAP0R register description.

# 5 Memory map

**Figure 5. Memory map**




(1) In internal Flash Boot Mode, internal FLASH is aliased at 0x0000 0000h
(2) Only available in STR750Fx2

Reserved

**Figure 14. Power consumption measurements in power scheme 3 (regulators enabled)**

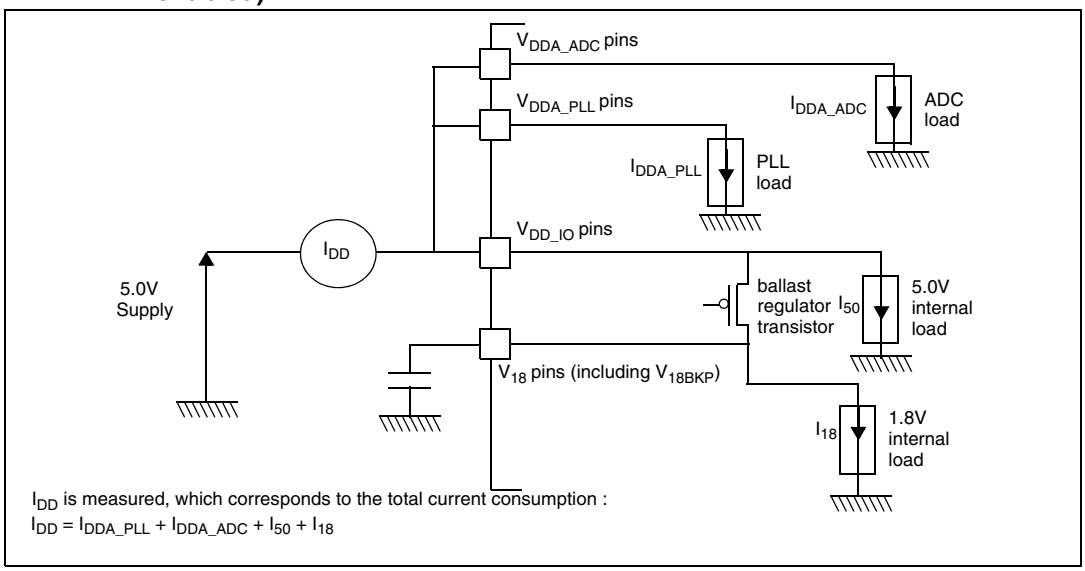
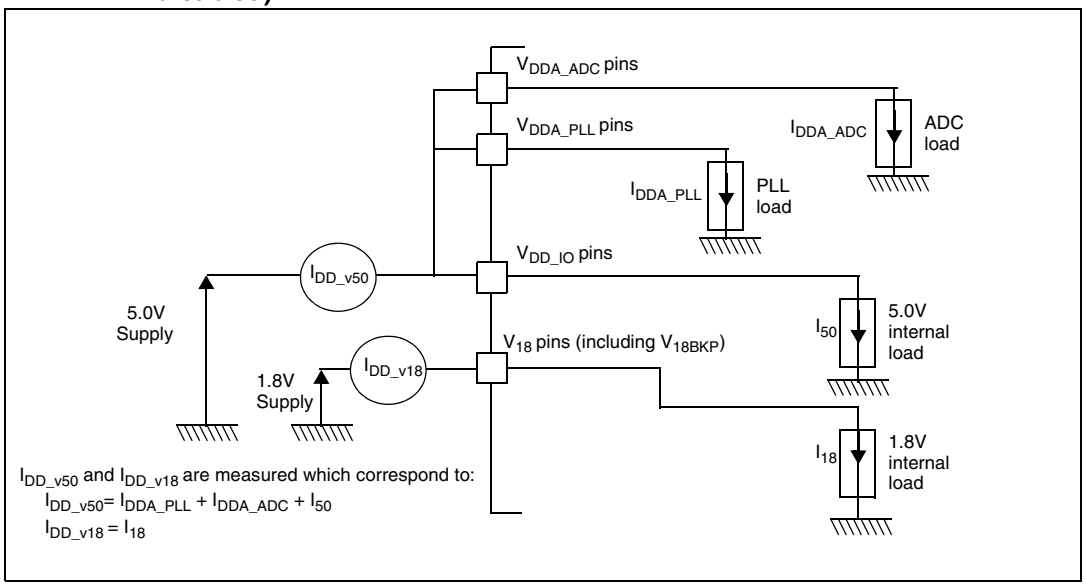



**Figure 15. Power consumption measurements in power scheme 4 (regulators disabled)**



### 6.2.2 Current characteristics

**Table 8. Current characteristics**

| Symbol | Ratings | Maximum value | Unit |
|---|---|---|---|
| $I_{VDD\_IO}$ (1) | Total current into $V_{DD\_IO}$ power lines (source) (2) | 150 | mA |
| $I_{VSS\_IO}$ (1) | Total current out of $V_{SS}$ ground lines (sink) (2) | 150 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/Os and control pin | - 25 | |
| $I_{INJ(PIN)}$ (3) & (4) | Injected current on NRSTIN pin | ± 5 | |
| | Injected current on XT1 and XT2 pins | ± 5 | |
| | Injected current on any other pin (5) | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ (3) | Total injected current (sum of all I/O and control pins) (5) | ± 25 | |

1. The user can use GPIOs to source or sink high current (up to 20 mA for O8 type High Sink I/Os). In this case, the user must ensure that these absolute max. values are not exceeded (taking into account the RUN power consumption) and must follow the rules described in *Section 6.3.8: I/O port pin characteristics on page 54*.
2. All 3.3 V or 5.0 V power ($V_{DD\_IO}$, $V_{DDA\_ADC}$, $V_{DDA\_PLL}$) and ground ($V_{SS\_IO}$, $V_{SSA\_ADC}$, $V_{DDA\_ADC}$) pins must always be connected to the external 3.3V or 5.0V supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Data based on $T_A$=25°C.
4. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.12: 10-bit ADC characteristics on page 72*.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

### 6.2.3 Thermal characteristics

**Table 9. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

Subject to general operating conditions for $V_{DD\_IO}$, and $T_A$

**Table 15. Single supply typical power consumption in Run, WFI, Slow and Slow-WFI modes**

| Symbol | Para meter | Conditions | 3.3V typ(1) | 5V typ(2) | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ (3) | Supply current in RUN mode(4) | Clocked by OSC4M with PLL multiplication, all peripherals enabled in the MRCC_PLCKEN register:<br>$f_{HCLK}$=60 MHz, $f_{PCLK}$=30 MHz<br>$f_{HCLK}$=56 MHz, $f_{PCLK}$=28 MHz<br>$f_{HCLK}$=48 MHz, $f_{PCLK}$=24 MHz<br>$f_{HCLK}$=32 MHz, $f_{PCLK}$=32 MHz<br>$f_{HCLK}$=16 MHz, $f_{PCLK}$=16 MHz<br>$f_{HCLK}$=8 MHz, $f_{PCLK}$=8 MHz | <br>80<br>75<br>65<br>59<br>34<br>20 | <br>82<br>77<br>67<br>61<br>37<br>22 | mA |
| | | Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register:<br>$f_{HCLK}$=60 MHz, $f_{PCLK}$=30 MHz<br>$f_{HCLK}$=56 MHz, $f_{PCLK}$=28 MHz<br>$f_{HCLK}$=48 MHz, $f_{PCLK}$=24 MHz<br>$f_{HCLK}$=32 MHz, $f_{PCLK}$=32 MHz<br>$f_{HCLK}$=16 MHz, $f_{PCLK}$=16 MHz<br>$f_{HCLK}$=8 MHz, $f_{PCLK}$=8 MHz | <br>65<br>60<br>54<br>42<br>22<br>16 | <br>67<br>62<br>55<br>44<br>24<br>18 | mA |
| | Supply current in WFI mode(4) | Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register:<br>$f_{HCLK}$=60 MHz, $f_{PCLK}$=30 MHz(5)<br>$f_{HCLK}$=56 MHz, $f_{PCLK}$=28 MHz(5)<br>$f_{HCLK}$=48 MHz, $f_{PCLK}$=24 MHz(5)<br>$f_{HCLK}$=32 MHz, $f_{PCLK}$=32 MHz(6)<br>$f_{HCLK}$=16 MHz, $f_{PCLK}$= 16 MHz (6)<br>$f_{HCLK}$= 8 MHz, $f_{PCLK}$= 8 MHz(6) | <br>62<br>59<br>53<br>22<br>13<br>10 | <br>63<br>60<br>54<br>23<br>15<br>11 | mA |
| | Supply current in SLOW mode(4) | Clocked by FREEOSC: $f_{HCLK}$=$f_{PCLK}$=~5 MHz,<br>Clocked by OSC4M: $f_{HCLK}$=$f_{PCLK}$=4 MHz<br>Clocked by LPOSC: $f_{HCLK}$=$f_{PCLK}$=~300 kHz<br>Clocked by OSC32K: $f_{HCLK}$=$f_{PCLK}$=32.768 kHz | 9<br>8<br>3.65<br>3.5 | 10<br>9<br>3.9<br>4.2 | mA |
| | Supply current in SLOW-WFI mode(4)(7) | Clocked by FREEOSC: $f_{HCLK}$=$f_{PCLK}$=~5 MHz<br>Clocked by OSC4M: $f_{HCLK}$=$f_{PCLK}$=4 MHz<br>Clocked by LPOSC: $f_{HCLK}$=$f_{PCLK}$=~300 kHz<br>Clocked by OSC32K: $f_{HCLK}$=$f_{PCLK}$=32.768 kHz | 3.5<br>3.1<br>1.15<br>0.98 | 4.0<br>3.75<br>1.65<br>1.5 | mA |

1. Typical data based on $T_A$=25° C and $V_{DD\_IO}$=3.3V.
2. Typical data based on $T_A$=25° C and $V_{DD\_IO}$=5.0V.
3. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4 on page 36*.
4. Single supply scheme see *Figure 14*.
5. Parameter setting BURST=1, WFI_FLASHEN=1
6. Parameter setting BURST=0, WFI_FLASHEN=0
7. Parameter setting WFI_FLASHEN=0, OSC4MOFF=1

**Table 16. Dual supply supply typical power consumption in Run, WFI, Slow and Slow-WFI modes**

To calculate the power consumption in Dual supply mode, refer to the values given in *Table 15*. and consider that this consumption is split as follows:

$I_{DD(single\ supply)} \sim I_{DD(dual\ supply)} = I_{DD\_V18} + I_{DD(VDD\_IO)}$

For 3.3V range: $I_{DD(VDD\_IO)}$ ~ 1 to 2 mA

For 5V range: $I_{DD(VDD\_IO)}$ ~ 2 to 3 mA

Therefore most of the consumption is sunk on the $V_{18}$ power supply

This formula does not apply in STOP and STANDBY modes, refer to *Table 17*.

Subject to general operating conditions for $V_{DD\_IO}$, and $T_A$

**Table 17. Typical power consumption in STOP and STANDBY modes**

| Symbol | Parameter | Conditions | | 3.3V Typ(1) | 5V Typ(2) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$(3) | Supply current in STOP mode(4) | LP_PARAM bits: ALL OFF(5) | | 12 | 15 | µA |
| | | LP_PARAM bits : MVREG ON, OSC4M OFF, FLASH OFF(6) | | 130 | 135 | |
| | | LP_PARAM bits: MVREG ON, OSC4M ON , FLASH OFF(6) | | 1950 | 1930 | |
| | | LP_PARAM bits: MVREG ON, OSC4M OFF, FLASH ON (6) | | 630 | 635 | |
| | | LP_PARAM bits: MVREG ON, OSC4M ON, FLASH ON (6) | | 2435 | 2425 | |
| | Supply current in STOP mode(7) | LPPARAM bits: ALL OFF, with $V_{18}$=1.8 V | $I_{DD\_V18}$<br>$I_{DD\_V33}$ | 5<br><1 | 5<br><1 | µA |
| | | LP_PARAM bits: OSC4M ON, FLASH OFF | $I_{DD\_V18}$<br>$I_{DD\_V33}$ | 410<br>1475 | 410<br>1435 | |
| | | LP_PARAM bits: OSC4M OFF, FLASH ON | $I_{DD\_V18}$<br>$I_{DD\_V33}$ | 550<br><1 | 550<br>1 | |
| | | LP_PARAM bits: OSC4M ON, FLASH ON | $I_{DD\_V18}$<br>$I_{DD\_V33}$ | 910<br>1475 | 910<br>1445 | |
| | Supply current in STANDBY mode(4) | RTC OFF | | 11 | 14 | µA |
| | | RTC ON clocked by OSC32K | | 14 | 18 | |

1. Typical data are based on $T_A$=25°C, $V_{DD\_IO}$=3.3 V and $V_{18}$=1.8 V unless otherwise indicated in the table.
2. Typical data are based on $T_A$=25°C, $V_{DD\_IO}$=5.0 V and $V_{18}$=1.8 V unless otherwise indicated in the table.
3. The conditions for these consumption measurements are described at the beginning of *Section 6.3.4 on page 36*.
4. Single supply scheme see *Figure 12*.
5. In this mode, the whole digital circuitry is powered internally by the LPVREG at approximately 1.4 V, which significantly reduces the leakage currents.
6. In this mode, the whole digital circuitry is powered internally by the MVREG at 1.8 V.
7. Dual supply scheme see *Figure 13*.

difference between N+1 consecutive clock rising edges and $T_{min}$ is the minimum time difference between N+1 consecutive clock rising edges.

N should be kept sufficiently large to have a long term jitter (ex: thousands).

For N=1, this becomes the single period jitter.

See *Figure 23*

- Cycle-to-cycle jitter (N period jitter)

  This corresponds to the time variation between adjacent cycles over a random sample of adjacent clock cycles pairs. Jitter(cycle-to-cycle) = Max(Tcycle n- Tcycle n-1) for n=1 to N.

  See *Figure 24*

**Figure 23. Self-referred jitter (single and long term)**

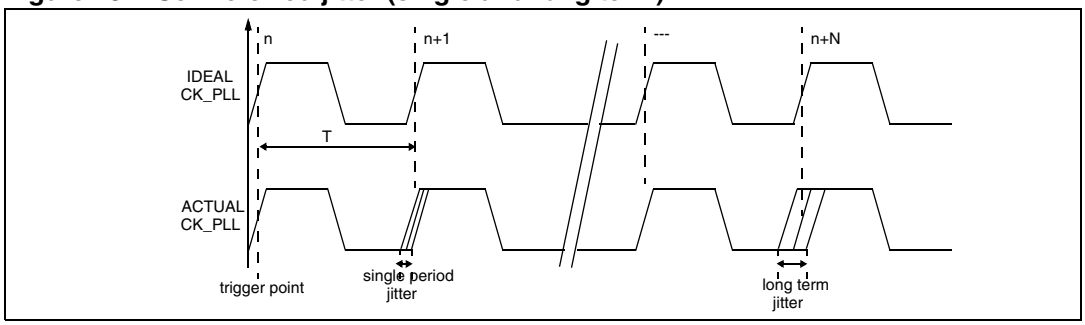
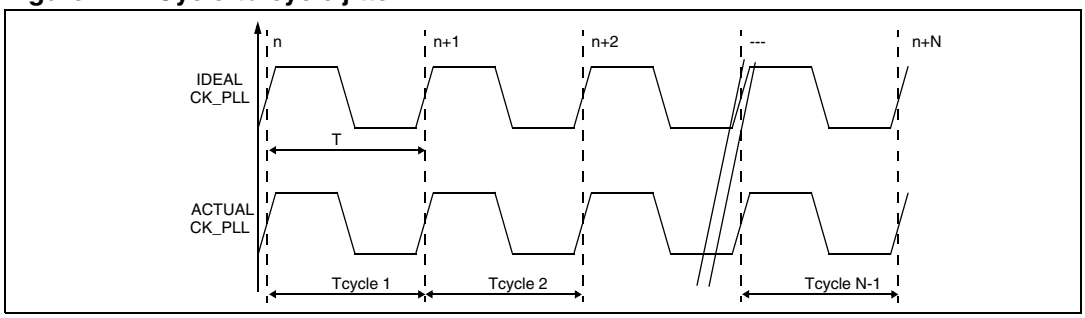



**Figure 24. Cycle-to-cycle jitter**



### Static and dynamic latch-up

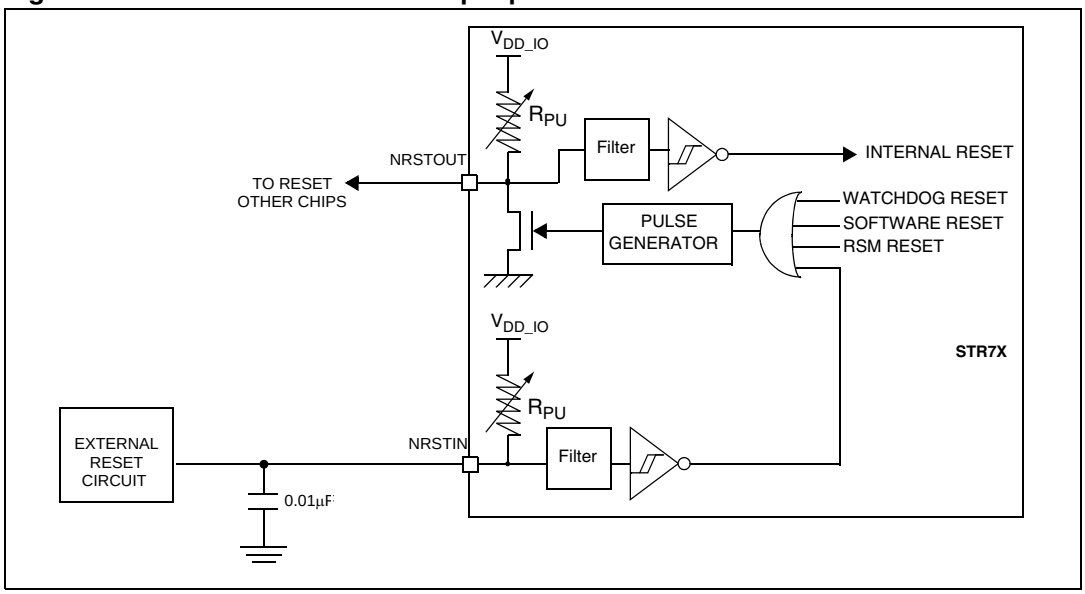
- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

**Table 31. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class(1) |
|---|---|---|---|
| LU | Static latch-up class | $T_A$=+25° C<br>$T_A$=+85° C<br>$T_A$=+105° C | Class A |
| DLU | Dynamic latch-up class | $V_{DD}$= 5.5 V, $f_{OSC4M}$=4 MHz,<br>$f_{CK\_SYS}$=32 MHz, $T_A$=+25° C | Class A |

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

**Figure 27. Recommended NRSTIN pin protection**




1. The user must ensure that the level on the NRSTIN pin can go below the $V_{IL(NRSTIN)}$ max. level specified in *NRSTIN and NRSTOUT pins on page 58*. Otherwise the reset will not be taken into account internally.

## SSP synchronous serial peripheral in slave mode (SPI or TI mode)

Subject to general operating conditions with $C_L \approx 45$ pF

**Table 39. SSP slave mode characteristics(1)**

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SPI clock frequency | | SSP0 | | 2.66 MHz ($f_{PLCK}$/12) | MHz |
| | | | SSP1 | | | |
| $t_{su(NSS)}$ | NSS input setup time w.r.t SCK first edge | | SSP0 | 0 | | ns |
| | | | SSP1 | 0 | | |
| $t_{h(NSS)}$ | NSS input hold time w.r.t SCK last edge | | SSP0 | $t_{PCLK}$+15ns | | |
| | | | SSP1 | $t_{PCLK}$+15ns | | |
| $t_{NSSLQV}$ | NSS low to Data Output MISO valid time | | SSP0 | $2t_{PCLK}$ | $3t_{PCLK}$+30 ns | |
| | | | SSP1 | $2t_{PCLK}$ | $3t_{PCLK}$+30 ns | |
| $t_{NSSLQZ}$ | NSS low to Data Output MISO invalid time | | SSP0 | $2t_{PCLK}$ | $3t_{PCLK}$+15 ns | |
| | | | SSP1 | $2t_{PCLK}$ | $3t_{PCLK}$+15 ns | |
| $t_{SCKQV}$ | SCK trigger edge to data output MISO valid time | | SSP0 | | 15 | |
| | | | SSP1 | | 30 | |
| $t_{SCKQX}$ | SCK trigger edge to data output MISO invalid time | | SSP0 | $2t_{PCLK}$ | | |
| | | | SSP1 | $2t_{PCLK}$ | | |
| $t_{su(MOSI)}$ | MOSI setup time w.r.t SCK sampling edge | | SSP0 | 0 | | |
| | | | SSP1 | 0 | | |
| $t_{h(MOSI)}$ | MOSI hold time w.r.t SCK sampling edge | | SSP0 | $3t_{PCLK}$+15 ns | | |
| | | | SSP1 | $3t_{PCLK}$+15 ns | | |

1. Data based on characterisation results, not tested in production.

**Figure 33. SPI configuration, slave mode with CPHA=0, single transfer**

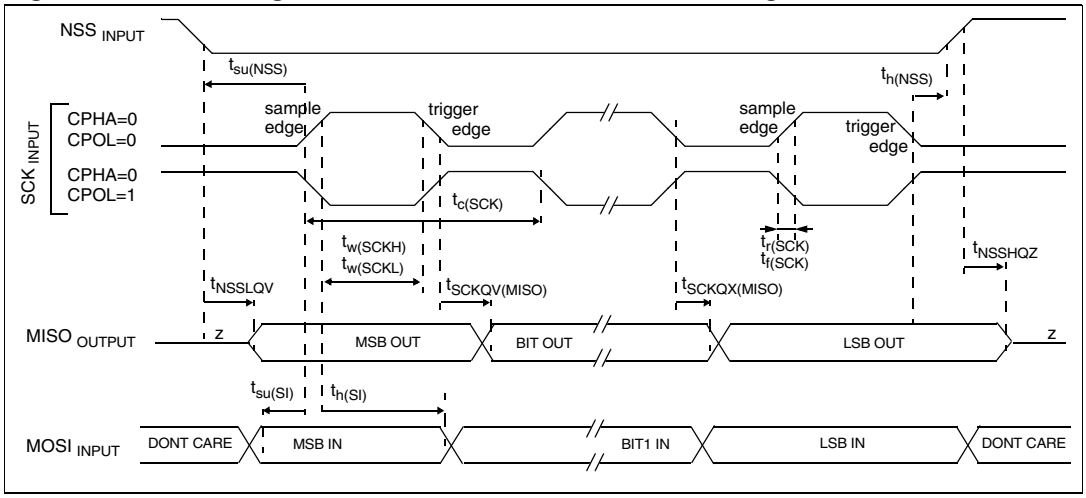


**Figure 34. SPI configuration - slave mode with CPHA=0, continuous transfer**

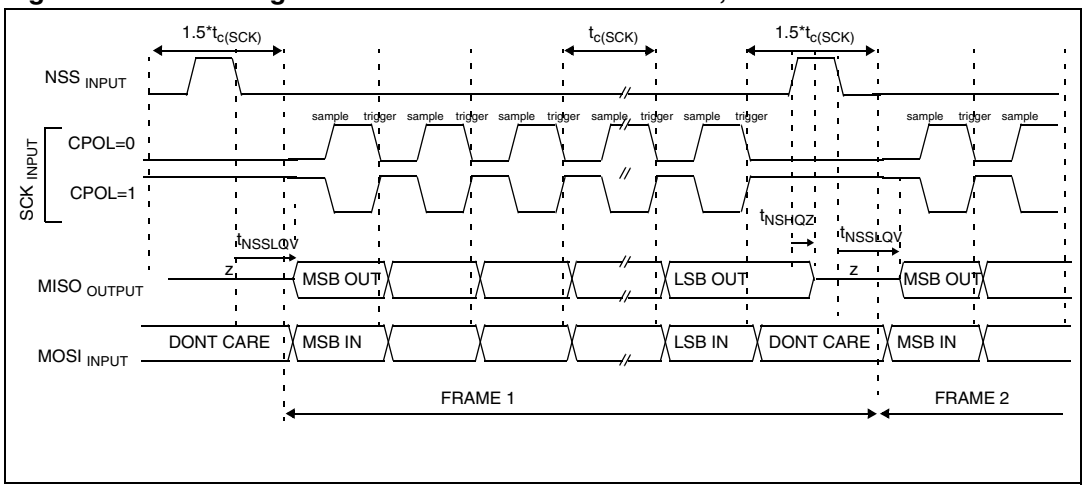



**Figure 35. SPI configuration, slave mode with CPHA=1, single transfer**

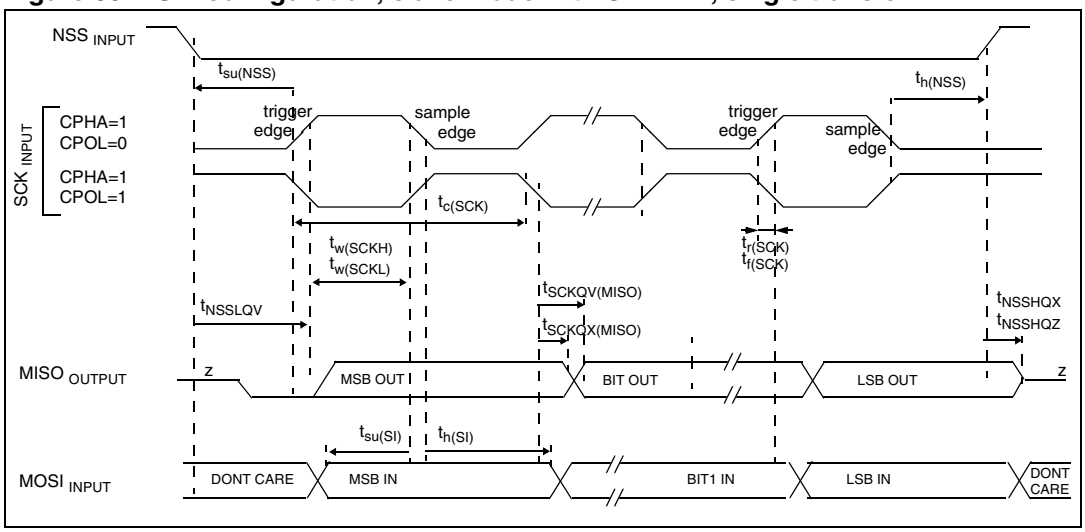



**Figure 36. SPI configuration - slave mode with CPHA=1, continuous transfer**

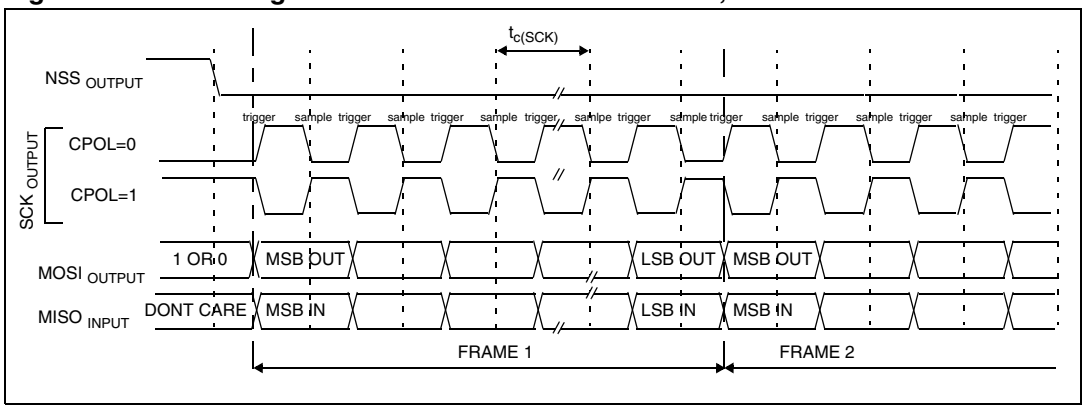


**Figure 37. TI configuration - slave mode, single transfer**

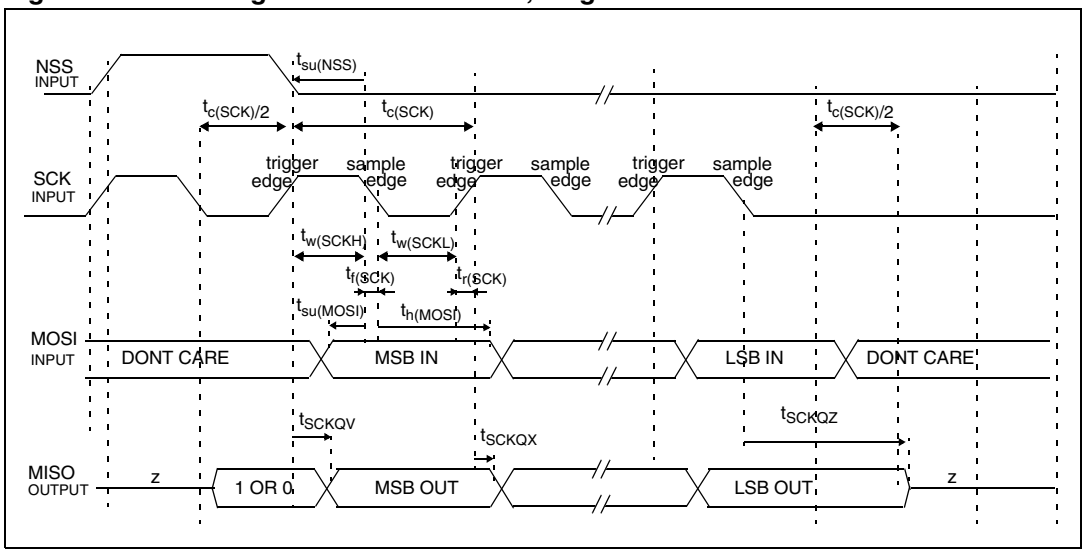
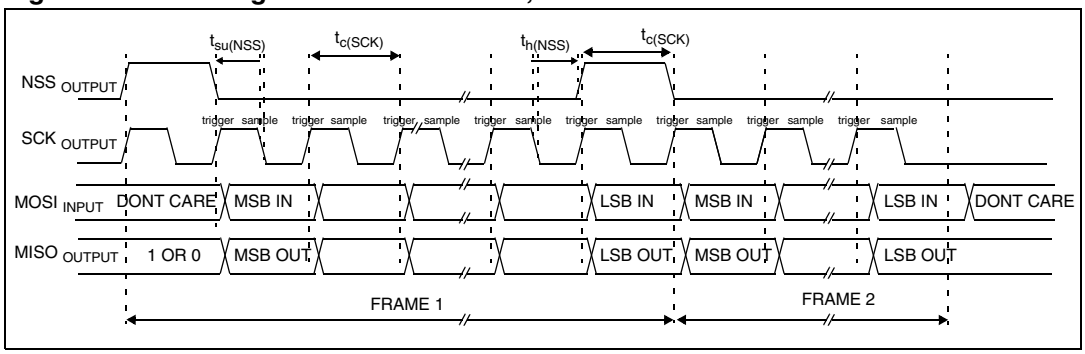



**Figure 38. TI configuration - slave mode, continuous transfer**



## SMI - serial memory interface

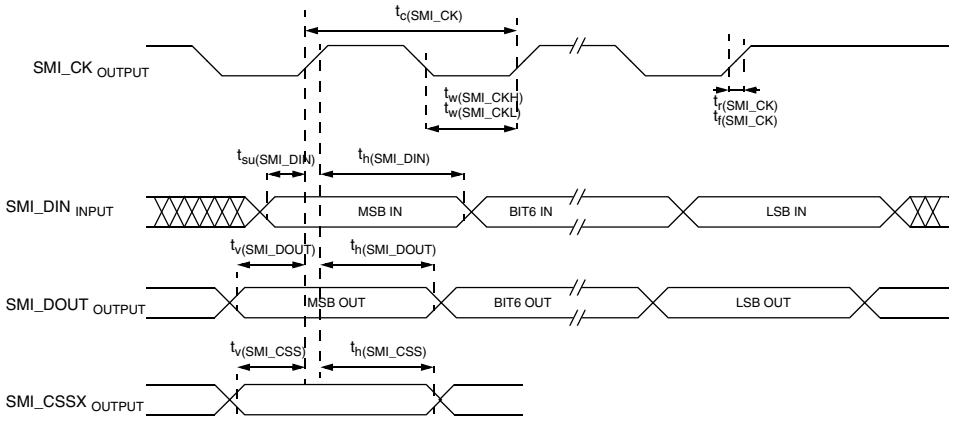
Subject to general operating conditions with $C_L \approx 30$ pF.

**Table 40. SMI characteristics(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{SMI\_CK}$ | SMI clock frequency | | 32(2)(3) | MHz |
| | | | 48(4) | |
| $t_{r(SMI\_CK)}$ | SMI clock rise time | | 10 | ns |
| $t_{f(SMI\_CK)}$ | SMI clock fall time | | 8 | |
| $t_{v(SMI\_DOUT)}$ | Data output valid time | | 10 | |
| $t_{h(SMI\_DOUT)}$ | Data output hold time | | 0 | |
| $t_{v(SMI\_CSSx)}$ | CSS output valid time | | 10 | |
| $t_{h(SMI\_CSSx)}$ | CSS output hold time | | 0 | |
| $t_{su(SMI\_DIN)}$ | Data input setup time | 0 | | |
| $t_{h(SMI\_DIN)}$ | Data input hold time | 5 | | |

1. Data based on characterisation results, not tested in production.
2. Max. frequency = $f_{PCLK}/2 = 64/2 = 32$ MHz.
3. Valid for all temperature ranges: -40 to 105 °C, with 30 pF load capacitance.
4. Valid up to 60 °C, with 10 pF load capacitance.

**Figure 39. SMI timing diagram**




## I²C - Inter IC control interface

Subject to general operating conditions for $V_{DD\_IO}$, $f_{PCLK}$, and $T_A$ unless otherwise specified.

The I²C interface meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

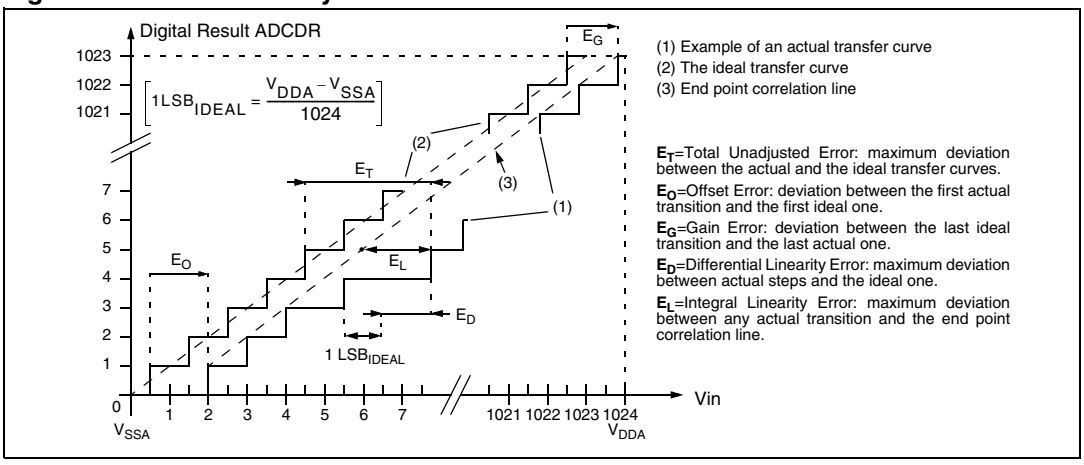
**Restriction:** The I/O pins which SDA and SCL are mapped to are not “True” Open-Drain: when configured as open-drain, the PMOS connected between the I/O pin and $V_{DD\_IO}$ is disabled, but it is still present. Also, there is a protection diode between the I/O pin and $V_{DD\_IO}$. Consequently, when using this I²C in a multi-master network, it is

**Table 47. ADC accuracy**

| ADC accuracy with $f_{CK\_SYS}$ = 20 MHz, $f_{ADC}$=8 MHz, $R_{AIN}$ < 10 kΩ<br>This assumes that the ADC is calibrated(1) | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Typ** | **Max** | **Unit** |
| $\|E_T\|$ | Total unadjusted error (2) (3) | $V_{DDA\_ADC}$=3.3 V | 1 | 1.2 | LSB |
| | | $V_{DDA\_ADC}$=5.0 V | 1 | 1.2 | |
| $\|E_O\|$ | Offset error(2) (3) | $V_{DDA\_ADC}$=3.3 V | 0.15 | 0.5 | |
| | | $V_{DDA\_ADC}$=5.0 V | 0.15 | 0.5 | |
| $E_G$ | Gain Error (2) (3) | $V_{DDA\_ADC}$=3.3 V | -0.8 | -0.2 | |
| | | $V_{DDA\_ADC}$=5.0 V | -0.8 | -0.2 | |
| $\|E_D\|$ | Differential linearity error(2) (3) | $V_{DDA\_ADC}$=3.3 V | 0.7 | 0.9 | |
| | | $V_{DDA\_ADC}$=5.0 V | 0.7 | 0.9 | |
| $\|E_L\|$ | Integral linearity error (2) (3) | $V_{DDA\_ADC}$=3.3 V | 0.6 | 0.8 | |
| | | $V_{DDA\_ADC}$=5.0 V | 0.6 | 0.8 | |

1. Calibration is needed once after each power-up.
2. Refer to *ADC accuracy vs. negative injection current on page 73*
3. ADC Accuracy vs. MCO (Main Clock Output): the ADC accuracy can be significantly degraded when activating the MCO on pin P0.01 while converting an analog channel (especially those which are close to the MCO pin). To avoid this, when an ADC conversion is launched, it is strongly recommended to disable the MCO.

**Figure 44. ADC accuracy characteristics**



# 8 Order codes

**Table 49. Order codes**

| Order code | Flash Prog. Memory (Bank 0) Kbytes | Package | CAN Periph | USB Periph | Nominal Temp. Range ($T_A$) |
|---|---|---|---|---|---|
| STR750FV0T6 | 64 | LQFP100 14x14 | Yes | Yes | -40 to +85°C |
| STR750FV1T6 | 128 | | | | |
| STR750FV2T6 | 256 | | | | |
| STR750FV0H6 | 64 | LFBGA100 10x10 | | | |
| STR750FV1H6 | 128 | | | | |
| STR750FV2H6 | 256 | | | | |
| STR751FR0T6 | 64 | LQFP64 10x10 | - | Yes | -40 to +85°C |
| STR751FR1T6 | 128 | | | | |
| STR751FR2T6 | 256 | | | | |
| STR751FR0H6 | 64 | LFBGA64 8x8 | | | |
| STR751FR1H6 | 128 | | | | |
| STR751FR2H6 | 256 | | | | |
| STR752FR0T6 | 64 | LQFP64 10x10 | Yes | - | -40 to +85°C |
| STR752FR1T6 | 128 | | | | |
| STR752FR2T6 | 256 | | | | |
| STR752FR0H6 | 64 | LFBGA64 8x8 | | | |
| STR752FR1H6 | 128 | | | | |
| STR752FR2H6 | 256 | | | | |
| STR752FR0T7 | 64 | LQFP64 10x10 | Yes | - | -40 to +105°C |
| STR752FR1T7 | 128 | | | | |
| STR752FR2T7 | 256 | | | | |
| STR752FR0H7 | 64 | LFBGA64 8x8 | | | |
| STR752FR1H7 | 128 | | | | |
| STR752FR2H7 | 256 | | | | |
| STR755FR0T6 | 64 | LQFP64 10x10 | - | - | -40 to +85°C |
| STR755FR1T6 | 128 | | | | |
| STR755FR2T6 | 256 | | | | |
| STR755FR0H6 | 64 | LFBGA64 8x8 | | | |
| STR755FR1H6 | 128 | | | | |
| STR755FR2H6 | 256 | | | | |

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