Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	489 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86d990hz008sg

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters
532 Race Street
San Jose, CA 95126-3432
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

Document Disclaimer

List of Figures

  - Three timer interrupts
  - One low-battery detector flag

Operating Characteristics

- 8-MHz operation
- 3.0 V to 5.5 V operating voltage (Z86D990/Z86D991)
- 2.3 V to 5.5 V operating voltage (Z86L990/Z86L991)
- Low power consumption with three standby modes:
  - Stop
  - Halt
  - Low Voltage Standby
- Low-battery detection flag
- Low-voltage protection circuit (also known as V_{BO}, or voltage brownout, circuit)
- Watch-dog timer and power-on reset circuits

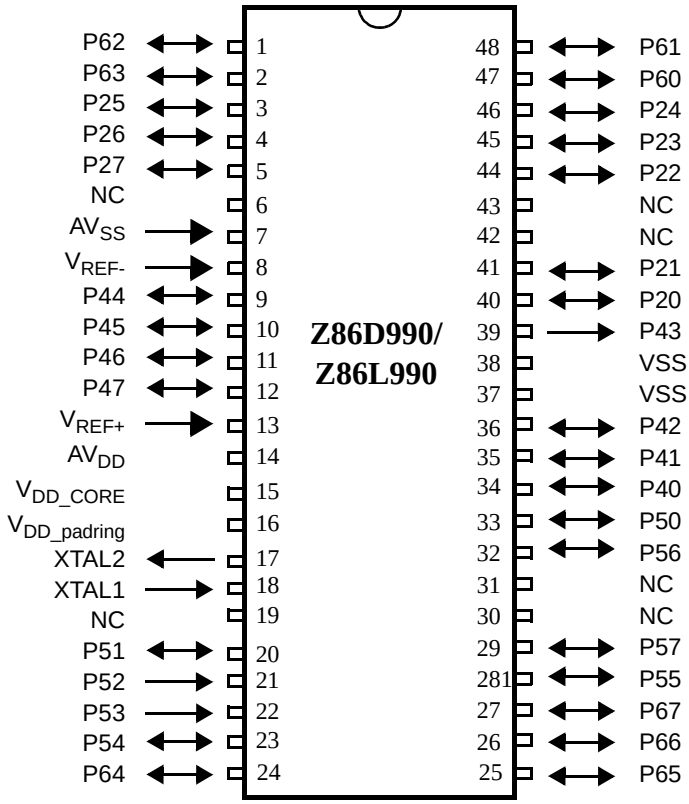
User-Programmable Option Bits

- Clock source—RC/other (LC, resonator, or crystal)
- Watch-dog timer permanently enable
- 32-kHz crystal
- Port 20–27 pull-up resistive transistor
- Port 40–42 pull-up resistive transistor
- Port 44–47 pull-up resistive transistor
- Port 50–51 pull-up resistive transistor
- Port 54–57 pull-up resistive transistor
- Port 60–63 pull-up resistive transistor (not available in Z86D991/Z86L991)
- Port 64–67 pull-up resistive transistor (not available in Z86D991/Z86L991)
- P43 high impedance in STOP mode (available in OTP only)

  Force P43 to output a 1 in the open-drain configuration

Pin Descriptions

Figure 2 through Figure 4 show the pin names and locations.



Notes:

1. Both V_{SS} pins must be connected to ground.
2. NC is no connection to the die.
3. AV_{DD} must be connected to V_{DD_CORE} and a 10-µF capacitor for good A/D conversion.
4. Power must be connected to $V_{DD\_padring}$. Current passes to V_{DD_CORE} through the internal power filter.

Figure 2. 48-Pin SSOP Pin Assignments

Table 2. Pin Descriptions (Continued)

Symbol	Pin # 28 PDIP/SOIC	40 PDIP	48 SSOP	Direction	Description
P41	20	30	35	I/O	Port 4 Bit 1, T16 Output
P42	21	31	36	I/O	Port 4 Bit 2
P43	23	33	39	Output	T8/T16 Output, Controlled current output
P44	4	8	9	I/O	Port 4 Bit 4, A/D Channel 0*
P45	5	9	10	I/O	Port 4 Bit 5, A/D Channel 1*
P46	6	10	11	I/O	Port 4 Bit 6, A/D Channel 2*
P47	7	11	12	I/O	Port 4 Bit 7, A/D Channel 3*
P50, CREF1	18	28	33	I/O	Port 5 Bit 0, Comparator 1 reference
P51, CIN1	11	17	20	I/O	Port 5 Bit 1, Capture timer input, IRQ_2
P52, CIN2	12	18	21	Input	Port 5 Bit 2, Timer 1 timer input, IRQ_0
P53, CREF2	13	19	22	Input	Port 5 Bit 3, Comparator 2 reference, IRQ_1
P54	14	20	23	I/O	Port 5 Bit 4, High drive output
P55	15	25	28	I/O	Port 5 Bit 5, High drive output
P56	17	27	32	I/O	Port 5 Bit 6, Timer 1 output, High drive output
P57	16	26	29	I/O	Port 5 Bit 7, High drive output
P60		39	47	I/O	Port 6 Bit 0
P61		40	48	I/O	Port 6 Bit 1
P62		1	1	I/O	Port 6 Bit 2
P63		2	2	I/O	Port 6 Bit 3
P64		21	24	I/O	Port 6 Bit 4
P65		22	25	I/O	Port 6 Bit 5
P66		23	26	I/O	Port 6 Bit 6
P67		24	27	I/O	Port 6 Bit 7
XTAL1	10	16	18	Input	Crystal, Oscillator clock
XTAL2	9	15	17	Output	Crystal, Oscillator clock
AV_{DD}		13	14		Analog power supply
V_{DD_CORE}		13	15		Z8 core power supply
AV_{SS}		6	7		Analog ground
V_{Ref-}		7	8	Input	A/D converter lower reference
V_{Ref+}		12	13	Input	A/D converter upper reference
$V_{DD\_padring}$	8**	14	16		Power supply (pad ring)
V_{SS}	22**	32	37, 38		Ground

Notes: *A/D converter is not available in the 28-pin configuration.
**In the 28-pin configuration, all three (core, pad ring, and analog) powers are tied together.

Location (Hex)	
FFFF FF00	256 bytes **Executable RAM**
	Not Implemented
3FFF/7FFF (ROM)/(OTP) 000C	**PROGRAM MEMORY** Location of the first byte of the initial instruction executed after RESET
000B	IRQ_5 (lower byte)
000A	IRQ_5 (upper byte)
0009	IRQ_4 (lower byte)
0008	IRQ_4 (upper byte)
0007	IRQ_3 (lower byte)
0006	IRQ_3 (upper byte)
0005	IRQ_2 (lower byte)
0004	IRQ_2 (upper byte)
0003	IRQ_1 (lower byte)
0002	IRQ_1 (upper byte)
0001	IRQ_0 (lower byte)
0000	IRQ_0 (upper byte)

Figure 5. Program Memory Map

Z8 Standard Register File (Bank 0)

Bank 0 of the Z8 expanded register file architecture is known as the standard register file of the Z8. As shown in Figure 6, the Z8 standard register file consists of 16 groups of sixteen 8-bit registers known as Working Register (WR) groups. Working Register Group F contains various control and status registers. The lower half of Working Register Group 0 consists of I/O port registers (R0 to R7), the upper eight registers are available for use as general-purpose RAM registers. Working Register Group 1 through Group E of the standard register file are available to be used as general-purpose RAM registers. The user can use 233 bytes of general-purpose RAM registers in the standard Z8 register file (Bank 0).

start the interrupt process. However, the IPR does not have to be initialized for polled processing.

Interrupts must be globally enabled using the EI instruction. Setting bit 7 of the IMR is not sufficient. Subsequent to this EI instruction, interrupts can be enabled either by IMR manipulation or by use of the EI instruction, with equivalent effects.

Additionally, interrupts must be disabled by executing a DI instruction before the IPRs or IMRs can be modified. Interrupts can then be enabled by executing an EI instruction.

IRQ Software Interrupt Generation

IRQ can be used to generate software interrupts by specifying IRQ as the destination of any instruction referencing the Z8 Standard Register File. These Software Interrupts (SWIs) are controlled in the same manner as hardware-generated requests (the IPR and the IMR control the priority and enabling of each SWI level).

To generate a SWI, the request bit in the IRQ is set as follows:

```
OR    IRQ, #NUMBER
```

where the immediate data, *NUMBER*, has a 1 in the bit position corresponding to the appropriate level of the SWI.

For example, for an SWI on IRQ5, *NUMBER* has a 1 in bit 5. With this instruction, if the interrupt system is globally enabled, IRQ5 is enabled, and there are no higher priority pending requests, control is transferred to the service routine pointed to by the IRQ5 vector.

Reset Conditions

A system reset overrides all other operating conditions and puts the Z8 into a known state. The control and status registers are reset to their default conditions after a power-on reset (POR) or a Watch-Dog Timer (WDT) time-out while in RUN mode. The control and status registers are not reset to their default conditions after Stop Mode Recovery (SMR) while in HALT or STOP mode.

General-purpose registers are undefined after the device is powered up. Resetting the Z8 does not affect the contents of the general-purpose registers. The registers keep their most recent value after any reset, as long as the reset occurs in the specified V_{CC} operating range. Registers do not keep their most recent state from a V_{LV} reset, if V_{CC} drops below V_{RAM} (see Table 54 on page 87).

Following a reset (see Table 5), the first routine executed must be one that initializes the control registers to the required system configuration.

equivalent to a hardware POR reset. If the mask option of the permanently enabled watch-dog timer is selected, it runs when power up. If the option is not selected, the WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction.

The WDT instruction does not affect the Zero (Z), Sign (S), and Overflow (V) flags. Permanently enabled WDTs are always enabled, and the WDT instruction is used to refresh it. The WDT cannot be disabled after it has been initially enabled. The WDT is off during both HALT and STOP modes.

The WDT circuit is driven by an on-board RC oscillator. The time-out period for the WDT is fixed to a typical value (see Table 57 on page 90).

Power Management

In addition to the standard RUN mode, the Z8 supports three power-down modes to minimize device current consumption. The following three modes are supported:

- HALT
- STOP
- Low-Voltage Standby

Table 6 shows the status of the internal CPU clock (SCLK), the internal Timer clock (TCLK), the external oscillator, and the Watch-Dog Timer during the RUN mode and three low-power modes.

Table 6. Clock Status in Operating Modes

Operating Mode	SCLK	TCLK	External OSC	WDT*
RUN	On	On	On	On
HALT	Off	On	On	Off
STOP	Off	Off	Off	Off
Low-Voltage Standby	Off	Off	Off	Off
Note: * When WDT is enabled by the mask option bit				

Using the Power-Down Modes

In order to enter HALT or STOP mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. You can flush the

Controlled Current Output

P43 is an open-drain output-only pin on the Z86D990/D991, but it can be configured as output or Tristate High Impedance on the Z86L990/L991. To function properly, Bit 3 of P4M must be set to zero to configure the pin as an open-drain output. For the Z86L990/L991 after reset, P43 defaults to Tristate High Impedance while the Z86D990/D991 P43 is always configured as output. The data at Port 4 must be initialized as it is undefined at power-on reset.

The current output is a controlled current source that is controlled by the output of the value of P43 (see Table 9). P43 *cannot* be configured as input, and if P43 is read, P43 always returns the state of the output value (1 for no sink and 0 for sink).

P43 uses internal current reference and will draw current if it outputs a low logic even without external connection. This applies to both Run mode and Stop mode.

Table 9. Current Sink Pad P43 Specifications (Preliminary)

Parameter	Min	Max	Conditions
Rise time		0.4 µ	LED load
Fall time		0.02 µ	LED load
V_{outmin}		0.54 V	@27C
Comparator response		0.2 µ	
Regulated current	80 mA	120 mA	
Internal resistance		80 Ω	

The pad driver can function in two modes:

- controlled current output, when the voltage on the pad is over a minimum value

$$V_{pad} > V_{outmin}$$

- resistive pull down when the driver cannot regulate the current; in this mode, the gate of the NMOS pull down is raised to the power rail.

The I-V characteristics of the pad are presented in Figure 17.

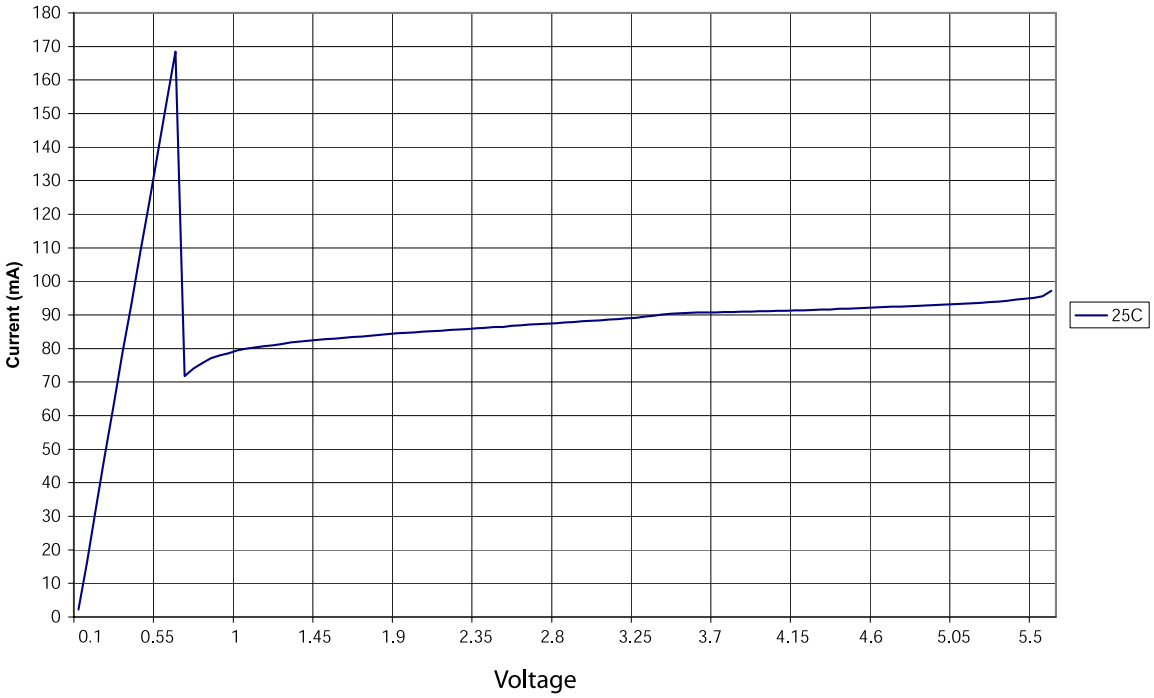


Figure 17. I-V Characteristics for the Current Sink Pad P43

The CPU reads the mode of the pad driver by reading bit number 2 from the LB register. This bit is the output of a Set-Reset flip-flop that sets whenever the voltage on the pad is lower than V_{outmin} and is reset by a CPU write to the respective register.

T1 Timer

The Z86D99/Z86L99 family provides one general-purpose 8-bit counter/timer, T_1, driven by its own 6-bit prescaler, PRE_1. The T_1 counter/timer is independent of the processor instruction sequence, which relieves software from time-critical operations such as interval timing and event counting.

The T_1 counter/timer operates in either single-pass or continuous mode. At the end-of-count, counting either stops or the initial value is reloaded and counting continues. Under software control, new values are loaded immediately or when the end-of-count is reached. Software also controls the counting mode, how the counter/timer is started or stopped, and the counter/timer's use of I/O lines. Both the counter and prescaler registers can be altered while the counter/timer is running.

The six most significant bits (D_2–D_7) of PRE_1 hold the prescaler count modulo, a value from 11 to 64 decimal. The prescaler register also contains control bits that specify T_1 counting modes. These bits also indicate whether the clock source for T_1 is internal or external.

The counter/timer T_1 (F2h) consists of an 8-bit down-counter, a write-only register that holds the initial count value, and a read-only register that holds the current count value (see Figure 18 on page 35). The initial value can range from 1 to 256 decimal (01h, 02h, ..., 00h). Figure 21 illustrates the counter/timer register.

R242 T1
Counter/Timer 1 Register
(F2h; Read/Write)

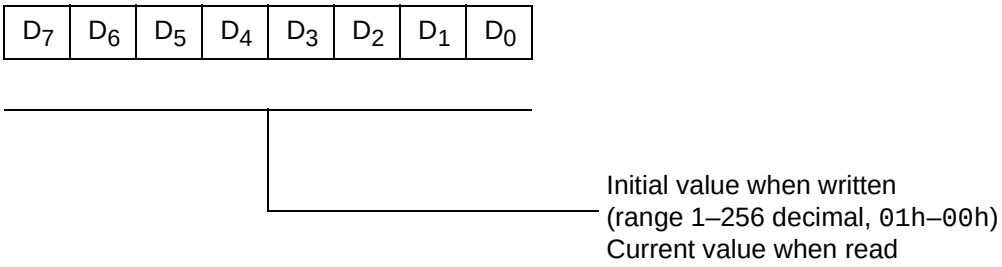


Figure 21. Counter/Timer 1 Register

Counter/Timer Operation

Under software control, T_1 is started and stopped using the Timer Mode register (F1h) bits D_2–D_3: a Load bit and an Enable Count bit. See Figure 22.

R241 TMR
Timer Mode Register
(F1h; Read/Write)

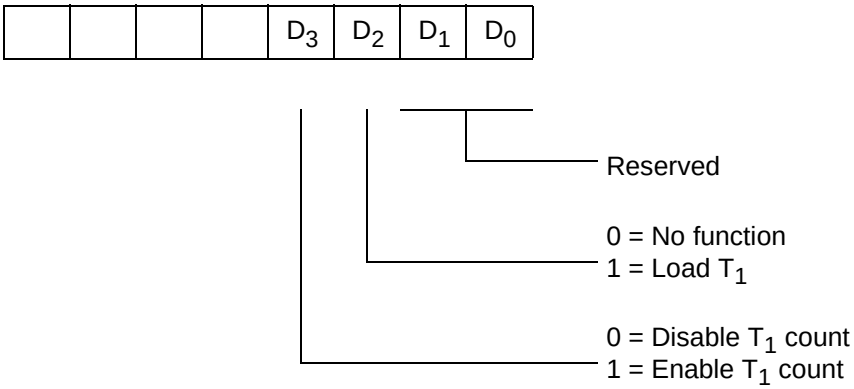


Figure 22. Timer Mode Register

The time interval (i) until end-of-count, is given by

i = t x p x v

where t is 8 divided by XTAL frequency, p is the prescaler value (1 – 64), and v is the counter/timer value (1 – 256). The prescaler and counter/timer are true divide-by-n counters.

T_{OUT} Modes

The Timer Mode register TMR (F1h) (Figure 25) is used in conjunction with the Port 5 Mode register P5M to configure $P5_6$ for T_{OUT} operation. In order for T_{OUT} to function, $P5_6$ must be defined as an output line by setting P5M bit D_6 to 0. Output is controlled by one of the counter/timers (T_0 or T_1) or the internal clock.

R241 TMR
Timer Mode Register
(F1h; Read/Write)

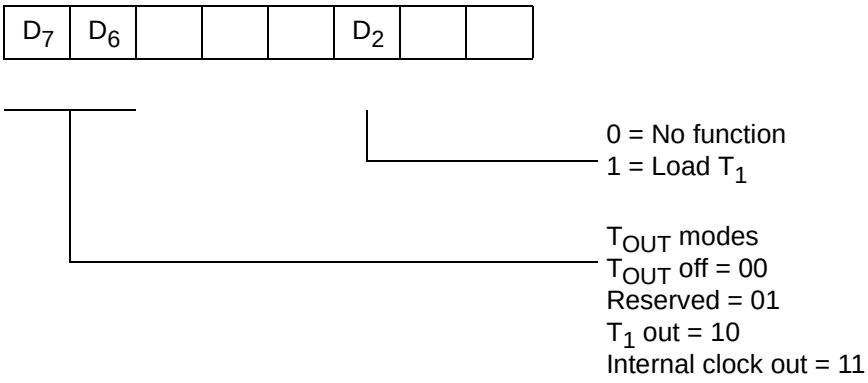


Figure 25. Timer Mode Register T_{OUT} Operation

The $P5_6$ output is selected by TMR bits D_7 and D_6. T_1 is selected by setting D_7 and D_6 to 1 and 0, respectively. The counter/timer T_{OUT} mode is turned off by setting TMR bits D_7 and D_6 both to 0, freeing $P3_6$ to be a data output line.

T_{OUT} is initialized to a logic 1 whenever the TMR Load bit D_2 is set to 1.

At end-of-count, the interrupt request line IRQ_5 clocks a toggle flip-flop. The output of this flip-flop drives the T_{OUT} line $P5_6$. In all cases, when the counter/timer reaches its end-of-count, T_{OUT} toggles to its opposite state (see Figure 26). If, for example, the counter/timer is in continuous counting mode, T_{OUT} has a 50% duty cycle output. You can control the duty cycle by varying the initial values after each end-of-count.

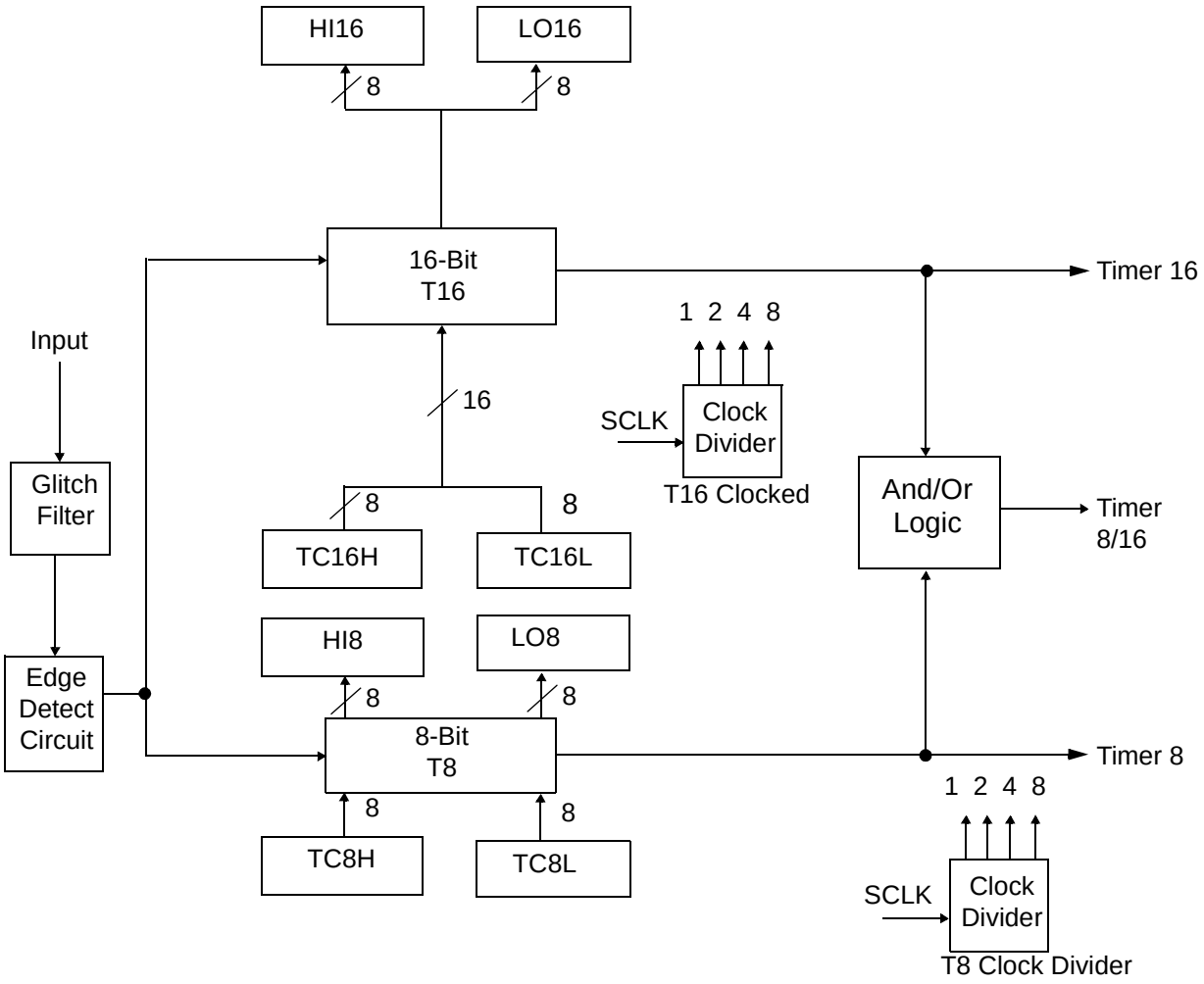


Figure 33. Counter/Timer Architecture

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If CTR1, D1 is 0, T8_OUT is 1. If CTR1, D1 is 1, T8_OUT is 0.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1 D1). If the initial value (CTR1 D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In single-pass mode (CTR0 D6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0 D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0 D1). In modulo-N mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. Then T8 loads a new count (if T8_OUT level is 0), TC8L is loaded; if T8_OUT is 1, TC8H is loaded.

Note: Do not use the same instructions for stopping the counter/timers and setting the status bits. Two successive commands are necessary—the first command for stopping counter/timers and the second command for resetting the status bits—because one counter/timer clock interval must complete for the initiated event to actually occur.

T8 Demodulation Mode

Program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both, depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both, depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If T8 is a positive edge, data is placed in LO8. If T8 is a negative edge, data is placed in H18. One of the edge-detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with TC8H and starts counting again. If T8 reaches 0, the time-out status bit (CTR0 D5) is set, and an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from FFh (see Figure 35).

Table 15. FLAGS Register [Group/Bank F0h, Register C (R252)] (Continued)

____3___	Decimal Adjust Flag (D)	R/W	1 0	Used for BCD arithmetic—after a subtraction, the flag is set to 1; following an addition, it is cleared to 0
_____2__	Half Carry Flag (H)	R/W	1 0	Set to 1, whenever an addition generates a “carry out” of bit position 3 (overflow) of an accumulator; or subtraction generates a “borrow into” bit 3
______1_	User Flag (F2)	R/W	1 0	User definable
_______0	User Flag (F1)	R/W	1 0	User definable

Register Pointer (RP)

Z8 instructions can access registers directly or indirectly using either a 4-bit or 8-bit address field. The upper nibble of the Register Pointer, as described in Table 16, contains the base address of the active Working Register GROUP. The lower nibble contains the base address of the Expanded Register File BANK. When using 4-bit addressing, the 4-bit address of the working register (r0 to rF) is combined with the upper nibble of the Register Pointer (identifying the WR GROUP), thus forming the 8-bit actual address.

Table 16. RP Register [Group/Bank F0h, Register D (R253)]

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit/Field	**Working Register Group**				**Expanded Register File Bank**			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	**Bit/Field**	**R/W**	**Value**	**Description**
7654_____	Working Register Group Pointer	R/W	X	Identifies 1 of 16 possible WR Groups, each containing 16 Working Registers
_____3210	Expanded Register File Bank Pointer	R/W	X	Identifies 1 of 16 possible ERF Banks; only Banks 0, D, and F are valid for the Z86D99/Z86L99 family

Interrupt Request Register

The IRQ, as described in Table 23, is a read/write register that stores the interrupt requests for both vectored and polled interrupts. When an interrupt request is made by any of the six interrupts, the corresponding bit in the IRQ is set to 1.

Table 23. IRQ (Group/Bank 0Fh, Register A)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Interrupt Edge		Set IRQ5	Set IRQ4	Set IRQ3	Set IRQ2	Set IRQ1	Set IRQ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76_____	Interrupt Edge Trigger	R/W	11 10 01 00	P51 Rise/FallingP52 Rise/Falling P51 Rising P52 Falling P51 FallingP52 Rising P51 FallingP52 Falling
__5_____	Set IRQ_5	R R W W	1 0 1 0	IRQ_5 Inactive IRQ_5 Active Set IRQ_5 Reset IRQ_5
___4____	Set IRQ_4	R R W W	1 0 1 0	IRQ_4 Inactive IRQ_4 Active Set IRQ_4 Reset IRQ_4
____3___	Set IRQ_3	R R W W	1 0 1 0	IRQ_3 Inactive IRQ_3 Active Set IRQ_3 Reset IRQ_3
_____2__	Set IRQ_2	R R W W	1 0 1 0	IRQ_2 Inactive IRQ_2 Active Set IRQ_2 Reset IRQ_2
______1_	Set IRQ_1	R R W W	1 0 1 0	IRQ_1 Inactive IRQ_1 Active Set IRQ_1 Reset IRQ_1
_______0	Set IRQ_0	R R W W	1 0 1 0	IRQ_0 Inactive IRQ_0 Active Set IRQ_0 Reset IRQ_0

Table 35. TMR Register [Group/Bank F0h, Register 1 (R241)] (Continued)

_____2__	T_1 Load	R/W	1 0	Load T_1 No effect
______10	Reserved	R W	1 X	Always reads 11 No effect

T1 Prescale Register (PRE1)

The T1 prescaler consists of an 8-bit register and a 6-bit down-counter. The six most significant bits (D2–D7) of PRE1 hold the prescaler's count modulo, a value from 1 to 64 decimal, as shown in Table 36. The prescale register also contains control bits that specify the counting mode and clock source for T1.

Table 36. PRE1 Register [Group/Bank F0h, Register 3 (R243)]

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit/Field	**Prescaler_Modulo**						**Clock_ Source**	**Count_ Mode**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	**Bit/Field**	**R/W**	**Value**	**Description**
765432__	Prescaler Modulo	R/W	Data	Range: 1 to 64 Decimal
_____1_	Clock Source	R/W	1 0	T_1 Internal T_1 External (T_{IN} on P52)
_____0	Count Mode	R/W	1 0	T_1 Modulo-n T_1 Single Pass

Timer Control Registers—T8 and T16 Timers

One of the unique features of the Z86D99/Z86L99 family is a special timer architecture to automate the generation and reception of complex pulses or signals. This timer architecture consists of one programmable 8-bit counter timer with two capture registers and two load registers and a programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair and their associated control registers. These counter/timers can work independently or can be combined together using a number of user-selectable modes governed by the T8/T16 control registers.

T8/T16 Control Register A (CTR1)

The T8/T16 Control Register A controls the functions in common with both the T_8 and T_{16} counter/timers. The T_8 and T_{16} counter/timers have two primary modes of operation: Transmit Mode and Demodulation Mode. Transmit Mode is used for generating complex waveforms. The Transmit Mode has two submodes: Normal Mode and Ping-Pong Mode. The settings for CTR1 in Transmit Mode are given in Table 37.

Table 37. CTR1 Register (In Transmit Mode) (Group/Bank 0Dh, Register 1)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Mode	P43 Out	T8/T16_Logic		Transmit_ Submode		Initial_ T8_Out	Initial_ T16_ Out
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
7_____	Mode	R/W	1 0	Demodulation Transmit
_6_____	P43_Out	R/W	1 0	P43 configured as T8/T16 Output P43 configured as I/O
__54____	T_8/T_{16} Logic	R/W	11 10 01 00	NAND NOR OR AND
____32__	Transmit_ Submode	R/W	11 10 01 00	T16_Out = 1 T16_Out = 0 Ping-Pong Mode Normal Operation
_____1_	Initial_T8_Out	R/W	1 0	T8_Out set to 1 initially T8_Out set to 0 initially
_____0	Initial_T16_Out	R/W	1 0	T16_Out set to 1 initially T16_Out set to 0 initially

T16 MS-Byte Load Register (TC16H)

The T16 MS-Byte Load Register, as described in Table 48, is loaded with the most significant byte of the T_{16} counter value.

Table 48. TC16H Register (Group/Bank 0Dh, Register 7)

Bit	7	6	5	4	3	2	1	0
Bit/Field	T16_Data_HI							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	T_{16} Data HI	R/W	Data	MS-Byte of the T_{16} Counter

T16 LS-Byte Load Register (TC16L)

The T16 LS-Byte Load Register, as described in Table 49, is loaded with the least significant byte of the T_{16} counter value.

Table 49. TC16L Register (Group/Bank 0Dh, Register 6)

Bit	7	6	5	4	3	2	1	0
Bit/Field	T16_Data_LO							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	T_{16} Data LO	R/W	Data	LS-Byte of the T_{16} Counter

Stop-Mode Recovery Control Registers

The Z86D99/Z86L99 family of products allows 16 individual I/O pins (Ports 2 and 5) to be used as a stop-mode recovery sources. The STOP mode is exited when one of these SMR sources is toggled.