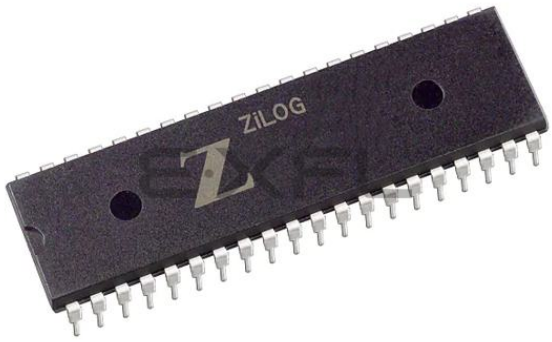

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	489 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86d990pz008sc

  - Three timer interrupts
  - One low-battery detector flag

Operating Characteristics

- 8-MHz operation
- 3.0 V to 5.5 V operating voltage (Z86D990/Z86D991)
- 2.3 V to 5.5 V operating voltage (Z86L990/Z86L991)
- Low power consumption with three standby modes:
  - Stop
  - Halt
  - Low Voltage Standby
- Low-battery detection flag
- Low-voltage protection circuit (also known as V_{BO}, or voltage brownout, circuit)
- Watch-dog timer and power-on reset circuits

User-Programmable Option Bits

- Clock source—RC/other (LC, resonator, or crystal)
- Watch-dog timer permanently enable
- 32-kHz crystal
- Port 20–27 pull-up resistive transistor
- Port 40–42 pull-up resistive transistor
- Port 44–47 pull-up resistive transistor
- Port 50–51 pull-up resistive transistor
- Port 54–57 pull-up resistive transistor
- Port 60–63 pull-up resistive transistor (not available in Z86D991/Z86L991)
- Port 64–67 pull-up resistive transistor (not available in Z86D991/Z86L991)
- P43 high impedance in STOP mode (available in OTP only)

  Force P43 to output a 1 in the open-drain configuration

Operational Description

Central Processing Unit (CPU) Description

The Z8 architecture is characterized by a flexible I/O scheme, an efficient register and address space structure and a number of ancillary features for cost-sensitive, high-volume embedded control applications. ROM-based products are geared for high-volume production (where the software is stable) and one-time programmable equivalents for prototyping as well as volume production where time to market or code flexibility is critical.

Architecture Type

The Z8 register-oriented architecture centers around an internal register file composed of 256 consecutive bytes, known as the standard register file. The standard register file consists of 4 I/O port registers (R2, R4, R5, and R6), 12 control and status registers, 233 general-purpose registers, and 7 registers reserved for future expansion. In addition to the standard register file, the Z86D99/Z86L99 family uses 21 control and status registers located in the Z8 expanded register file. Any general-purpose register can be used as an accumulator and address pointer or an index, data, or stack register.

All active registers can be referenced or modified by any instruction that accesses an 8-bit register, without the requirement for special instructions. Registers accessed as 16 bits are treated as even-odd register pairs. In this case, the data's most significant byte (MSB) is stored in the even-numbered register, while the least significant byte (LSB) goes into the next higher odd-numbered register.

The Z8 CPU has an instruction set designed for the large register file. The instruction set provides a full compliment of 8-bit arithmetic and logical operations. BCD operations are supported using a decimal adjustment of binary values, and 16-bit quantities for addresses and counters can be incremented and decremented. Bit manipulation and Rotate and Shift instructions complete the data-manipulation capabilities of the Z8 CPU. No special I/O instructions are necessary because the I/O is mapped into the register file.

CPU Control Registers

The standard Z8 control registers govern the operation of the CPU. Any instruction which references the register file can access these control registers. The following are available control registers:

- Register Pointer (RP)
- Stack Pointer (SP)
- Program Control Flags (FLAGS)

Grp/Bnk	Reg	Working Register Group Function
(F0h)	r0 to 15	**Control and Status Registers**
(E0h)	r0 to 15	General-purpose RAM registers
(D0h)	r0 to 15	General-purpose RAM registers
(C0h)	r0 to 15	General-purpose RAM registers
(B0h)	r0 to 15	General-purpose RAM registers
(A0h)	r0 to 15	General-purpose RAM registers
(90h)	r0 to 15	General-purpose RAM registers
(80h)	r0 to 15	General-purpose RAM registers
(70h)	r0 to 15	General-purpose RAM registers
(60h)	r0 to 15	General-purpose RAM registers
(50h)	r0 to 15	General-purpose RAM registers
(40h)	r0 to 15	General-purpose RAM registers
(30h)	r0 to 15	General-purpose RAM registers
(20h)	r0 to 15	General-purpose RAM registers
(10h)	r0 to 15	General-purpose RAM registers
	r8 to 15	General-purpose RAM registers
(00h)	r0 to 7	**I/O Port Registers**

Figure 6. Standard Z8 Register File (Working Reg. Groups 0–F, Bank 0)

Z8 Expanded Register File

In addition to the Standard Z8 Register File (Bank 0), Expanded Register File Banks F and D of Working Register Group 0 have been implemented on the Z86D99/Z86L99. Figure 7 illustrates the Z8 Expanded Register File architecture. These two expanded register file banks of Working Register Group 0 provide a total of 32 additional RAM control and status registers. The Z86D99/Z86L99 family has implemented 21 of the 32 available registers.

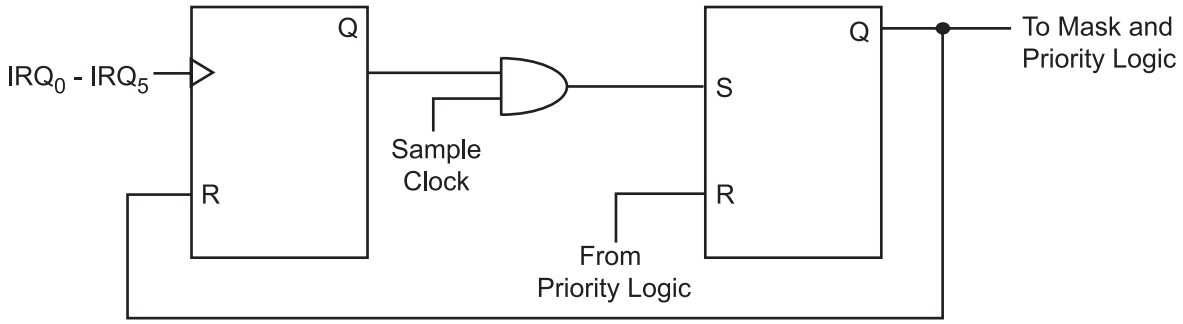


Figure 10. IRQ Logic

Internal interrupt requests are sampled during the most recent clock cycle before an Op Code fetch (see Figure 11.) External interrupt requests are sampled two internal clocks earlier than internal interrupt requests because of the synchronizing flip-flops shown in Figure 9.

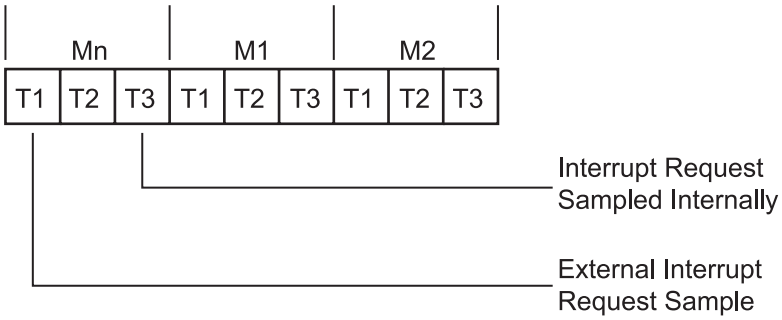


Figure 11. Interrupt Request Timing

At sample time, the interrupt request is transferred to the second flip-flop shown in Figure 10, which drives the interrupt mask and priority logic. When an interrupt cycle occurs, this flip-flop is reset only for the highest priority level that is enabled.

The user has direct access to the second flip-flop by reading and writing to the IRQ. The IRQ is read by specifying it as the source register of an instruction, and the IRQ is written by specifying it as the destination register.

Interrupt Initialization

After RESET, all interrupts are disabled and must be re-initialized before vectored or polled interrupt processing can begin. The Interrupt Priority Register, Interrupt Mask Register, and Interrupt Request Register must be initialized, in that order, to

equivalent to a hardware POR reset. If the mask option of the permanently enabled watch-dog timer is selected, it runs when power up. If the option is not selected, the WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction.

The WDT instruction does not affect the Zero (Z), Sign (S), and Overflow (V) flags. Permanently enabled WDTs are always enabled, and the WDT instruction is used to refresh it. The WDT cannot be disabled after it has been initially enabled. The WDT is off during both HALT and STOP modes.

The WDT circuit is driven by an on-board RC oscillator. The time-out period for the WDT is fixed to a typical value (see Table 57 on page 90).

Power Management

In addition to the standard RUN mode, the Z8 supports three power-down modes to minimize device current consumption. The following three modes are supported:

- HALT
- STOP
- Low-Voltage Standby

Table 6 shows the status of the internal CPU clock (SCLK), the internal Timer clock (TCLK), the external oscillator, and the Watch-Dog Timer during the RUN mode and three low-power modes.

Table 6. Clock Status in Operating Modes

Operating Mode	SCLK	TCLK	External OSC	WDT*
RUN	On	On	On	On
HALT	Off	On	On	Off
STOP	Off	Off	Off	Off
Low-Voltage Standby	Off	Off	Off	Off
Note: * When WDT is enabled by the mask option bit				

Using the Power-Down Modes

In order to enter HALT or STOP mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. You can flush the

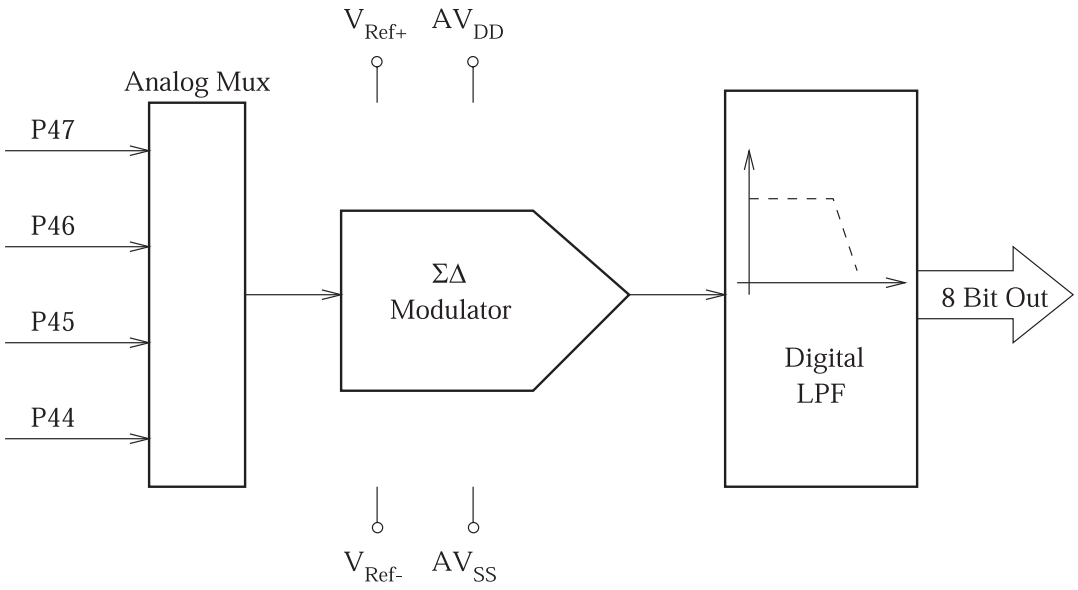


Figure 14. ADC Block Diagram

The low-pass filter transfer function is presented in Figure 15 with the –3-dB frequency given by the formula:

$$f_{3db} = 0.0021 \cdot f_{ADC}$$

where f_{ADC} is the sampling frequency of the modulator.

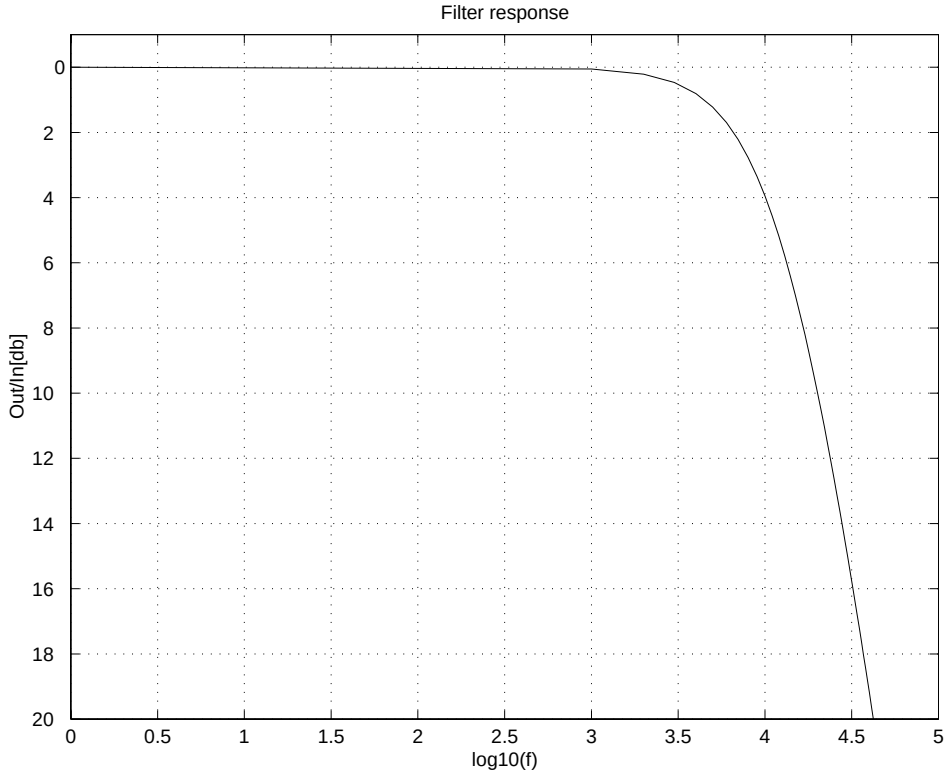


Figure 15. Low-Pass Filter (with 8-MHz Crystal)

The sampling frequency of the modulator f_{ADC} can be selected between f_{SCLK} and $f_{SCLK}/2$ (bit1 from ADCCTRL). Reducing the clock frequency lowers the power dissipated in the ADC block.

The ADC can be enabled or disabled. When enabled, the ΣΔ converter tracks the input voltage. When switching between the channels (step response), the required time to reach the final value is given by the time constant of the low-pass filter:

$$T_{delay} = \frac{2}{f_{3db}} = \frac{2}{0.0021 f_{ADC}} = \frac{952}{f_{ADC}}$$

When available, the reference for the ADC is set externally with the V_{ref+} and V_{ref-} pins. The output code represents the following ratio:

$$D_{out} = \frac{V_{in} - V_{Ref-}}{V_{Ref+} - V_{Ref-}} \times 256$$

Counter/timer 1 is driven by a timer clock generated by dividing the internal clock by four. The divide-by-four stage, the 6-bit prescaler, and the 8-bit counter/timer form a synchronous 16-bit divide chain. Counter/timer T_1 can also be driven by an external input (T_{IN}) using Port P52. Port $P5_6$ can serve as a timer output (T_{OUT}) through which T_1 or the internal clock can be output. The timer output toggles at the end-of-count. Figure 18 is a block diagram of the counter/timer.

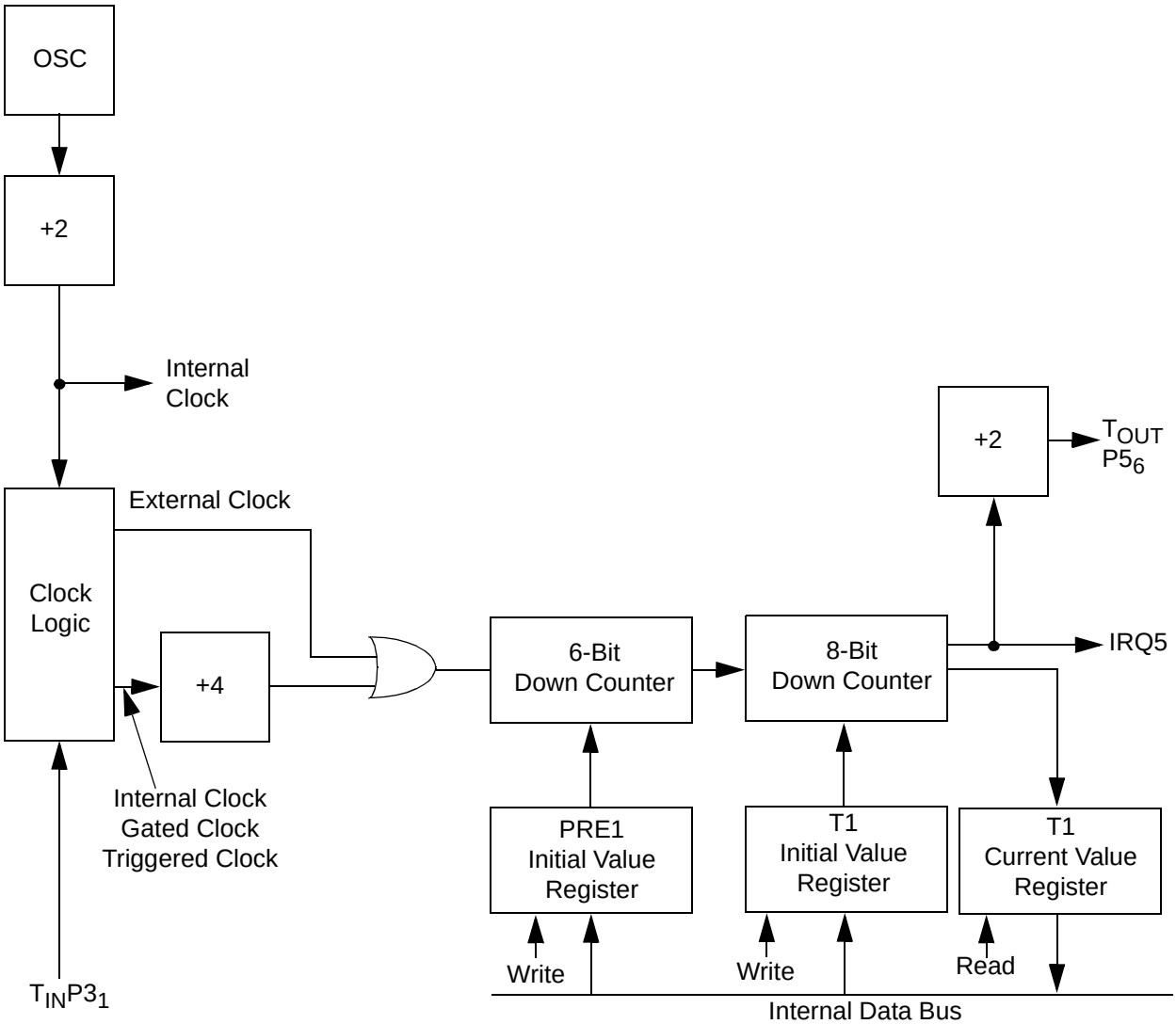


Figure 18. T_1 Counter/Timer Block Diagram

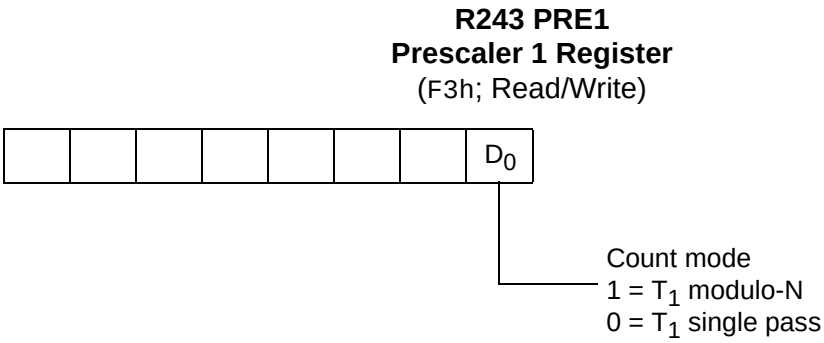


Figure 24. Counting Modes

When the PRE_1 register is loaded with 000000 in the six most significant bits, the prescaler divides by 64. If that number is 000001, the prescaler does not divide and passes its clock on to T_1.

Each time the prescaler reaches its end-of-count, a carry is generated, which allows the counter/timer to decrement by one on the next timer clock input. When T_1 and PRE_1 both reach their end-of-count, an interrupt request is generated—IRQ_5 for T_1. Depending on the counting mode selected, the counter/timer either comes to rest with its value at 00h (single-pass mode), or the initial value is automatically reloaded and counting continues (continuous mode). In single-pass mode, the prescaler still continues to decrement when the timer T_1 has reached its end-of-count. The prescaler always starts from its programmed value upon restarting the counter.

The counting modes are controlled by bit D_0 of PRE_1, with D_0 cleared to 0 for single-pass counting mode or set to 1 for continuous mode.

The counter/timer can be stopped at any time by setting the Enable Count bit to 0 and restarted by setting the Enable Count bit back to 1. The T_1 counter/timer continues its count value at the time it was stopped. The current value in the T_1 counter/timer can be read at any time without affecting the counting operation.

New initial values can be written to the prescaler or the counter/timer registers at any time. These values are transferred to their respective down-counters on the next load operation. If the counter/timer mode is continuous, the next load occurs on the timer clock following an end-of-count. New initial values must be written before the load operation because the prescaler always effectively operates in continuous count mode.

If the value loaded in the T_1 register is 01h, the timer is actually not timing or counting at all; the timer is passing the prescaler end-of-count through. Because the prescaler is continuously running, regardless of the single-pass/continuous mode operation, the 8-bit timer continuously times out at the rate of the prescaler end-of-count if the T_1 timer value is programmed to 01h.

T8 counts down to 0, toggles T8_OUT, sets the time-out status bit (CTR0 D5), and generates an interrupt if enabled (CTR0 D1). This completes one cycle. T8 then loads from TC8H or TC8L, according to the T8_OUT level, and repeats the cycle.

The user can modify the values in TC8H or TC8L at any time.The new values take effect when they are loaded. Do not write these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed. An initial count of 0 causes TC8 to count from 0 to FFh to FEh. Transition from 0 to FFh is not a time-out condition (see Figure 34).

ADC Data Register (ADCDATA)

The ADCDATA register is a read-only register that contains the digital output of the analog-to-digital converter. See Table 20.

Table 20. ADCDATA Register (Group/Bank 00h, Register 7)

Bit	7	6	5	4	3	2	1	0
Bit/Field	ADC Data							
R/W	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	ADC Data	R	Data	Output of the ADC
		W	X	No Effect

Interrupt Control Registers

The Z8 allows up to six different interrupts from a variety of sources. These interrupts can be masked and their priorities set by using the Interrupt Mask Register and Interrupt Priority Register. The Interrupt Request Register stores the interrupt requests for both vectored and polled interrupts.

Interrupt Request Register

The IRQ, as described in Table 23, is a read/write register that stores the interrupt requests for both vectored and polled interrupts. When an interrupt request is made by any of the six interrupts, the corresponding bit in the IRQ is set to 1.

Table 23. IRQ (Group/Bank 0Fh, Register A)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Interrupt Edge		Set IRQ5	Set IRQ4	Set IRQ3	Set IRQ2	Set IRQ1	Set IRQ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76_____	Interrupt Edge Trigger	R/W	11 10 01 00	P51 Rise/FallingP52 Rise/Falling P51 Rising P52 Falling P51 FallingP52 Rising P51 FallingP52 Falling
__5_____	Set IRQ_5	R R W W	1 0 1 0	IRQ_5 Inactive IRQ_5 Active Set IRQ_5 Reset IRQ_5
___4____	Set IRQ_4	R R W W	1 0 1 0	IRQ_4 Inactive IRQ_4 Active Set IRQ_4 Reset IRQ_4
____3___	Set IRQ_3	R R W W	1 0 1 0	IRQ_3 Inactive IRQ_3 Active Set IRQ_3 Reset IRQ_3
_____2__	Set IRQ_2	R R W W	1 0 1 0	IRQ_2 Inactive IRQ_2 Active Set IRQ_2 Reset IRQ_2
______1_	Set IRQ_1	R R W W	1 0 1 0	IRQ_1 Inactive IRQ_1 Active Set IRQ_1 Reset IRQ_1
_______0	Set IRQ_0	R R W W	1 0 1 0	IRQ_0 Inactive IRQ_0 Active Set IRQ_0 Reset IRQ_0

Table 25. P3M Register [Group/Bank F0h, Register 7 (R247)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	Reserved							P2_ Output
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	1

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
7654321_	Reserved	R	1	Always reads 1111111
		W	X	No Effect
_____0	Port 2 Output Configuration	W	1	Push-Pull Active
			0	Open Drain Outputs

Port 2 Control and Mode Registers (P2 and P2M)

Port 2 is a general-purpose 8-bit, bidirectional I/O port, as shown in Table 26. Each of the eight Port 2 I/O lines can be independently programmed as either input or output using the Port 2 Mode Register (see Table 27.)

Table 26. P2 Register [Group/Bank 00h, Register 2 (R2)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	Port 2 Data							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	Port 2 Data	R/W	Data	Port 2 Input/Output Register

Table 27. P2M Register [Group/Bank F0h, Register 6 (R246)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	P27M	P26M	P25M	P24M	P23M	P22M	P21M	P20M
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	1

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210 (by bit)	Port 2 Mode Select	R	1	Always reads 11111111
		W	1	Input
		W	0	Output

Port 5 Control and Mode Registers (P5 and P5M)

Port 5 is a general-purpose 8-bit, bidirectional I/O port, as shown in Table 30. Each of the eight Port 5 I/O lines can be independently programmed as either input or output using the Port 5 Mode Register (see Table 31.)

Table 30. P5 Register [Group/Bank 00h, Register 5 (R5)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	**Port 5 Data**							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X
R = Read, W = Write, X = Indeterminate								

Bit Position	Bit/Field	R/W	Value	Description
76543210	Port 5 Data	R/W	Data	Port 5 Input/Output Register

Table 31. P5M Register (Group/Bank 0Fh, Register 4)

Bit	7	6	5	4	3	2	1	0
Bit/Field	**P57M**	**P56M**	**P55M**	**P54M**	**P53M**	**P52M**	**P51M**	**P50M**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
R = Read, W = Write, X = Indeterminate								

Bit Position	Bit/Field	R/W	Value	Description
7654__10 (by bit)	Port 5 Mode Select	R/W	1 0	Input Output
____32__	P53, P52 Mode Select	R/W	1	Input Regardless of what is written to this pin, P53 and P52 are always in input mode.

A bit set to a 1 in the P5M Register configures the corresponding bit in Port 5 as an input, while a bit set to 0 configures an output line.

Note: Regardless of how P5M bits 2 and 3 are set, P52 and P53 are always in input mode.

T8/T16 Control Register B (CTR3)

The T8/T16 Control Register B, known as CTR3, is a new register to the Z86D99/ Z86L99 family. This register allows the T_8 and T_{16} counters to be synchronized. The settings of CTR3 are described in Table 39.

Table 39. CTR3 Register (Group/Bank 0Dh, Register 3)

Bit	7	6	5	4	3	2	1	0
Bit/Field	T16_ Enable	T8_ Enable	Sync Mode	Reserved				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	X	X	X	X	X

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
7_____	T_{16} Enable	R	1	Counter Enabled
		R	0	Counter Disabled
		W	1	Enable Counter
		W	0	Stop Counter
_6_____	T_8 Enable	R	1	Counter Enabled
		R	0	Counter Disabled
		W	1	Enable Counter
		W	0	Stop Counter
__5____	Sync Mode	R/W	1	Enable Sync Mode
			0	Diable Sync Mode
___43210	Reserved	R	1	Always reads 11111
		W	X	No Effect

T8 High Capture Register (HI8)

The T8 High Capture Register, as described in Table 41, holds the captured data from the output of the T_8 counter/timer. This register is typically used to hold the number of counts when the input signal is high (or 1).

Table 41. HI8 Register (Group/Bank 0Dh, Register B)

Bit	7	6	5	4	3	2	1	0
Bit/Field	T8_Capture_HI							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	T_8 Capture High Value	R W	Data	Captured Data No Effect

T8 Low Capture Register (LO8)

The T8 Low Capture Register, as described in Table 42, holds the captured data from the output of the T_8 counter/timer. This register is typically used to hold the number of counts when the input signal is low (or 0).

Table 42. LO8 Register (Group/Bank 0Dh, Register A)

Bit	7	6	5	4	3	2	1	0
Bit/Field	T8_Capture_LO							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	T_8 Capture Low Value	R W	Data	Captured Data No Effect

Analog-to-Digital Converter Characteristics

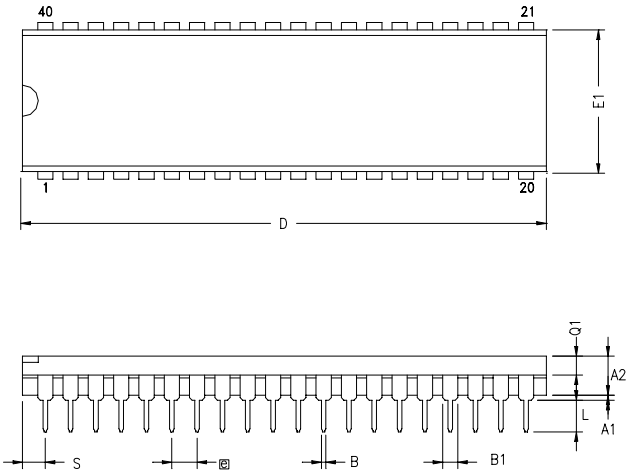
Table 56 lists the analog-to-digital converter characteristics.

Table 56. Analog-to-Digital Converter Characteristics

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		bits
Integral Nonlinearity		0.5	1	LSB
Differential Nonlinearity		0.5	1	LSB
Zero Error at 25 °C			7.8	mV
Supply Voltage Range (OTP)	3.0		5.5	V
Supply Voltage Range (ROM)	2.3		5.5	V
Power Dissipation (No Load)			1.2	mW
Clock Frequency (f ADC)			4	MHz
Input Voltage Range	V_{Ref-}		V_{Ref+}	V
Step Response			2/(0.0021 X f ADC)	s
ADC Input Capacitance	25		40	pF
Vref Input Capacitance	25		40	pF
V_{Ref+} Range	V_{Ref-}+2.0		AV_{DD}	V
V_{Ref-} Range	AGND		V_{Ref+}–2.0	V
$(V_{Ref+})–(V_{Ref-})$	2.0		AV_{DD}	V
Temperature Range	0		70	°C
3-db Frequency		(0.0021 X f ADC)		Hz
Signal to Noise	47			db
ADC Output Code		Dout		
Vref Input Source Impedance			1.0	kOhms
ADC Input Source Impedance			1.0	kOhms

Notes: Dout= $[(Vin–V_{Ref-})/(V_{Ref+}–V_{Ref-})]$ X 256
f ADC = set in ADCCTRL configuration register
Step Response is the time to track the input if a step from V_{Ref-} to V_{Ref+} is applied.

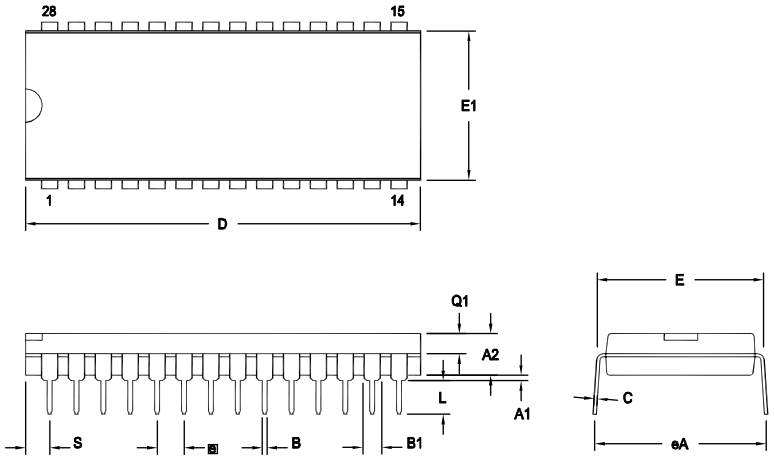
The ADC input is a switching capacitor that charges up to the applied input voltage whenever it is configured as an ADC input. If you switch it from digital mode to



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

Figure 38. 40-Pin PDIP



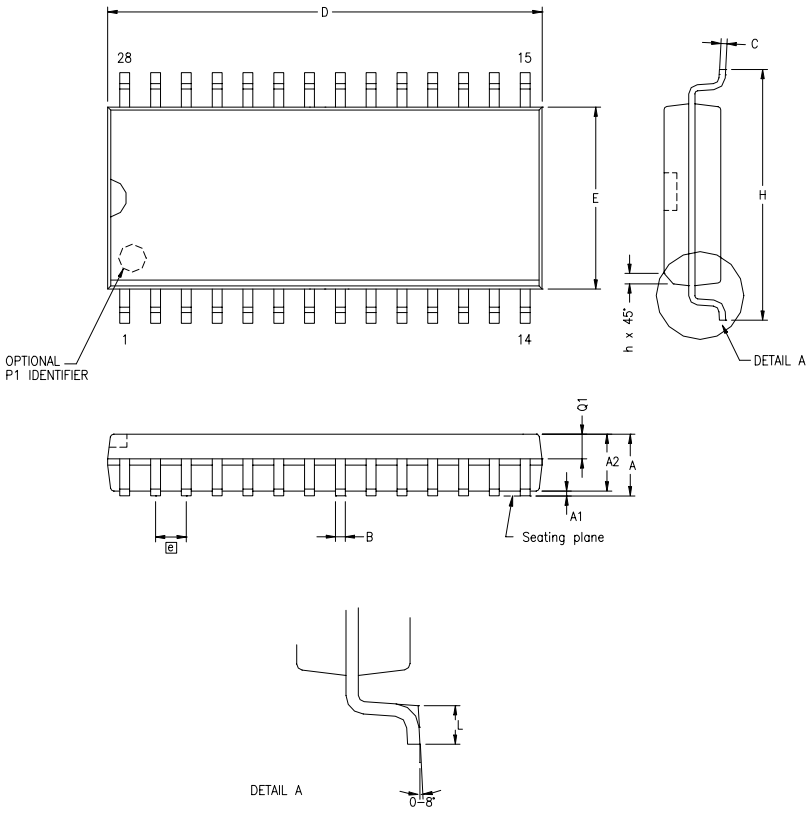
SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Note: ZiLOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 39. 28-Pin PDIP



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 40. 28-Pin SOIC

Design Considerations

The Z8 uses a Pierce oscillator with an internal feedback circuit. The advantages of this circuit are low cost, large output signal, low-power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects.)

One drawback is the requirement for high gain in the amplifier to compensate for feedback path losses. Traces connecting crystal, capacitors, and the Z8 oscillator pins must be as short and wide as possible. Short and wide traces reduce parasitic inductance and resistance. The components (capacitors, crystal, and resistors) must be placed as close as possible to the oscillator pins of the Z8.

The traces from the oscillator pins of the integrated circuit (IC) and the ground side of the lead capacitors must be guarded from all other traces (clock, V_{CC}, and system ground) to reduce cross-talk and noise injection. Guarding the traces is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit and by placing a Z8 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead capacitors must be connected to a single trace to the Z8 V_{SS} (GND) pin. It must not be shared with any other system ground trace or components except at the Z8 device V_{SS} pin. Not sharing the ground side of the oscillator lead capacitors is to prevent differential system ground noise injection into the oscillator.